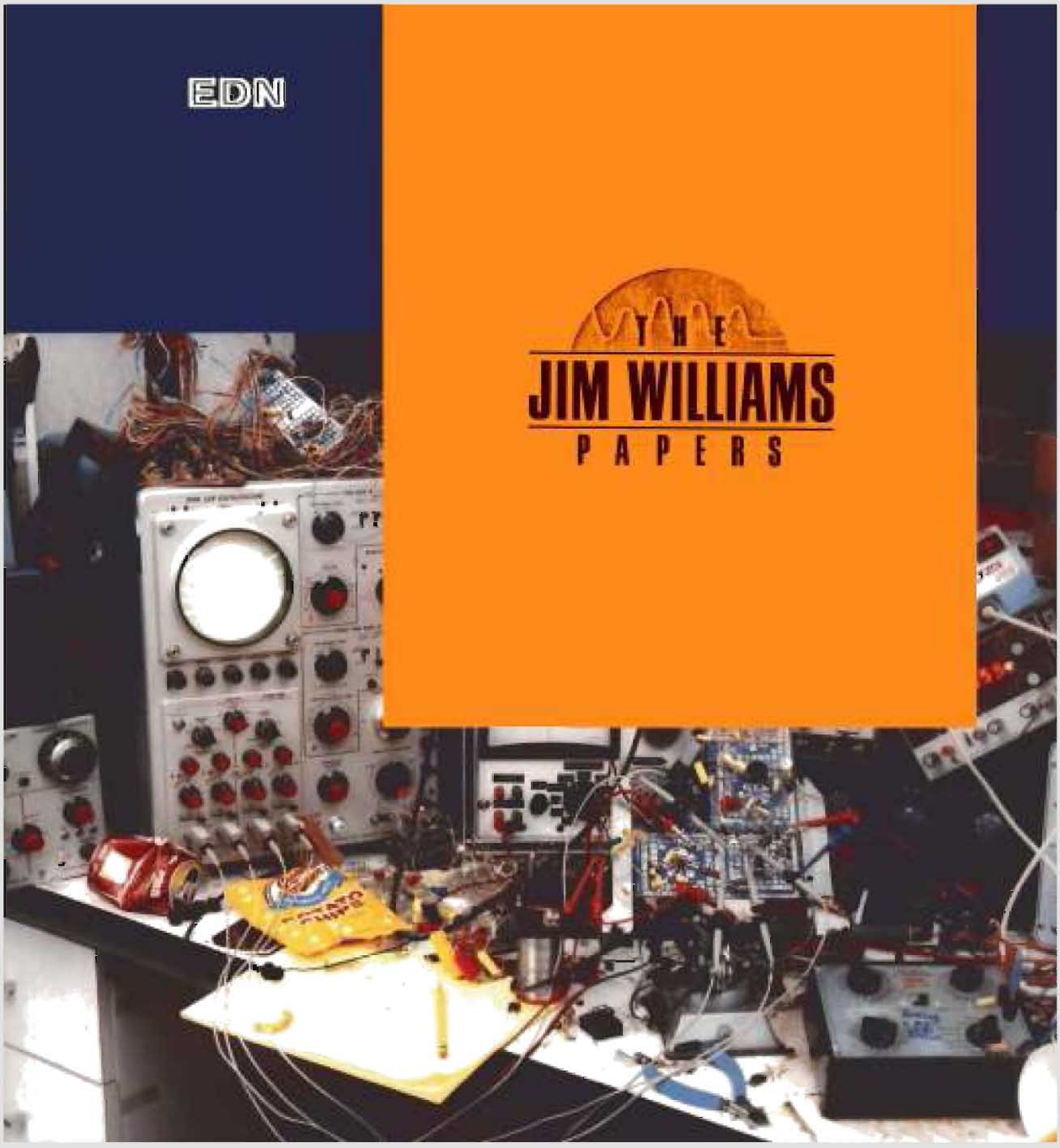
# *A Tribute to Jim Williams*

## EDN – 2 (1990-1999)



# Basic principles and ingenious circuits yield stout switchers

*A substantial percentage of power supplies are step-down regulators. Although the theory of step-down, "buck" switching regulators is well established, myriad practical details, if mishandled, can spoil the theory's pristine beauty. Luckily, convenient, easily applied switching-regulator ICs have recently become available.*

Jim Williams, *Linear Technology Corp*

To design a step-down switching regulator, you can't just copy a circuit from a data sheet or use a theoretical method from a book. Designing step-down switching regulators means solving a nettlesome host of problems and properly following some basic principles.

By far, the toughest nuts to crack are the magnetic components. Magnetic components account for probably 90% of the problems in switching-regulator design. Because of the overwhelming level of difficulty associated with magnetic components, you must choose them judiciously.

The most common magnetic-component problem is saturation. An inductor saturates when it cannot support any more magnetic flux. As an inductor saturates, it begins to look more resistive and less inductive. When it's saturated, only the inductor's dc copper resistance and the source's capacity limit current flow. Thus, saturation often results in destruction.

Although you could apply electromagnetic theory (**Ref 1**), practically speaking, an empirical approach is often the best way for you to select inductors. A practical approach involves real-time analyses using the ultimate simulator—a breadboard. If you desire, you can use inductor-design theory to augment or confirm your experimental results.

**Fig 1** shows a typical step-down switching regulator. The #845 inductor kit from Pulse Engineering (San Diego, CA) proves useful at the breadboard stage. **Fig 2a** shows the results of installing a 450-μH, high-capacity-core inductor in **Fig 1**'s circuit and the circuit running at its intended voltage and current levels. Trace A is the regulator-IC $V_{SW}$ pin's voltage; trace B shows its current. When $V_{SW}$ is high, inductor current flows. This particular inductor's high value results in the current rising relatively slowly. The circuit's behavior is linear, indicating that no saturating is occurring.

**Fig 2b** shows the results of installing a lower-value unit. Although the current rises at a steeper rate, the inductor does not saturate. **Fig 2c** shows a still lower inductance. Here the current ramp is quite pronounced, but still well controlled. **Fig 2d** brings some informative surprises. This high-value unit, wound on a low-capacity core, starts out well but saturates rapidly; it is clearly unsuitable.

Trying out different inductors this way quickly narrows your choice to a range of devices. Several may produce acceptable results. You could further select

*Think carefully about your capacitors' requirements; you must account for all operating conditions.*

When the $V_{SW}$ pin is off, current is no longer available to charge the inductor. The magnetic field therefore collapses, causing the $V_{SW}$ pin's voltage to go negative, ending the similarity to the basic regulator. In the modified version the output current (trace F) receives a boost as the magnetic field collapses. The boost results when the energy stored in the tapped inductor transfers to the output. This current step circulates through C1 and D2 (trace E) and increases the output-voltage ripple.

Not all the energy, however, transfers to the output-side turns. Current (trace C) will continue to flow in the switch-side winding because of leakage inductance, whose effects are suppressed by a snubber network. To minimize snubber losses, the tapped inductor is bifilar wound for maximum coupling.

In most instances the switching regulator's output will go directly to the load. However, those applications requiring faster transient response or reduced noise will benefit from linear post regulation. To incur minimal efficiency losses, you must set the switching-regulator IC's output to provide just enough voltage to the linear regulator to maintain regulation. In such applications, a low-dropout linear regulator works best.

### Post regulation, variable case

Some applications require variable linear post regulation (**Fig 9a**). The circuit operates with little efficiency sacrifice. The linear regulator operates in normal fashion, supplying a variable 1.2 to 28V output. The remainder of the circuit forms a switched-mode preregulator that maintains a small, fixed voltage

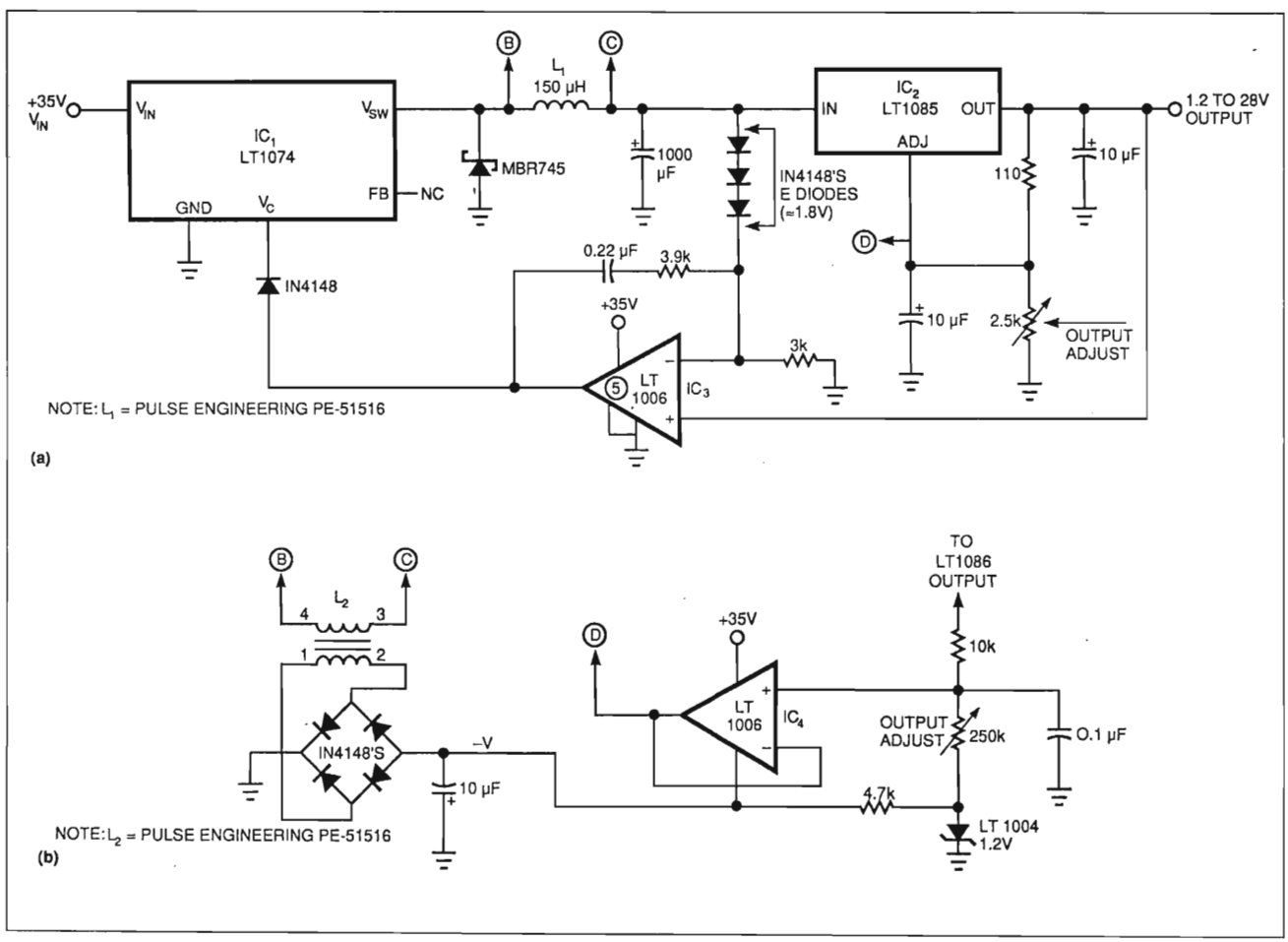



***Fig 9—The feedback loop of this variable-output regulator, (a), ensures that the voltage impressed across the linear postregulator, set by the "E" diode string, is always just the minimum voltage it needs to operate. The optional circuit in (b) permits output voltages down to 0V.***

*Layout is vital; don't mix signal, frequency-compensation, and feedback returns with high-current returns.*

across the linear regulator regardless of its output.

$IC_3$ biases the step-down switching regulator to produce whatever voltage is necessary to maintain the "E diodes" potential across the linear regulator. You can adjust the number of diodes in the "E diode" string to achieve different voltages across the linear regulator. $IC_3$'s inputs are balanced when the linear regulator's output is "E diodes" below its input. $IC_3$ maintains this condition regardless of line, load, or output-voltage conditions. Thus, the circuit maintains good efficiency over the full range of output voltages. The RC network at $IC_3$ compensates the loop.

Deliberately introducing a positive offset to $IC_3$ ensures loop startup. Grounding $IC_3$'s appropriate balance (in this case pin 5), induces the offset, resulting in a positive 6-mV offset, which, normally considered poor practice because it increases amplifier drift, causes no measurable error in this application. As shown, the circuit cannot produce outputs below the regulator IC's 1.2V internal reference. Applications requiring outputs adjustable down to 0V will benefit from the option in **Fig 9b**, which replaces $L_1$ with $L_2$. $L_2$'s primary winding performs the same function as $L_1$'s, while its coupled secondary winding produces a negative-bias output, $-V$. The negative bias allows regulated outputs down to 0V.

The $-V$ potential derived from $L_2$'s secondary winding varies considerably with operating conditions; wildly varying duty cycles necessitate the optional circuit's full-wave bridge rectifier. The high feedback string values and $IC_4$'s buffering ensure that the circuit will be stable for "starved" values of $-V$. $IC_4$ and its attendant circuitry replace all components associated with the linear regulator's ADJ pin.

### Low quiescent-current regulators

Many applications require currents in the ampere range under normal conditions, but only microamperes while in standby or "sleep" mode. A typical laptop computer, for example, may draw 1 to 2A running, but need only a few hundred microamperes for its memory when turned off. In theory, any regulator, with a loop properly designed to be stable under no load, will work. In practice, a switcher having relatively large quiescent current may be unacceptable because of excessive battery drain during low current-output periods—even if it operates serenely.

**Fig 10**'s simple loop effectively reduces circuit quiescent current from 6 mA to only 250 μA. The circuit uses the regulator IC's shutdown pin. When the circuit pulls this pin to within 350 mV of ground, the IC shuts down and draws only 1200 μA. Short on times keep the duty cycle low, resulting in the small, effective quiescent current. Comparator $IC_2$ combines with the regulator IC's reference and $Q_1$ to form a "bang-bang" control loop around the regulator IC, which bypasses the regulator IC's internal feedback amplifier and reference.

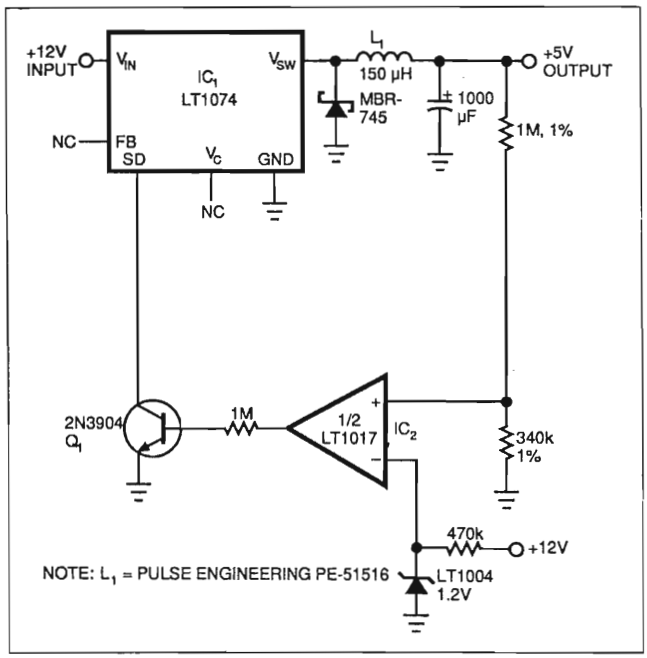



***Fig 10—This circuit's simple loop** reduces its quiescent current from 6 to only 250 mA by switching the regulator off at low loadings.*

When the circuit's output falls slightly below 5V, $IC_2$'s output switches low, turning off $Q_1$ and enabling the regulator IC. The $V_{SW}$ pin then pulses at full duty cycle, forcing the output back above 5V. $IC_2$ then biases $Q_1$ on again, the regulator IC goes into shutdown, and the external loop's action repeats. The frequency of this on-off control action is directly load dependent, with typical repetition rates of 0.2 Hz at no load. The on-off operation combines with the LC filtering action in the regulator's $V_{SW}$ line to generate an output hysteresis of about 50 mV.

The external loop performs well but has two potential drawbacks. At higher output currents the loop oscillates in the 1 to 10-kHz range, causing audible noise, which users may object to. Also, the control loop's operation forces about 50 mV of ripple on the output. Ripple frequency ranges from 0.2 Hz to 10 kHz depending on input voltage and output current.

*Transients usually cause the most trouble for diodes, introducing stresses whose results are often hard to predict.*

**Fig 11**'s more sophisticated circuit eliminates these two problems with some increase in complexity while maintaining quiescent current at 150 μA. The technique is particularly significant, having broad implications in battery-powered systems because you can easily apply it to a wide variety of regulators.

**Fig 11**'s signal flow is similar to **Fig 10**'s, but additional circuitry appears between the feedback divider and the regulator IC. The circuit does not use the regulator IC's internal feedback amplifier and voltage reference. Under no load, the output voltage will slowly ramp down over a period of seconds, during which the comparator $IC_1$'s output is low, as are the outputs of the paralleled 74C04 inverters. The inverters, in turn, pull the regulator IC's $V_C$ pin low, forcing the IC to a zero duty cycle. Simultaneously, $IC_2$'s output is low, putting the regulator in shutdown mode. Therefore, the $V_{SW}$ pin is off and no inductor current flows.

When the output drops by about 60 mV, $IC_1$ triggers and the inverters go high, pulling the $V_C$ pin up and biasing the regulator. $IC_2$ also rises, taking the IC out of shutdown mode. The $V_{SW}$ pin then pulses the inductor at its normal, 100-kHz clock rate, causing the output to rise abruptly. This action trips $IC_1$ low, forcing the $V_C$ pin back low and shutting off $V_{SW}$'s pulsing. $IC_2$ also goes low, putting the IC back into shutdown.

This "bang-bang" control loop keeps the 5V output's level within the loop's 60-mV hysteresis window. Note that compared with the loop's oscillation period of seconds, the $R_1$-$C_2$ time constant at $V_C$ is not significant. Because the regulator spends almost all of its time in shutdown mode, the circuit draws very little quiescent current—150 μA.

As the load increases, the loop's oscillation frequency increases to keep up with the load's demand; $R_1$-$C_1$ begins to filter the waveform at the $V_C$ pin. If the load continues to increase, the loop's oscillation frequency will also increase. The $R_1$-$C_1$ time constant, however, is fixed. Beyond some frequency, $R_1$-$C_1$ must average loop oscillations to dc. Here, the $V_C$ waveform becomes heavily filtered at loads of 7 mA and above. At 1A

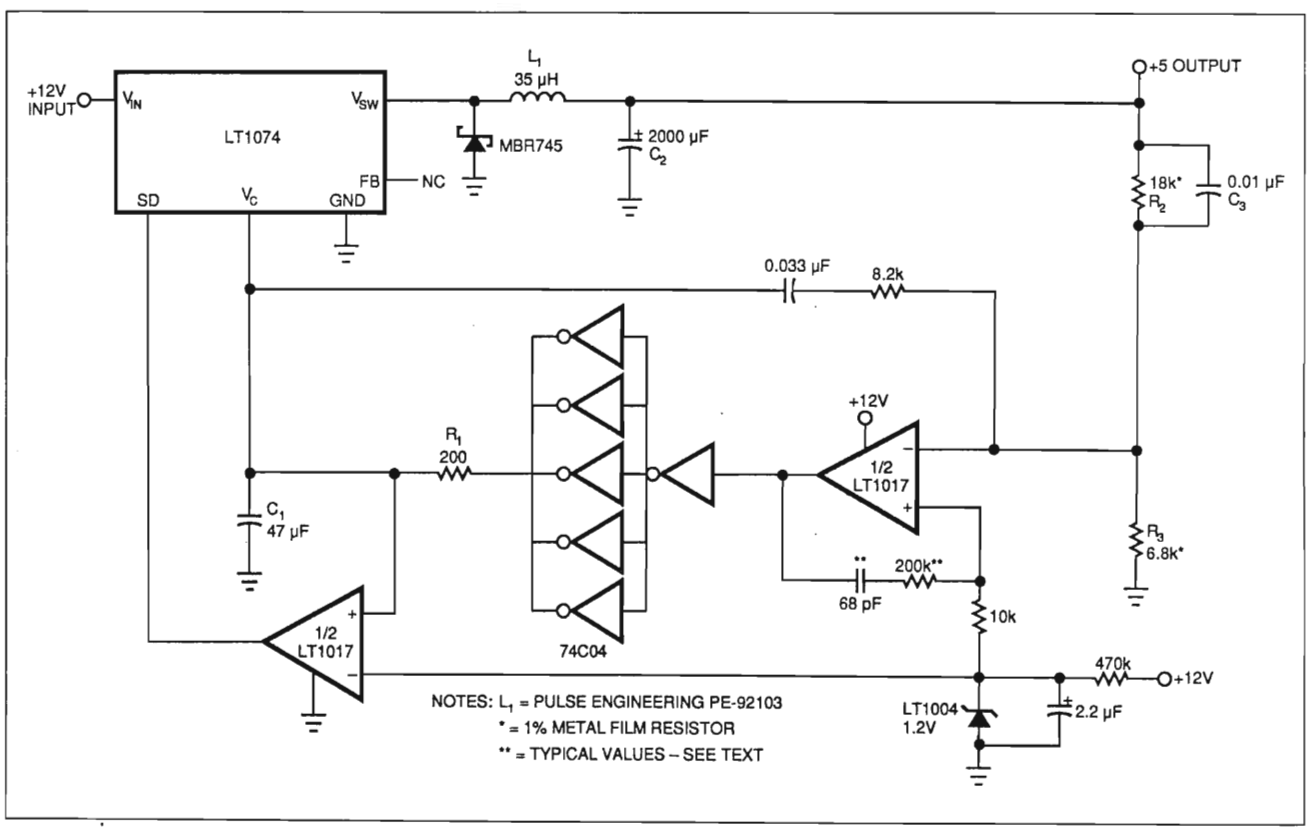



***Fig 11—The RC filter at the regulator IC's $V_C$ pin gradually filters the quiescent-current, switched-feedback circuit's pulsed output to a steady dc signal as the output load increases, thereby canceling unwanted cycling of the regulator IC at high loads.***

*In theory, any regulator, with a loop properly designed to be stable under no load, will work.*

loads, the regulator IC's $V_C$ pin will see pure dc; the regulator IC will be running at its full 100-kHz clock rate.

With the $V_C$ pin at dc, you can conveniently think of $IC_1$ and the inverters as a linear error amplifier with a closed-loop gain set by the $R_2$-$R_3$ feedback divider. In fact, $IC_1$ is *still* trying to modulate the duty cycle at the $V_C$ pin, but at a rate far above $R_1$-$C_1$'s break frequency. $R_1$-$C_1$'s roll-off and the phase lead of $C_3$ into $IC_1$ dominate $C_2$'s phase error ($C_2$ was, after all, selected for low loop frequency at low output currents).

The loop is stable and responds linearly for all loads beyond 10 mA. In its high-current region, the regulator IC is desirably fooled into behaving like a conventional step-down regulator.

### Formal analysis difficult

A formal stability analysis for this circuit is quite complex; simplifying it somewhat lends insight into the loop's operation. At 250 μA, $C_2$ and the 20-kΩ load form a decay-time constant exceeding 30 sec. This delay is orders of magnitude larger than $R_2$-$C_2$, $R_1$-$C_1$, or the regulator IC's 100-kHz commutation rate. As a result, $C_2$ dominates the loop. Wideband comparator $IC_1$ sees phase-shifted feedback, and very low-frequency oscillations occur. Although $C_2$'s *decay* time constant is long, its *charge* time constant is short because the circuit has low sourcing impedance. This difference accounts for the ramp nature of the oscillations.

Increased loading reduces the $C_2$-load decay time constant. As loading increases, the loop oscillates at a higher frequency because of $C_2$'s decreased decay time. When the load impedance becomes low enough, $C_2$'s decay time constant ceases to dominate the loop. $R_1$ and $IC_2$ almost entirely determine this point. Once $R_1$ and $IC_2$ reign as the dominant time constant, the loop begins to behave like a linear system. Now, $C_3$ becomes significant, performing as a simple feedback lead to smooth output response ("zero compensation" for all you technosnobs out there).

A fundamental tradeoff exists for $C_3$'s phase lead. When the switcher is running in its linear region, $C_3$'s phase lead must dominate the loop's time-lag-generated hysteretic characteristic. As such, select $C_3$ to be the best compromise between output ripple at high load and loop-transient response.

Despite the circuit's complex dynamics, its transient response is quite good. Further, its high-power efficiency is similar to standard switchers; low-power efficiency is somewhat better—although poor in the lowest ranges. The poor efficiency is not particularly bothersome, because power loss is very small.

The loop provides a controlled, conditional instability instead of the usually more desirable (and often elusive) unconditional stability. This deliberately introduced instability dramatically lowers switcher quiescent current without sacrificing high-power performance. EDN

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## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

Article Interest Quotient (Circle One)
High 491 Medium 492 Low 493

*Magnetic components account for probably 90% of the problems in switching-regulator design.*

the optimal unit on the basis of other parameters, such as cost, size, and operating temperature. A standard device may suffice, or the inductor manufacturer can supply a customized version.

### The invasion of the drawer dwellers

An alternate inductor-selection method exists—one favored by those who have no inductor kit, time, or adequate instruments. You can use this alternate method when faced with an immediate deadline and a drawer full of inductors of unknown or questionable lineage. Confronting these challenges, engineers often simply insert one of these drawer dwellers into an unsuspecting circuit.

Although this method's theoretical underpinning is perhaps questionable, its seemingly limitless popularity compels coverage. At Linear Technology, we've developed a 2-step procedure for screening inductors of unknown characteristics. Inductors passing both stages of the test have an excellent chance (75%—based on a sample of randomly selected inductors) of performing adequately in a prototype circuit. The only instruments required are an ohmmeter and a scale.

The first test consists of weighing the candidate inductor. Acceptable limits range between 0.01 and 0.25 lbs. The second test involves measuring the inductor's dc resistance. Acceptable limits are usually between 0.01 and 0.25Ω.

When using an inductor selected by this method, by all means try low power first, then gradually increase loading. As you increase loading, observe the inductor's and regulator chip's heating, making sure that their dissipation is no more than warm to the touch. Disproportionate heat increases as you increase the load probably indicate that the inductor is saturating. Either reduce the load or go back to the drawer and try again.

### Capacitors require consideration

Think carefully about your capacitors' requirements, as you must account for all operating conditions. Though voltage rating is the most obvious consideration, remember to also plan for the effects of the capacitors' equivalent series resistance (ESR) and inductance. These specifications can have significant impact on your circuit's performance. In particular, an output capacitor with high ESR can make compensating the loop difficult or decrease efficiency. Other considerations are layout, diode breakdown, and switching requirements.

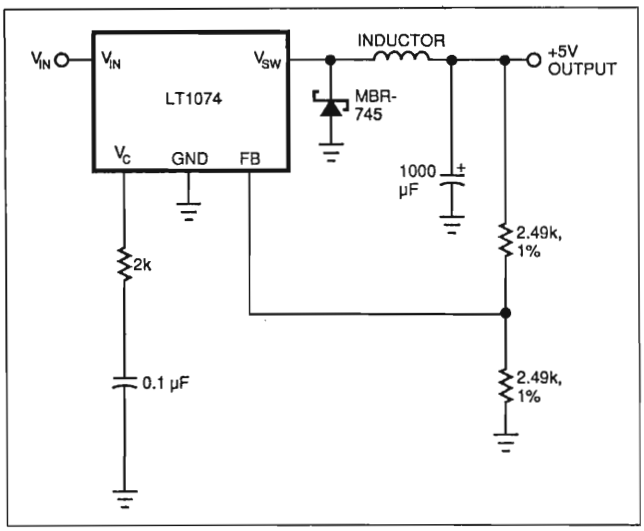



***Fig 1—You can use a typical switching-regulator** circuit to sample candidate inductors.*

Layout is vital. Don't mix signal, frequency-compensation, and feedback returns with high-current returns. Arrange the grounding scheme for the best compromise between ac and dc performance. In many cases, a ground plane may help. Account for possible effects of stray flux from the inductor or other components and plan your layout accordingly.

You must think through diodes' breakdown and switching ratings and account for all operating conditions. Transients usually cause the most trouble for diodes, introducing stresses that are often hard to predict. Study the datasheet's breakdown, current capacity, and switching-speed ratings carefully. Ask yourself if these specifications were determined under the same conditions as those in your circuit. If in doubt, consult the manufacturer.

Switching diodes have two important transient characteristics: reverse-recovery time and forward turn-on time. Reverse-recovery time occurs because the diode stores charge during its forward-conduction cycle. This stored charge causes the diode to act as a low-impedance conductive element for a short period of time after reverse drive is applied.

Hard turn-off diodes switch abruptly from one state to the other following reverse-recovery time. They therefore dissipate very little power, even with moderate reverse-recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can dissipate considerable power during the turn-off interval.

Even fast diodes can be useless if stray inductance

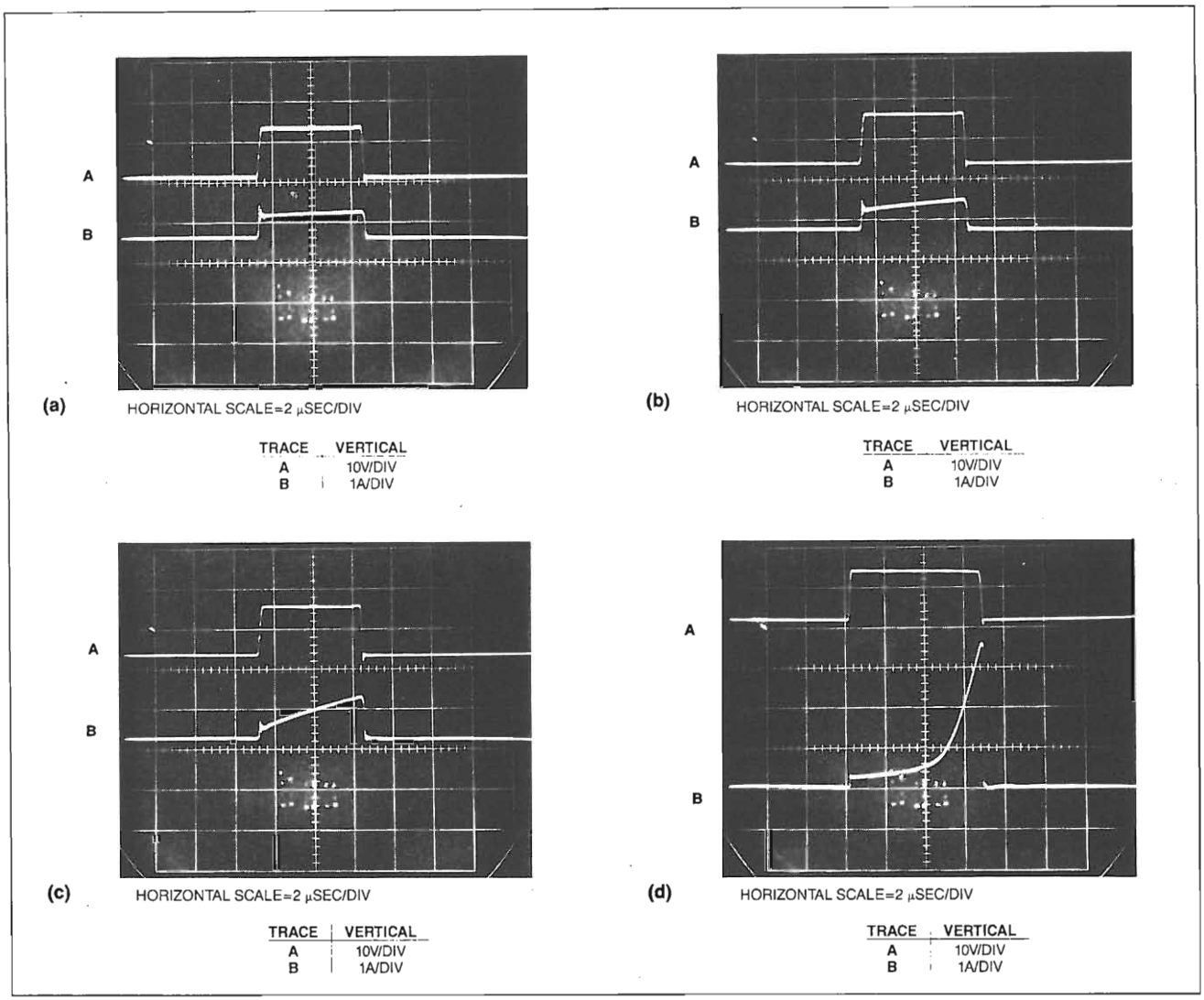



***Fig 2—After installing a 450-μH,*** *high-capacity-core inductor in the test circuit the waveforms in* ***(a)*** *result: Trace A is the regulator-IC* $V_{SW}$ *pin's voltage; trace B is its current waveform. A lower-value, 170-μH inductor produces these waveforms* ***(b)****. After installing an even lower-value, 55-μH inductor, the current ramp becomes quite pronounced* ***(c)****. In* ***(d)****, a 500-μH, low-capacity-core inductor plainly has too low a value because the current waveform shows that the inductor has quickly saturated.*

in the diode, output capacitor, or control loop is high. Remember that 20-gauge hook-up wire has 30 nH/in. of inductance. Currents switching on the order of 10 A/sec are typical in regulator circuits. These fast-changing currents can easily generate several volts/in. across the wiring's stray inductance. Keep the diode, capacitor, and regulator-chip-lead lengths short.

The basic step-down configuration of **Fig 1** is relatively free of frequency-compensation difficulties. A simple RC damper network from the $V_C$ pin to ground will usually suffice. Things become more complex when you add gain- and phase-contributing elements to the regulator's control loop. In these cases, you should view the regulator IC as a low-bandwidth power stage. The stage's delays arise from the sampled-data nature of its power delivery (100-kHz switching frequency) and its output LC filter. In general, limiting the regulator's gain-bandwidth product below that of the added loop elements will stabilize such a complex loop. This principle accords with established feedback theory.

Squeezing the utmost efficiency out of a switching regulator is a complex, demanding design task. Effi-

*The most common magnetic-component problem is saturation.*

ciency exceeding 80 to 85% requires some combination of finesse, witchcraft, and just plain luck. Interacting electrical and magnetic terms produce subtle effects that influence efficiency. A detailed, generalized method for obtaining maximum converter efficiency isn't possible, but some guidelines do exist.

Losses fall into several loose categories including drive, junction, ohmic, switching, and magnetic. Semiconductor junctions produce losses. Diode drops increase with operating current and can be quite costly in low-output-voltage switchers. For example, a 700-mV drop in a 5V-output switcher introduces more than a 10% loss. Though Schottky devices will cut the loss nearly in half, it is still appreciable. The ohmic losses in germanium diodes (now rarely used) are lower still, but switching losses negate the low dc drop of germa-

## Techniques and equipment measure changing current

Accurately measuring rapidly changing current flow is essential to switching-regulator design. In many cases, current waveforms contain more valuable information than do voltage measurements.

The most powerful and convenient current-measuring tool is the clip-on current probe. The Tektronix P-6042 (bottom left in **Fig A**) is a Hall-effect, stabilized current transformer that responds from dc to 50 MHz.

These clip-on probes contain a current transformer and a Hall-effect transducer. The transducer senses current at dc and low frequencies; the transformer simultaneously processes the signal's high-frequency content. Their dc response allows you to determine the dc content of high-speed current waveforms. Sensitivities range from fractions of a milliampere to amperes.

The combination of convenience, broad bandwidth, and dc response make Hall-effect, stabilized current probes the instruments of choice for converter designers.

Transformer-based clip-on current probes are also available. Though they lack the dc response of their Hall-effect cousins, they're still quite useful. The Tektronix type 131 (upper left, **Fig A**), and the more modern 134, respond from hundreds of hertz to about 40 MHz.

AC current probes are also available with a simple termination (left foreground **Fig A**). These devices are more difficult to use than the actively terminated models because of their complex gain switching. Their low-frequency response is also poorer, although their high-frequency response exceeds 100 MHz.

The simple transformer (**Fig A**'s foreground) is a final form of ac current probe. These transformers are not clip-on devices, and they usually have significant performance limits compared with the clip-on instruments. However, they are inexpensive and can provide meaningful measurements when used according to manufacturers' recommendations. In practice, you thread the conductor through the opening provided and monitor the signal at the transformer's output pins.

**Fig A** also shows a wide-ranging dc clip-on current probe. The Hewlett-Packard 428B (upper right) responds from dc to only 400 Hz but features 3% accuracy over a 100-μA to 10A range. The instrument obviously cannot distinguish high-speed events, but it is invaluable for determining overall efficiency and quiescent current.

A great strength of these probes is that they take a fully floating measurement. Extract-

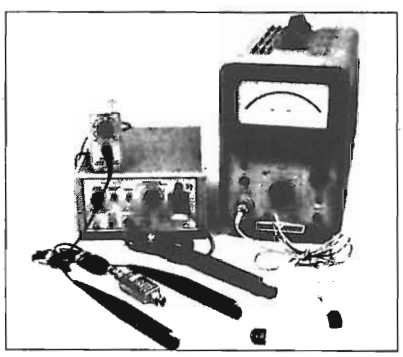


***Fig A—A host of devices can help** you make current measurements.*

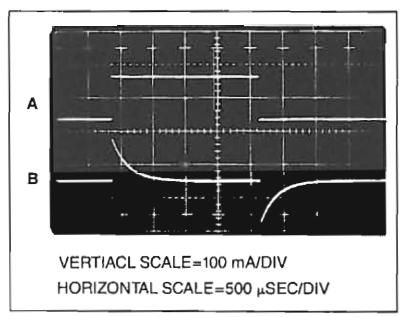



***Fig B—Trace A is the output of a** stabilized Hall-effect current probe, and trace B is the same signal measured with a transformer-based probe; clearly, the transformer-based probe is useless at low frequencies.*

nium at high switching speeds. In very low-power switchers, germanium's reverse leakage may be equally oppressive. Synchronously switched rectifiers are more complex, but can sometimes simulate a more efficient diode.

When evaluating rectifying and switching schemes, remember to include both ac and dc drive losses in your efficiency estimates. DC losses include base or gate current in addition to dc consumption in any driver stage. AC losses might include the effects of base or gate capacitance, transition-region dissipation (the switch spends some time in its linear region), and power lost because of timing skew between drive signals and actual switch action.

The LT1074 regulator IC's output switch, for example, comprises a PNP transistor driving a power NPN

ing current information via magnetic coupling eliminates common-mode voltage considerations. As good as they are, however, current probes have limits and characteristics that you must remember in order to avoid unpleasant surprises. At high currents, for example, the probe may saturate. The saturation will corrupt the resulting CRT waveforms, rendering the measurement useless and confusing the unwary.

Further, for Hall-effect types, noise interferes with measurements below a few hundred microamperes. Luckily, this noise is obvious on the display.

Keep in mind that signal-transit delays vary from current probe to current probe and all are different from voltage probes. At high-sweep speeds these effects show up in multitrace displays as time skewing between individual channels. You can mentally factor in the current probes' transit-time delay to reduce error when interpreting the display. Note that active probes have the longest signal transit, on the order of 25 nsec.

When interpreting CRT displays,you must also keep in mind the low-frequency bandwidth restrictions of ac current probes. **Fig B** clearly demonstrates this principle by showing the ac probe's inability to follow low frequency. Similarly, remember that the probe's stated bandpass is −3 dB, meaning that signal information is not entirely present in the display at this frequency. When working at, or approaching, either end of the probe's bandpass consider that displayed information may be distorted or incomplete.

There are other ways to measure wideband current signals, although they're less convenient and desirable than clip-on current probes. Current shunts (**Fig C**, foreground) are low-value resistors with 4-terminal connections for accurate measurement. In theory, measuring voltage across a current shunt should yield accurate information. In practice, common-mode voltages introduce measurement difficulties, particularly at speed. Making such measurements requires an isolated probe or high-speed differential oscilloscope plug-in. The isolation amplifier in **Fig C** from Signal Acquisition Technologies (Minden, NV), has a 10-MHz bandwidth, a galvanically floating input, and 600V common-mode capability. The instrument allows any oscilloscope to take a floating measurement across a shunt.

Differential oscilloscope plug-ins, while not galvanically floating, can measure the voltage across a shunt. Tektronix types W, 1A5, and 7A13 have 1-mV sensitivity with a bandwidth as high as 100 MHz and excellent common-mode rejection. Types 1A7 and 7A22 have 10-μV sensitivity, although their bandwidth is limited to 1 MHz. All differential plug-ins have bandwidth or common-mode-voltage restrictions that vary with sensitivity. You must review these tradeoffs when you select the optimal shunt value for a particular measurement. In general, the smallest practical shunt value is preferable. This small value minimizes the inserted resistance's parasitic effects on the circuit's operation.

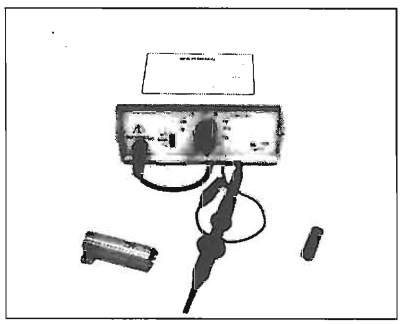


***Fig C—Current shunts are low-value** resistors having 4-terminal connections for accurate current measurements.*

*An empirical approach, using the ultimate simulator—a breadboard—is often the best way for you to select inductors.*

transistor. The switch's drop can reach 2V at high currents. This drop will usually be the major loss in the circuit. You can mitigate the drop's effect on efficiency by using the highest possible input voltage. Higher output voltages will further minimize losses.

Actual losses from switch-saturation effects and diode drops are sometimes difficult to precisely ascertain. Changing duty cycles and time-varying currents make determining losses tricky. One simple way to judge relative losses is to measure various devices' temperature rises. Appropriate tools here include thermal probes and, at low voltages, the perhaps more readily available human finger. At lower power, even though the percentage of loss may be as great, the latter "digital" technique is less effective. Sometimes deliberately adding a known loss to the component in question and noting changes in efficiency allows you to determine actual losses.

Ohmic losses in conductors are usually only significant at higher currents. Hidden ohmic losses include socket and connector-contact resistance and ESR in capacitors. ESR generally drops with capacitor value and rises with operating frequency. Consider the copper resistance of inductive components. You must often evaluate tradeoffs of an inductor's copper resistance versus its magnetic characteristics.

Switching losses occur when the switching device spends significant amounts of time in its linear region relative to operating frequency. At higher switching frequencies, transition times can engender substantial losses.

The design of the magnetic components also influences efficiency. Inductive-component design is well beyond the scope of this article, but some of the tradeoffs and specifications include core-material selection, wire type, winding techniques, size, operating frequency, current levels, temperature, and others. No substitute exists for access to a skilled magnetic-components specialist. Fortunately, the nonmagnetic losses previously mentioned usually dominate, allowing you to obtain good efficiencies with standard magnetic components. Thus, you usually need to employ custom magnetic components only after you have reduced other circuit losses to their lowest practical level.

## Practical circuits

To illuminate practical circuits, first reconsider the simple example of a voltage step-down regulator in **Fig 1** with a 150-μH inductor installed. Conceptually, you can think of the regulator IC as having a switch between its $V_{IN}$ and $V_{SW}$ pins. When this "switch" closes, the input voltage appears at the inductor. Current flowing through the inductor-capacitor combination builds over time. When the switch opens, current flow

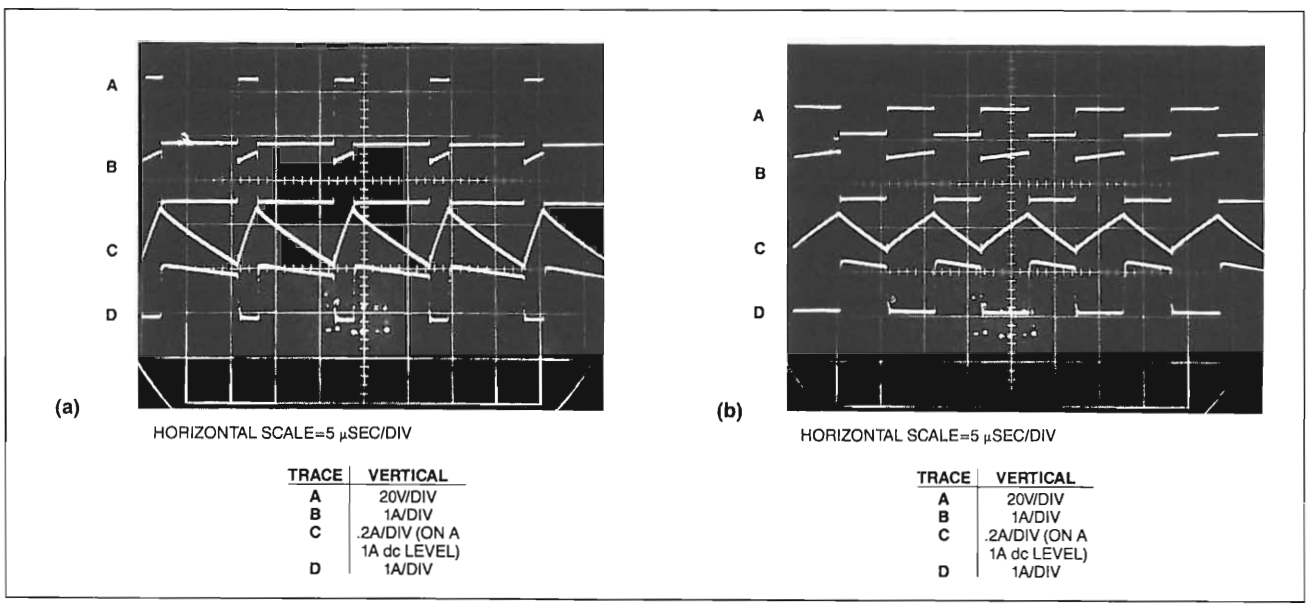



***Fig 3—In these operating waveforms for Fig 1's** circuit with a 150-μH inductor installed and $V_{IN}$=28V, trace A is the $V_{SW}$ pin's voltage and trace B is its current. Inductor current appears in trace C and diode current in trace D. The waveforms in **(a)** correspond to a 5V, 1-kΩ load while the waveforms in **(b)** show significant duty-cycle changes when the input voltage drops to 12V.*

ceases and the magnetic field around the inductor collapses.

As Faraday demonstrated, the voltage that the collapsing magnetic field induces is opposite in polarity to the originally applied voltage. As such, the inductor's left side becomes negative and the diode clamps it to ground. The capacitor's accumulated charge has no discharge path and a dc potential appears at the output; the dc potential is lower than the input voltage because the inductor limits current during the switch's on time. In this basic circuit, feedback-controlled switching action regulates the output voltage. Switch on time, and thus inductor charge time, vary to maintain the output-voltage level against changes in input voltage or output loading.

Ideally, no dissipative elements exist in this voltage step-down conversion. Thus, although the output voltage is lower than the input voltage, no energy-conversion losses occur. In practice, the circuit elements *do* have losses, of course, but step-down regulator efficiency is still higher than with inherently dissipative, voltage-divider approaches.

Components at the regulator IC's $V_C$ compensation pin control the IC's frequency compensation, stabilizing the feedback loop. You select the feedback resistors to force the voltage at the FB feedback pin to match the device's internal 2.5V reference value.

**Fig 3a** shows operating waveforms for the regulator at $V_{IN}=28V$ with a 5V, 1-kΩ load. Trace A is the $V_{SW}$ pin's voltage; trace B is its current. Inductor current appears in trace C; diode current appears in trace D. Examining the current waveforms allows you to determine the $V_{SW}$'s and diode path's contributions to the inductor's current. Note that the inductor current's waveform occurs on top of a 1A dc level. **Fig 3b** shows significant duty-cycle changes when $V_{IN}$ drops to 12V. This lower input voltage requires longer inductor-charge times to maintain the required output level.

### Dual-output step-down regulator

**Fig 4**, a logical extension of the basic step-down switching regulator, provides positive and negative outputs. The circuit is essentially identical to **Fig 1**'s basic switcher, except that it has a winding coupled to $L_1$. This floating winding's output gets rectified, filtered, and regulated to a −5V output. The negative output can use a positive voltage regulator because its floating bias allows you to assign the regulator's output terminal to ground. You can also reference its output to any voltage within the breakdown capability of the device. Hence, the secondary output *could* be +5V or, if stacked on the +15V output, +20V.

Flux pickup from $L_1$'s driven winding sets the limit for negative output power. With a 2A load at the +15V output, the −5V output can supply more than 500 mA.

You can also obtain negative outputs with a simple,

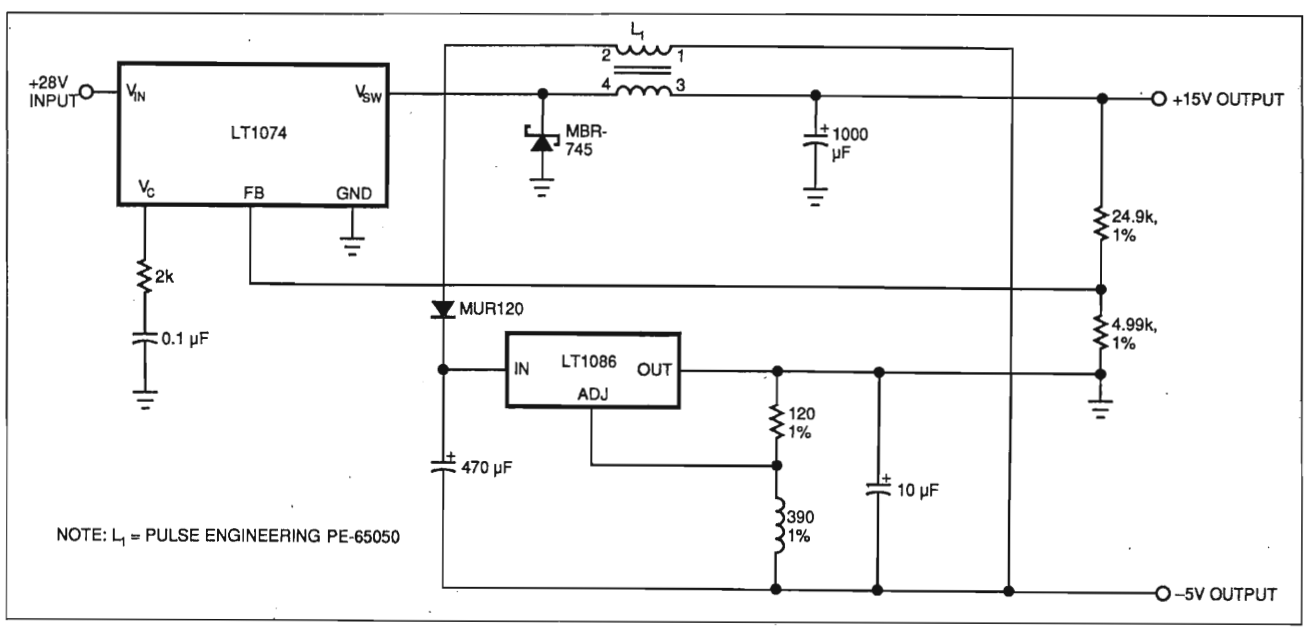



***Fig 4—Adding a coupled winding to the basic** circuit's inductor allows you to tap off a floating auxiliary output.*

*Confronting the challenge of selecting the proper inductor, engineers often simply insert an anonymous drawer dweller into an unsuspecting circuit.*

2-terminal inductor instead of a multiwinding inductor (**Fig 5**). You essentially ground the inductor and steer the catch diode's negative current to the output. $IC_2$ closes the loop by inverting and scaling the negative output to the regulator IC's feedback pin. The 1% resistors' scale factor sets output voltage; the RC network around $IC_2$ gives frequency compensation. Waveforms for this circuit are reminiscent of **Fig 1**'s, with the exception that diode current is negative.

**Fig 6**, which we call "Nelson's circuit," provides the same function as the previous circuit, but eliminates the level-shifting op amp. Circuit ground is common to input and output. Connecting the regulator IC's ground pin to the negative output accomplishes the design's level shift. The regulator IC senses feedback relative to the circuit's ground, and it drives its output so as to force its feedback pin to be 2.5V above its ground pin. The previous negative-output circuit has

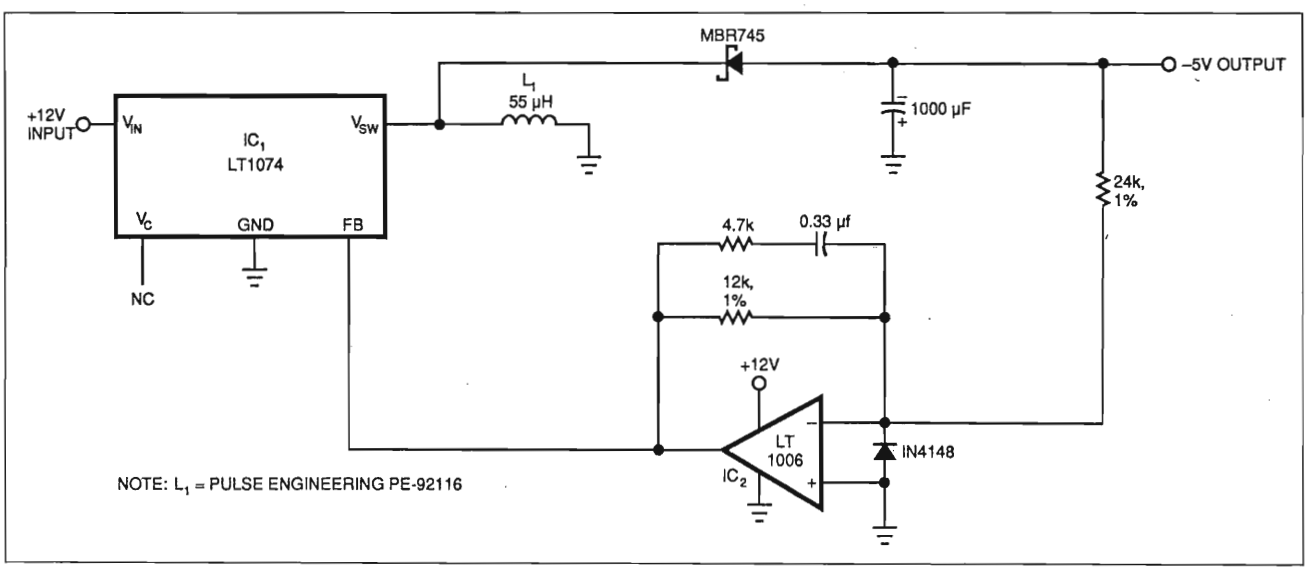



***Fig 5—You can obtain negative outputs*** *using a simple 2-terminal inductor—if you ground one end and properly orient the catch diode.*

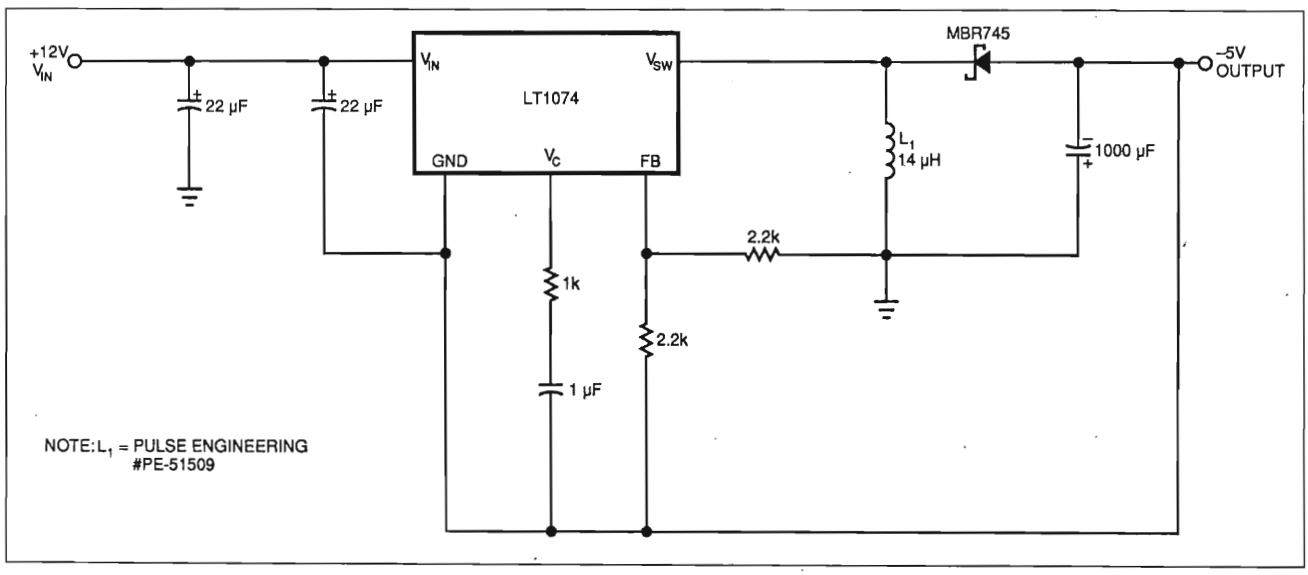



***Fig 6—This negative-output circuit*** *eliminates the level-shifting op amp. Connecting the regulator IC's ground pin to the negative output accomplishes this design's level shift.*

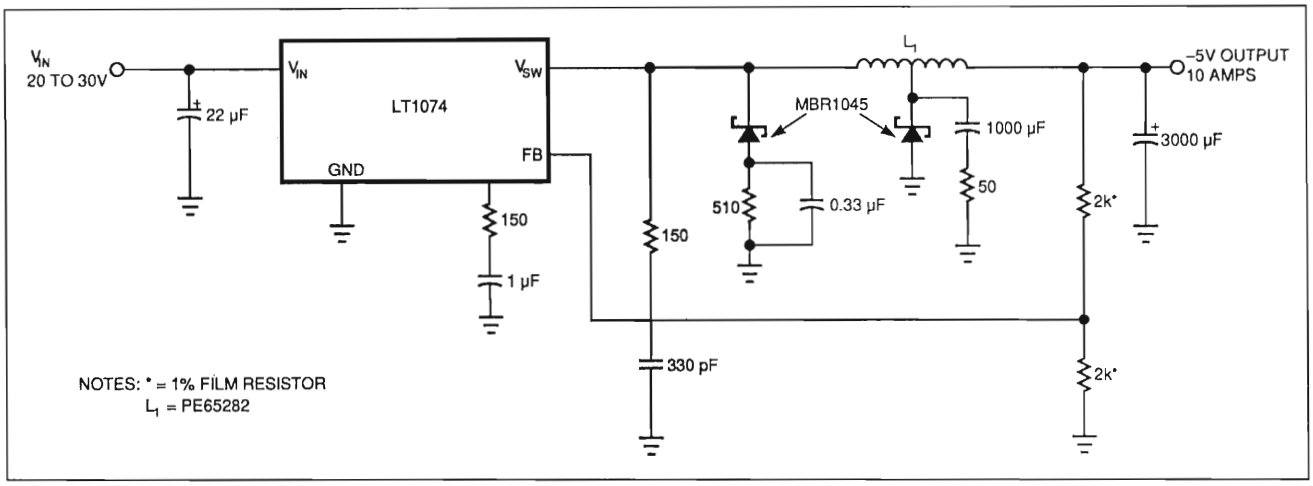



***Fig 7—Don't be fooled. $D_1$ is not a catch diode; it's part of a snubber circuit.*** *$D_2$ is the catch diode. When $D_2$ conducts, it switches out a portion of the inductor's turns, forcing the inductor's magnetic field to deliver its stored energy through an effectively smaller inductance and thereby increasing the circuit's output-current capability.*

two advantages, compared with Nelson's. First, the package can directly contact a grounded heat sink. Second, the IC's control pins are ground referred.

Note that the inductor values in both negative-output designs are notably lower than in the positive-output designs. The reduced loop-phase margin of these circuits demands the lower-value inductors. Higher inductance values, while preferable for limiting peak current, will make the loop unstable or even cause it to oscillate.

## Current-boosted step-down regulator

**Fig 7** shows a novel way to obtain significantly higher output currents—by utilizing efficient energy storage in the regulator IC's output inductor. The technique prolongs current flow from the inductor and thereby effectively increases the inductor's duty cycle, compared with the standard step-down switching regulator's, allowing more energy storage in the inductor. But beware, the increased output current comes at the cost of higher output-voltage ripple.

The key to the design is its tapped inductor. With it, the circuit has current gain. If N is the ratio of switch-side turns to output-side turns, current delivered to the output will be N+1 times higher during the $V_{SW}$'s off time as compared to the current flowing during its on time.

**Fig 8** shows the circuit's operating waveforms. Its operating characteristics are initially similar to that of the step-down switching regulator in **Fig 1**. During $V_{SW}$'s on time (trace A), the regulator IC applies the input voltage to one end of the tapped inductor. Because inductor current (trace F) is still present, current from the $V_{SW}$ pin (trace B) ramps up almost instantaneously, then slows as the core stores energy. The current proceeds into the inductor (trace D) and finally to the load.

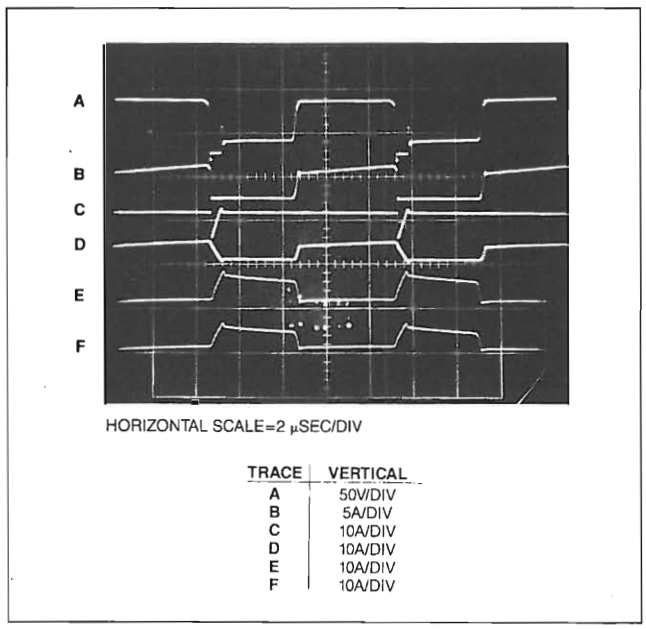



***Fig 8—In these operating waveforms for Fig 12's circuit, trace A is $V_{SW}$'s voltage, trace B is its output current, trace C is the snubber circuit's $D_1$ current, trace D is the inductor's input current (minus the snubber circuit's contribution), trace E is the current through $D_2$, and trace F is the output current.***

# SIGNALS & NOISE

## Reader questions "empirical" approach

I normally enjoy reading Jim Williams' articles because he has a real creative ability to develop innovative applications for his company's products. The latest one, however, "Basic principles and ingenious cir-

cuits yield stout switchers" (EDN, January 18, 1990, pg 151), really caused me some concern. Jim states at the beginning of this article that switching regulators may be designed by following some basic principles, and then he says, "Because of the overwhelming level of difficulty associated with magnetic components ...an empirical approach is often the best way to select inductors."

Granting that most designers, myself included, may not be as familiar with Ampere's and Faraday's laws as we are with Ohm's law, magnetics is not that much of a black art. When I read Jim's suggestion that you may select an appropriate inductor by feeling its weight and measuring its dc resistance, I don't know whether to laugh or cry. If Jim is putting us on, he is a very funny writer, but it's a sad day for engineering if readers get the impression that this is an acceptable method for designing reliable switching regulators.

Specifying an inductor is not a trivial task but neither is it "overwhelmingly difficult." The equations are simple and readily available in probably hundreds of sources ranging from textbooks to manufacturer's application guides. I'm sorry to criticize, but to ignore all this in an article about "basic principles" does a disservice to our profession.

*Robert A Mammano*
*Vice President*
*Advanced Technology*
*Unitrode IC Corp*
*Santa Ana, CA*

*(The author's reply: I appreciate Robert Mammano's taking the time to write. I hope my reply will clear up any confusion.*

*I think it's important to examine the complete content and precise wording of the article, so I refer you to reading the text surrounding the suggestions Robert refers to. (See the entire section under the subhead, "The invasion of the drawer dwellers," pg 152.) The particular sentences that sharpen the focus of the context read: "An alternate inductor-selection method exists—one favored by those who have no inductor kit, time, or adequate instruments. You can use this alternate method when faced with an immediate deadline and a drawer full of inductors of unknown or questionable lineage." "Although this method's theoretical underpinning is perhaps questionable, its seemingly limitless popularity compels coverage." "Inductors passing both stages of the test have an excellent chance (75%—based on a sample of randomly selected inductors) of performing adequately in*

*a prototype circuit."*

*I think my suggestions in their original and complete form restore balance to their presentation. In particular, the majority of switching-regulator users have little experience in the area. More significantly, many do not desire to develop a substantial expertise. This observation doesn't make them poor or irresponsible engineers, but simply reflects their priorities. What they do want are concepts directly applicable to construction of working circuits with readily available parts.*

*The area of switching regulators is the most difficult application area I have worked in. To a large extent, the difficulty lies in the subject matter. Switchers are hard. Because of this, high levels of user trepidation are common. If the goal is to get designers to utilize switching technology, one way to begin is to make them feel comfortable about it. The section Robert questions was written with tongue-in-cheek, but not too firmly planted there! Fully 90% of switcher-customer inquiries I handle involve magnetic-selection difficulties. These engineers are often anxious to prototype a feasible solution to their problems. I want to ensure that their initial efforts are encouraging, not disheartening. It's much easier to work with and get enthusiastic about a functional circuit than one that doesn't work.*

*When writing technical material, I try to appeal to a broad section of the engineering population. The interest level and expertise spectrum of the audience varies considerably. A cardinal error is to assume that the most interested people possess a high degree of familiarity with the subject matter. This assumption is simply not true. As such, it is my responsibility as a writer to try to communicate with both aficionados and newcomers. I can't say I'm always successful at doing this, but it's the goal.*

*I'm sorry Robert Mammano didn't find this balance in my presentation, and I welcome his suggestion on how to achieve it.)*

# Thermal charging circuits safely boost NiCd batteries

*Charging methods based on thermal sensing are a simple and effective way to quickly charge NiCd batteries. As long as the circuit compensates for the battery's thermal time constant, thermal charging techniques won't harm batteries.*

Jim Williams, *Linear Technology Corp*

Fast charging of NiCd batteries is attractive in many applications. However, a short charge time requires high current, and battery heating is a potential difficulty with high-current charging. Excessive internal heating degrades the battery and can cause gas to vent to the outside atmosphere. By monitoring cell temperature and tapering the charge accordingly, thermal-charging methods let you charge batteries without abusing them.

Unlike thermal charging methods, techniques that sense only voltage or elapsed time aren't desirable for fast charging (**Ref 1**). Fast-charge schemes that monitor cell voltage during charging are risky, because the cell's voltage doesn't necessarily indicate the battery's charge state. Also, the battery's charge-voltage relationship may vary with the age and temperature of the battery. Open-loop charging methods—for instance, those that apply high charge currents for a fixed time period—don't account for the battery's charge state or for shifts in battery characteristics over life and temperature.

The temperature response of a battery during charging is quite predictable. A discharged battery converts current to stored electrochemical energy without producing much heat. However, when the battery arrives at full charge, the cell is saturated and can't hold any more energy. As a result, the battery now produces heat, and its temperature increases.

To detect the point of temperature rise, you can measure the difference between the cell's surface temperature and the ambient temperature. An absolute temperature measurement is undesirable because cell temperature is the sum of excess charging energy and ambient temperature. Also, the circuit must measure the ambient and battery temperatures in phase. The thermal time constant of a battery pack can easily exceed one hour. If you compare the slowly changing battery temperature to a quickly changing ambient temperature, poor charging characteristics can result.

Consider the case of a portable computer that's been sitting in a locked automobile on a summer day where passenger-compartment temperatures can exceed 120°F. Once inside an air-conditioned environment, the computer's ambient-temperature sensor quickly settles to 73°F. However, the battery-pack temperature lingers at 120°F, exhibiting a 1-hour thermal time constant. Because the charging circuit senses high temperature, it acts as if the battery has just received a full charge, and it delivers no charging current to the battery. The opposite effect occurs if the computer sits in a car parked overnight in Minneapolis in January.

You can avoid such problems by using charging methods that match the time constants of the information from the battery and ambient thermocouples. In

*A short charge time requires high current, and high-current charging causes battery heating.*

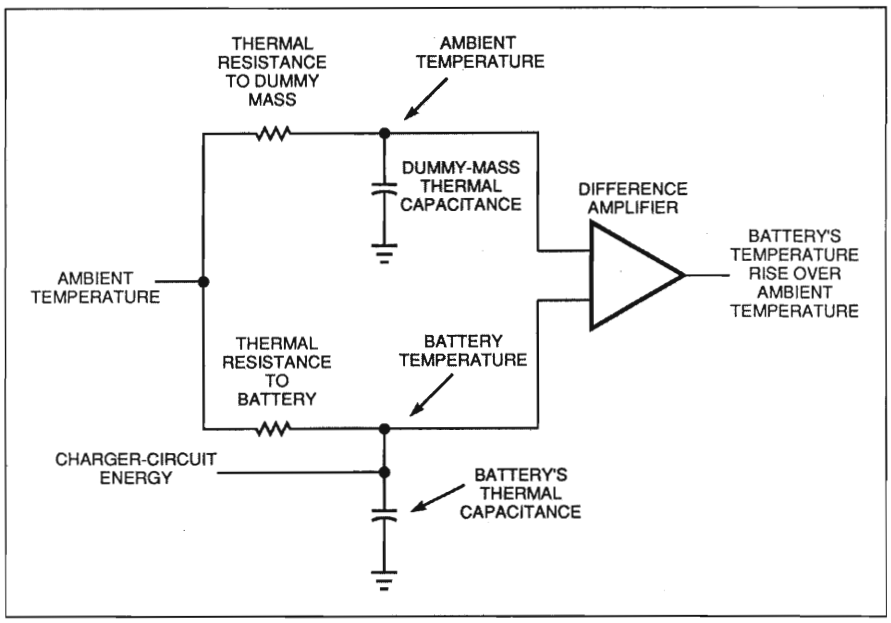



***Fig 1—The most effective thermal charging systems*** *measure the temperature difference between the battery pack and the ambient atmosphere and match the thermal time constants of each amplifier input.*

other words, the circuit must add lag to the ambient-temperature information so that its time constant matches that of the battery. **Fig 1** illustrates a circuit model in which the resistors represent thermal resistance, and the capacitors correspond to thermal capacitance. Ambient temperature appears as a common-mode term, but the charging circuit's energy affects only the battery. To present in-phase information to the difference amplifier, the ambient and battery temperatures don't require the same individual RC values; only the RC products must be the same. You can match the time constant of a massive battery pack that has a low thermal resistance to a well-insulated (high thermal resistance) small thermal mass.

## Measure the thermal effects

Two similar circuits are practical implementations of **Fig 1**'s scheme. **Fig 2a** and **b** are identical except for the location of the battery in the circuit. **Fig 2b**'s circuit charges batteries by connecting them to ground. The common-emitter output necessitates the exchange of amplifier input assignments, but the circuit's operation is identical to **Fig 2a**.

Two independent thermocouples sense cell and ambient temperatures. The LT1006 amplifier operates at the low voltage levels necessary to sense the microvolt-level thermocouple signals. The battery thermocouple mounts directly to one of the cells in the pack. The thermally insulated ambient thermocouple can mount to a mass such as the frame of the equipment that

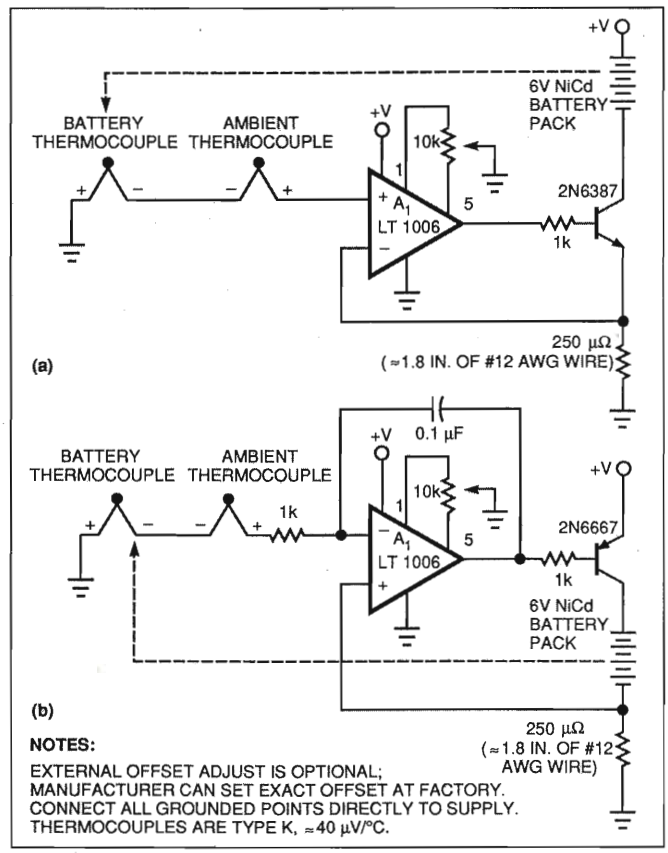



***Fig 2—Two simple circuits implement thermal charging.*** *Depending on your charger-design preferences, you can connect the battery between the supply and transistor collector* ***(a)*** *or refer the battery to ground* ***(b)***.

houses the battery pack and charger. If a discharged battery pack connects to **Fig 2a**'s transistor collector, the battery and ambient thermocouples will read identical temperatures. Under this condition, the phases of the sensors match, their outputs cancel, and $A_1$'s input is 0V.

The 10-kΩ offset adjustment introduces enough input offset for $A_1$ to swing positively, thereby turning on the transistor. If the manufacturer presets the amplifier's offset at the desired value, you can eliminate the potentiometer. Current flows from the supply through the battery pack and to ground through the 250-μΩ shunt (see **box**, "Create low-resistance shunts with wire"). The low-impedance shunt minimizes losses, cost, and complexity. The voltage across the shunt rises to about 625 μV—the amount of the potentiometer-induced offset—and the amplifier controls the flow of about 2.5A through the battery pack. As the battery charges, it heats, and the battery-mounted thermocouple picks up this heat. The temperature difference between the two thermocouples determines the voltage level at the amplifier's positive input.

As the battery temperature rises, this small, negative input voltage increases (1°C difference between the thermocouples equals 40 μV). The amplifier gradually reduces the current through the battery to maintain balanced inputs. **Fig 3** shows the effect of this current reduction. The battery charges at a high rate until heating occurs. As the temperature rises, the circuit tapers the charge. The component values in **Fig 2** limit the difference between the battery's surface and ambient temperatures to about 15°C.

## Create low-resistance shunts with wire

A simple, inexpensive way to construct low-resistance shunts is to use a small length of wire (**Fig Aa**) or a printed-circuit trace (**Fig Ab**). Either type of shunt should have separate Kelvin-style sense connections so that the high current doesn't corrupt readings.

If you construct the shunt with wire, the type and length of the wire determine the shunt resistance, which will vary with desired charging characteristics. **Table 1** tabulates resistance vs length characteristics for various wire sizes.

Printed-circuit traces can be precise low-resistance shunts, but their resistance depends on the type of pc-board material and the width and thickness of the trace. Consult with your pc-board manufacturer to determine the material's resistivity, with which you can calculate the area of the trace for your desired resistance. Ultimately, you'll need to measure the resistance of the actual trace.

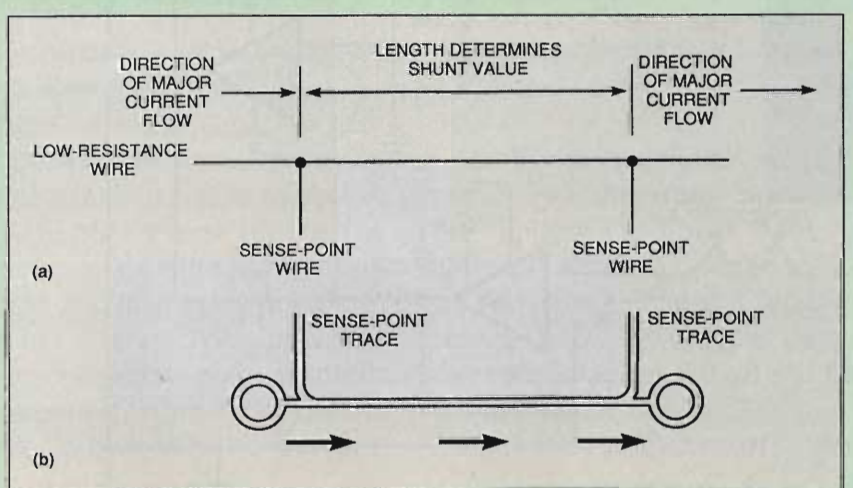



***Fig A—Low-resistance shunts** are easy to construct using either low-resistance wire **(a)** or a printed-circuit trace **(b)**.*

**Table 1—Wire-gauge resistances**

| WIRE GAUGE | μΩ/INCH |
|---|---|
| 10 | 83 |
| 11 | 100 |
| 12 | 130 |
| 13 | 160 |
| 14 | 210 |
| 15 | 265 |
| 16 | 335 |
| 17 | 421 |
| 18 | 530 |
| 19 | 670 |
| 20 | 890 |
| 21 | 1000 |
| 22 | 1300 |
| 23 | 1700 |
| 24 | 2100 |
| 25 | 2700 |

*If a battery soaks in an extreme environment, a poorly designed charging circuit may act as if the battery is completely charged or discharged when it's not.*

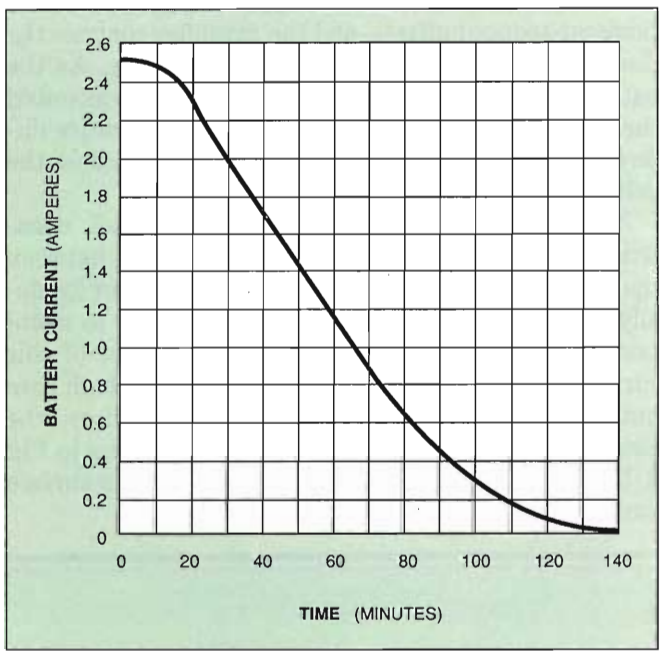



***Fig 3—To maintain balanced inputs,*** *the charging-circuit amplifiers gradually reduce the current through the battery as it charges and heats.*

For accurate results, the small shunt's sense voltage requires a ground with very low impedance. A high-quality ground ensures that the large current flow through the transistor doesn't combine with ground-return impedances and create errors. To avoid this problem in practice, you should connect all returns to the supply's common terminal. Similarly, you must design your circuit so that it's not susceptible to parasitic thermocouple effects (**Ref 2**).

Both of these circuits force the transistor to dissipate some power, particularly in the middle of the charge curve. The heat produced may be a problem in a very small enclosure. **Fig 4**'s circuit eliminates this problem. This design is similar to the others, except that $A_2$'s duty-cycle-modulator configuration separates $A_1$ from the output transistor. The transistor $Q_1$, in this case a power FET, operates in a switched mode, and it delivers duty-cycle-modulated current pulses to the battery pack. $R_7$ and $C_4$ filter the switching waveform. $R_6$ and $R_7$ ensure that $A_1$'s inverting- and noninverting-input source impedances balance. $C_2$ sets the circuit's gain roll-off.

**Fig 4**'s design relies on the source impedance of the

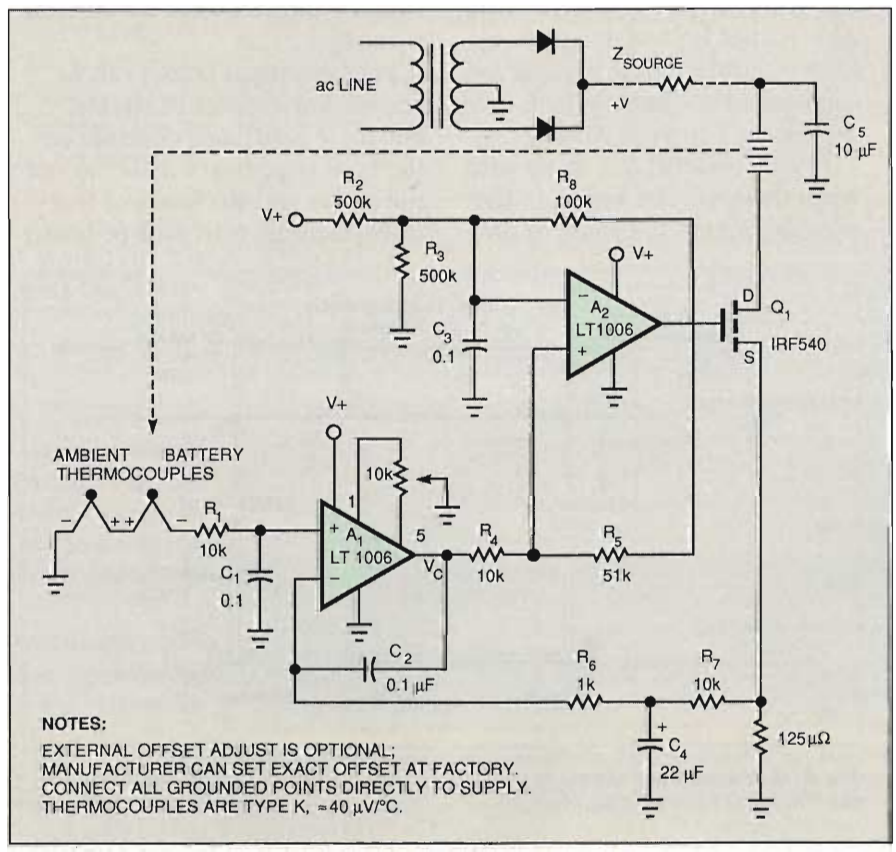



***Fig 4—A switched-mode thermal charger*** *allows you to charge NiCd batteries in small enclosures. This design relies on the source impedance of the wall transformer to limit the current through $Q_1$ and the battery pack.*

*One way to charge batteries without abusing them is to measure cell temperature and taper the charge accordingly.*

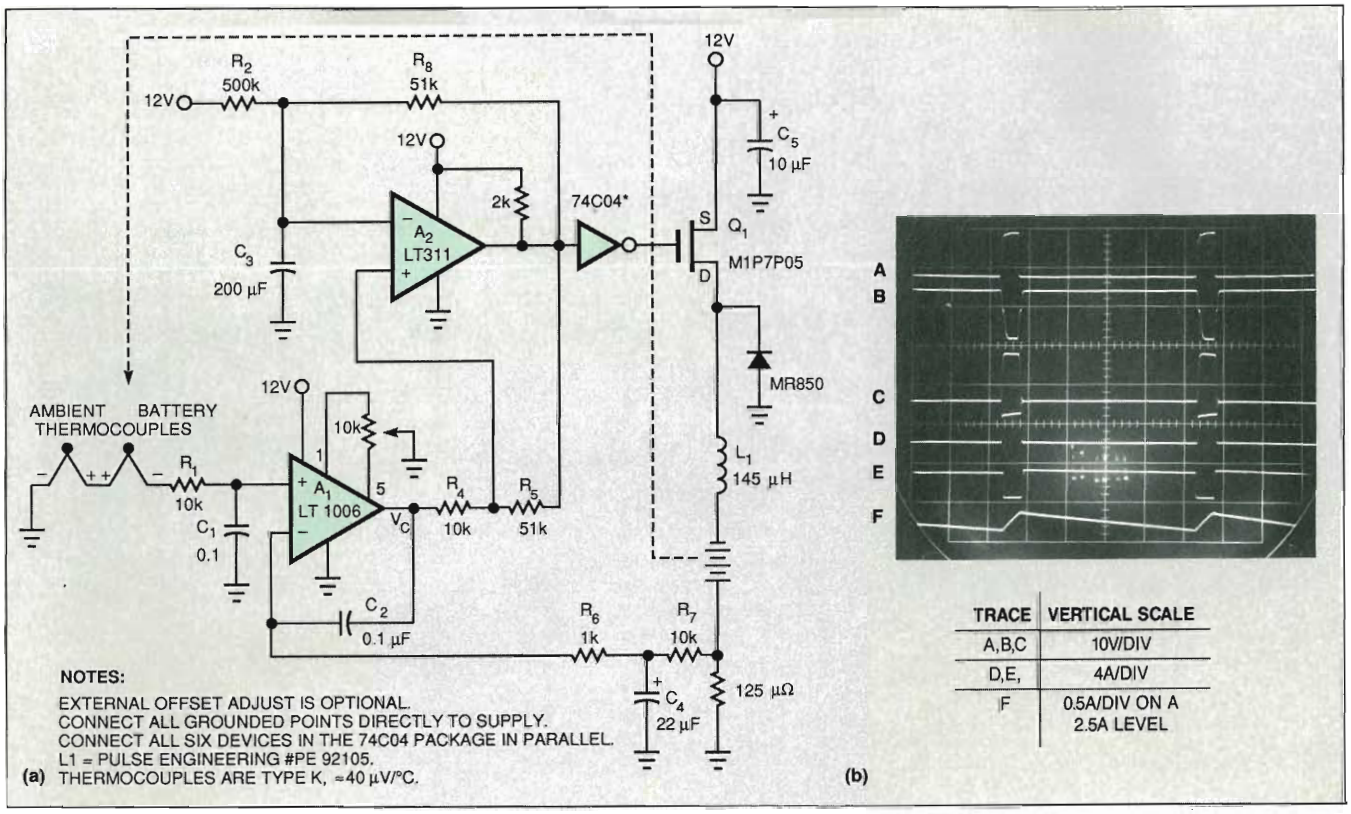



***Fig 5—This switched-mode design*** *works if your supply voltage* ***(a)*** *has a low impedance. Waveforms* ***(b)*** *illustrate various points in the circuit.*

wall transformer to limit the current through $Q_1$ and the battery pack. The specifications of the transformer set the current limit. The circuit in **Fig 5a** is useful when the charging source has a low impedance. In this figure, the circuit's output configuration is a simple, step-down switching regulator. The 74C04 gates provide phase inversion and drive current for $Q_1$, a P-channel MOSFET.

The waveforms in **Fig 5b** help you verify the circuit's operation. Trace A shows $A_2$'s output, and Trace B shows $Q_1$'s gate drive. Traces C and D display $Q_1$'s drain voltage and drain current, respectively. Trace E is the MR850 catch diode's current. Trace F is $L_1$'s current. $L_1$ smooths current flow, resulting in low-loss operation. EDN

## References


1. Swager, Anne Watson, "Team batteries with control circuits to achieve fast charging," *EDN*, December 7, 1989, pg 180.
2. Williams, Jim, "Application considerations and circuits for a new chopper-stabilized op amp," Application Note 9, Linear Technology Corp, March, 1985.


## Acknowledgment


*The author gratefully acknowledges William Cho for his contributions toward the completion of this article.*


## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

EDN DESIGNERS' GUIDE TO

bridge circuits
Part 1

# Good bridge-circuit design satisfies gain and balance criteria

*Bridge circuits are among the most elemental and powerful electrical tools. They are used in measurement, switching, oscillator, and transducer applications. This guide will help you choose the most appropriate circuit for your application. Part 1 of this 2-part series discusses dc and pulsed methods for bridge-circuit signal conditioning. Part 2 will discuss ac signal-conditioning methods.*

Jim Williams, *Linear Technology Corp*

Bridge circuits are the electrical analog of the mechanical beam balance as well as the predecessor of all electrical differential techniques. The basic resistor bridge (**Fig 1**) is usually credited to Charles Wheatstone, although S H Christie—who demonstrated this circuit in 1833—almost certainly preceded him. Wheatstone apparently had a better public relations agency, namely himself.

In the resistor bridge, if all resistor values are equal, the differential voltage is zero. The excitation voltage does not alter this relationship because it effects both sides of the bridge equally. When the bridge is unbalanced, the excitation's magnitude sets the output sensitivity. With a single variable resistor, the bridge's output is nonlinear. Two variable arms (such as $R_C$ and $R_B$) also produce a nonlinear output, although the sensitivity doubles. Linear outputs are made possible by complementary resistance swings in one or both sides of the bridge.

The Wheatstone bridge has attracted a great deal of attention. Designers have applied an almost uncountable number of tricks and techniques to enhance the linearity, sensitivity, and stability of the basic configuration. Transducer manufacturers are especially expert at adapting the bridge to their needs (see **box,** "Strain-gauge bridges"). Carefully matching the transducer's mechanical characteristics to the bridge's electrical response can provide a trimmed, calibrated output. Similarly, circuit designers have altered performance by adding amplifiers to the bridge, excitation source, or both.

TEST & MEASUREMENT

A primary concern with bridge circuits is accurately determining the differential output voltage. In bridges operating at the null point, the absolute scale factor of the readout device is normally less important than its sensitivity and zero-point stability. Bridge amplifiers extract the bridge's differential

*Designers have given a great deal of attention to the Wheatstone bridge. A variety of tricks and techniques enhance its basic linearity, sensitivity, and stability.*

output from its common-mode level. An amplifier's ability to reject a common-mode signal is critical. A typical strain-gauge transducer operating from a 10V source produces only 30 mV of signal riding on 5V of common-mode level. A 12-bit resolution of this signal has an LSB of only 7.3 μV, which is almost 120 dB below the common-mode signal. Other significant error terms include offset voltage (including its shift with temperature and time), bias current, and gain stability.

Instrumentation amplifiers make good bridge amplifiers. These devices are usually the first choice for bridge measurement, and their performance is adequate for most applications. In general, instrumentation amplifiers feature fully differential inputs and internally determined stable gain. The absence of a feedback network results in inputs that are essentially passive, and no significant bridge loading occurs. **Table 1** lists performance data for some specific instrumentation amplifiers. **Table 2** summarizes some options for dc-bridge signal conditioning by presenting various approaches and their pertinent characteristics. The constraints, freedoms, and performance requirements of the particular application define the best approach.

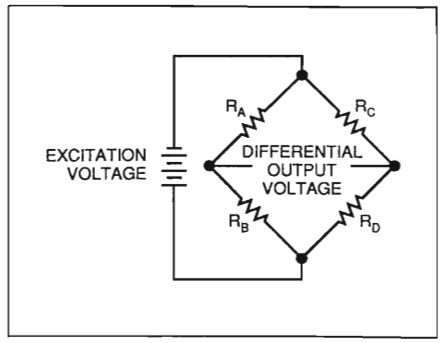



***Fig 1—Usually credited to Charles Wheatstone,** the basic resistor bridge is widely used in measurement applications.*

## DC bridge-circuit applications

**Fig 2** shows a typical bridge application and details signal conditioning for a 350Ω transducer bridge. The specified strain-gauge pressure transducer produces a 3-mV output for each volt of bridge excitation. The LT1021 reference, buffered by $IC_{1A}$ and $IC_2$, drives the bridge. This potential also supplies the circuit's ratio output, permitting ratiometric operation of a monitoring A/D converter. Instrumentation amplifier $IC_3$ extracts the bridge's differential output at a gain of 100; $IC_{1B}$ supplies additional trimmed gain.

You can adjust this configuration for a precise 10V output at full-scale pressure. The trimming adjustment at the bridge sets the zero-pressure scale point. The RC combination at the input of $IC_{1B}$ filters noise and determines the system's lowpass cutoff frequency. Noise may originate as residual RF line pickup or transducer responses to pressure variations. In cases where noise is relatively high, you may want to filter ahead of $IC_3$, thereby preventing any possible signal infidelity caused by nonlinear $IC_3$ operation. Saturation, slew-rate components, and rectification effects can produce such undesirable outputs.

When filtering ahead of the circuit's gain blocks, remember to allow for the effects of bias-current-induced errors caused by the filter's series resistance. This resistance can be a significant consideration because large-value capacitors, particularly electrolytic types, are not practical. If bias-current-induced errors rise to appreciable levels, you may need FET or MOS input amplifiers.

To trim this circuit, apply zero pressure to the transducer and adjust the 10-kΩ potentiometer until the output just comes off 0V. Next, apply full-scale pressure and trim the 1-kΩ adjustment. Repeat this procedure until both points are fixed.

**Fig 3** shows a way to reduce errors caused by the bridge's common-mode output voltage. $IC_1$ biases $Q_1$ to provide a servo action that forces the bridge's left mid-

## Table 1—Instrumentation-amplifier performance data

| Parameter | LTC1100 | LT1101 | LT1102 | LTC1043 (Using LTC1050 amplifier) |
|---|---|---|---|---|
| Offset | 10 μV | 160 μV | 500 μV | 0.5 μV |
| Offset drift | 100 nV/°C | 2 μV/°C | 2.5 μV/°C | 50 nV/°C |
| Bias current | 50 pA | 8 nA | 50 pA | 10 pA |
| Noise (0.1 to 10 Hz) | 2 μV p-p | 0.9 μV | 2.8 μV | 1.6 μA |
| Gain | 100 | 10,100 | 10,100 | Resistor programmable |
| Gain error | 0.03% | 0.03% | 0.05% | Resistor limited, 0.001% possible |
| Gain drift | 4 ppm/°C | 4 ppm/°C | 5 ppm/°C | Resistor limited, <1 ppm/°C possible |
| Gain nonlinearity | 8 ppm | 8 ppm | 10 ppm | Resistor limited, 1 ppm possible |
| CMRR | 104 dB | 100 dB | 100 dB | 160 dB |
| Power supply | Single or dual, 16V max | Single or dual, 44V max | Dual, 44V max | Single, dual 18V max |
| Supply current | 2.2 mA | 105 μA | 5 mA | 2 mA |
| Slew rate | 1.5 V/μsec | 0.07 V/μs | 25 V/μs | 1 mV/ms |
| Bandwidth | 8 kHz | 33 kHz | 220 kHz | 10 Hz |

## Strain-gauge bridges

In 1856, Lord Kelvin discovered that applying strain to a wire shifted its resistance. This effect is repeatable and is the basis for electrical-output strain measurement. Early devices were wires suspended between two insulated points. The mechanically measured force biased the wire, thus changing its resistance. Modern devices utilize foil-based designs (**Fig Aa**) in which the conductive material is deposited on an insulated carrier. Physically, these designs take many forms and allow a variety of applications. The gauges are usually configured in a bridge circuit and mounted on a beam, thus forming a transducer.

A useful transducer must be trimmed to a zero reference point, adjusted for gain, and compensated for temperature sensitivity. **Fig Ab** shows a typical arrangement. Trimming adjustments set the zero point and the gain. The gain trims include modulus gauges to compensate for the temperature sensitivity of the beam material. Arranging these trims and completing the mechanical assembly involves a fair amount of artistry and is best left to specialists.

Semiconductor-based strain-gauge transducers utilize resistive shift in semiconducting materials. These monolithic devices are smaller in size and considerably less expensive than manually assembled foil-based strain gauges and have more than 10 times the sensitivity. However, semiconductor-based transducers are more sensitive to temperature and other effects and suit less demanding applications. Although a semiconductor-based transducer's impedance levels are about 10 times higher than foil-based designs, the devices have electrically similar bridge configurations.

**Fig Ac** shows the construction of a semiconductor-based device that uses a piezoresistive effect to provide strain-gauge action. The diaphragm is anisotropically etched from a silicon substrate. The piezoresistive element is a single, 4-terminal strain gauge. It is located at the midpoint of the edge of the square diaphragm at an angle of 45°. This orientation maximizes the device's sensitivity to shear stress.

Excitation current passes longitudinally through the resistor (pins 1 and 3), and the pressure that stresses the diaphragm is applied at a right angle to the current flow. The stress establishes a transverse electric field in the resistor. Pins 2 and 4, which are the taps located at the midpoint of the resistor, sense this field as an output voltage. In a sense, the single-element, shear-stress strain gauge is the mechanical analog of a Hall-effect device.

The piezoresistive pressure transducer presents several advantages over the Wheatstone bridge configuration: improved linearity and a more consistent offset.

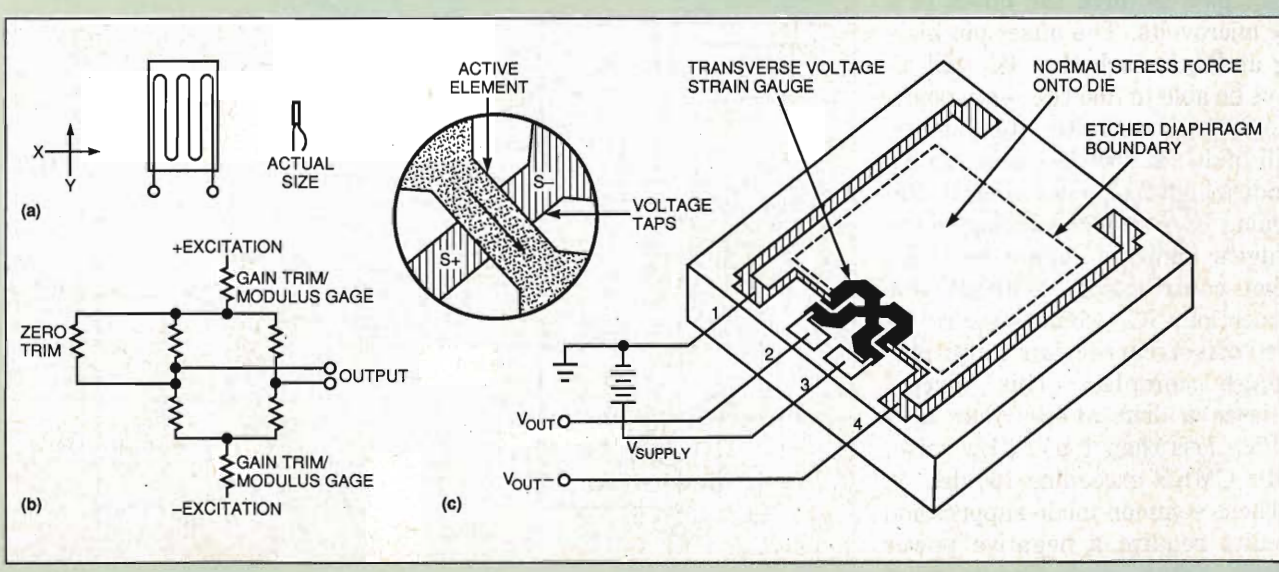



***Fig A—Modern strain gauges utilize** foil-based designs **(a)**; a simplified schematic shows trimming adjustments to set the zero point and the gain **(b)**. This semiconductor-based device **(c)** uses a piezoresistive effect to provide strain-gauge action.*

point to zero under all operating conditions. The 350Ω resistor ensures that $IC_1$ will find a stable operating point with 10V of drive delivered to the bridge. This arrangement lets $IC_2$ take a single-ended measurement, thus eliminating all common-mode-voltage errors. The approach works well and is often a good choice for high-precision work. The amplifiers in this example, which are CMOS chopper-stabilized units, essentially eliminate offset drift with time and temperature. Compared with an instrumentation-amplifier bridge circuit, this circuit is more complex and requires a negative supply.

**Fig 4** is similar to **Fig 3**, except that it uses low-noise bipolar amplifiers. This circuit trades slightly higher dc offset drift for lower noise and is a good candidate for stable resolution of small, slowly varying signals.

**Fig 5** employs chopper-stabilized $IC_1$ to reduce **Fig 4**'s already small offset error. $IC_1$ measures the dc error at $IC_2$'s inputs and biases $IC_1$'s offset pins to force the offset to a few microvolts. The offset-pin biasing at $IC_2$ is such that $IC_1$ will always be able to find the servo point. The 0.01-μF capacitor rolls off the gain of $IC_1$ at low frequencies; $IC_2$ handles high-frequency signals. Returning $IC_2$'s feedback string to the bridge's midpoint eliminates $IC_4$'s offset contribution. Without this connection, $IC_4$ would require its own offset-correction loop. Although complex, this circuit achieves a drift of less than 0.05 μV/°C, less than 1 nV/$\sqrt{\text{Hz}}$ noise, and a CMRR exceeding 160 dB.

These common-mode suppression circuits require a negative power supply. Often, such circuits must function in systems where only a positive rail is available. **Fig 6**

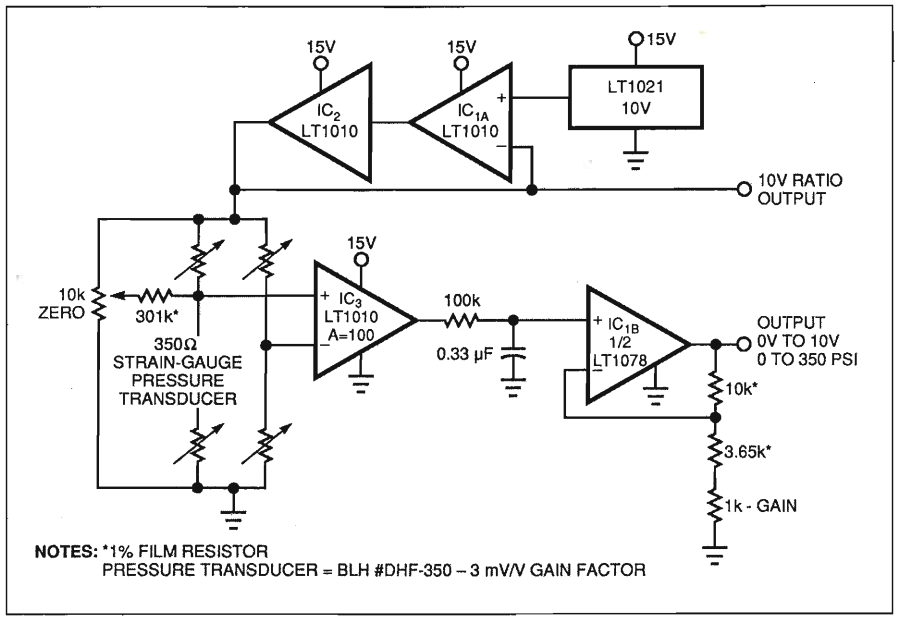



***Fig 2—This typical bridge application*** *uses an instrumentation amplifier, a voltage reference, and buffer amplifiers to provide signal conditioning for a 350Ω transducer.*

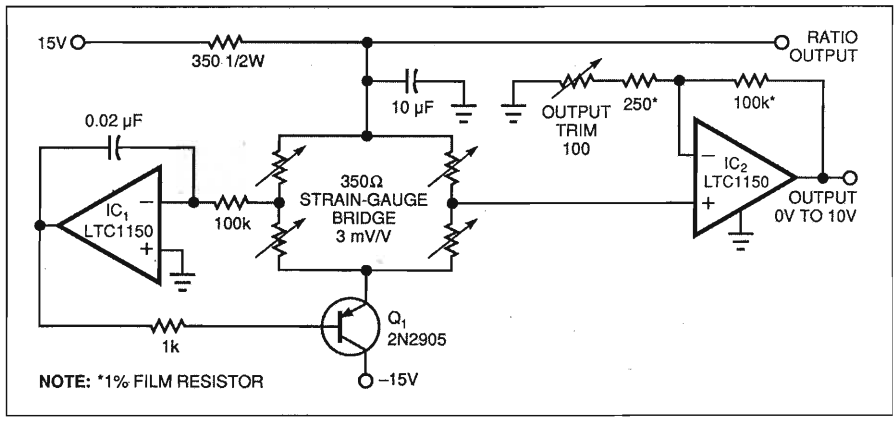



***Fig 3—Servo controlling the bridge drive*** *reduces errors caused by the bridge's common-mode output voltage.*

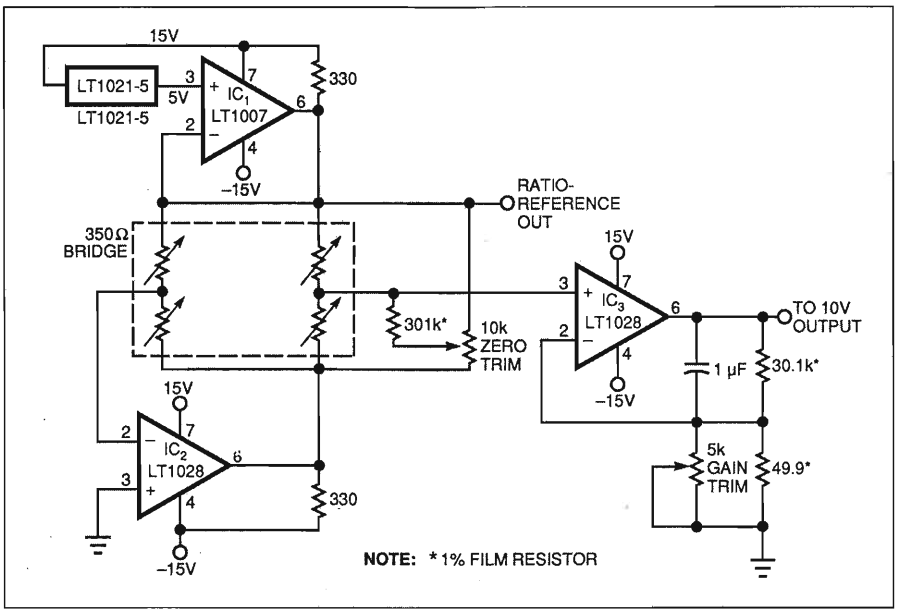
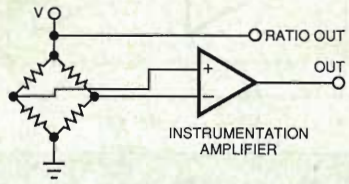
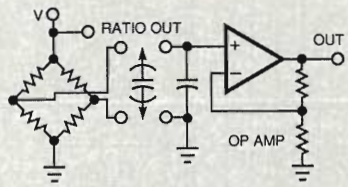
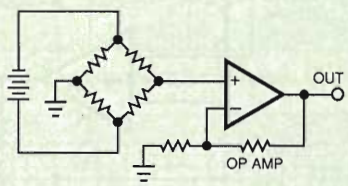
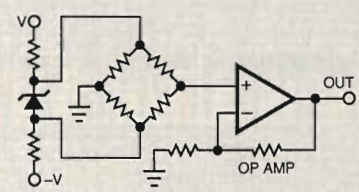
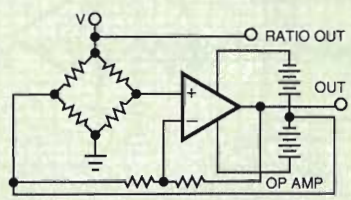
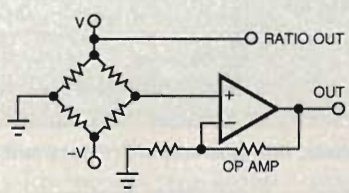
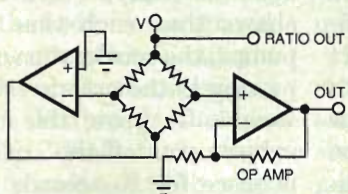



***Fig 4—Using low-noise bipolar amplifiers,*** *this circuit trades dc offset drift for lower noise and is a good candidate for resolving small, slowly varying signals.*

## Table 2—Bridge signal-conditioning methods

| Configuration | Advantages | Disadvantages |
|---|---|---|
|  | Best general choice. Simple, straightforward. CMRR typically >110 dB, drift 0.05-2 μV/°C, gain accuracy 0.03%, gain drift 4 ppm/°C, noise 10nV/√Hz–1.5 μV for chopper stabilized types. Direct ratiometric output. | CMRR, drift, and gain stability may not be adequate in highest precision applications. May require second stage to trim gain. |
|  | CMRR>120 dB, drift 0.05 μV/°C. Gain accuracy 0.001% possible. Gain drift 1 ppm with appropriate resistors. Noise 10nV/√Hz–1.5 μV for chopper stabilized types. Direct ratiometric output. Simple gain trim. Flying capacitor commutation provides lowpass filtering. Good choice for very high performance—monolithic versions (LTC1043) available. | Multipackage—moderately complex. Limited bandwidth. Requires feedback resistors to set gain. |
|  | CMRR>160 dB, drift 0.05-0.25 μV/°C, gain accuracy 0.001% possible, gain drift 1 ppm/°C, with appropriate resistors plus floating supply error, simple gain trim, noise 1nV/√Hz possible. | Requires floating supply. No direct ratiometric output. Floating supply drift is a gain term. Requires feedback resistors to set gain. |
|  | CMRR>140 dB, drift 0.05-0.25 μV/°C, gain accuracy 0.001% possible, gain drift 1 ppm/°C, with appropriate resistors plus floating supply error, simple gain trim, noise 1nV/√Hz possible. | No direct ratiometric output. Zener supply is a gain and offset term error generator. Requires feedback resistors to set gain. Low-impedance bridges require substantial current from shunt regulator or circuitry that simulates it. Usually poor choice if precision is required. |
|  | CMRR>160 dB, drift 0.05-0.25 μV/°C, gain accuracy 0.001% possible, gain drift 1 ppm/°C with appropriate resistors, simple gain trim, ratiometric output, noise 1nV/√Hz possible. | Requires precision analog-level shift, usually with isolation amplifier. Requires feedback resistors to set gain. |
|  | CMRR≈120-140 dB, drift 0.05-0.25 μV/°C, gain accuracy 0.001% possible, gain drift 1 ppm/°C with appropriate resistors, simple gain trim, direct ratiometric output, noise 1nV/√Hz possible. | Requires tracking supplies. Assumes high degree of bridge symmetry to achieve best CMRR. Requires feedback resistors to set gain. |
|  | CMRR 160 dB, drift 0.05-0.25 μV/°C, gain accuracy 0.001% possible, gain drift 1 ppm/°C, simple gain trim, direct ratiometric output, noise 1nV/√Hz possible. | Practical realization requires two amplifiers plus various discrete components. Negative supply necessary. |

*Bridge-output amplifiers can extract the bridge's differential output from its common-mode level.*

shows one way to achieve this goal. $IC_1$ biases the LT1054 positive-to-negative converter. The LTC1054's output pulls the bridge's output negative, which causes $IC_1$'s input to balance at 0V. This local loop lets a single-ended amplifier ($IC_2$) extract the bridge's output signal. The 10-kΩ, 1-μF RC network filters noise, and $IC_2$'s gain provides the desired output scale factor. Circuit biasing permits 8V to appear across the bridge, which requires the 100-mA-capable LT1054 to sink about 24 mA. You can use the ratio output to reference a monitoring A/D converter.

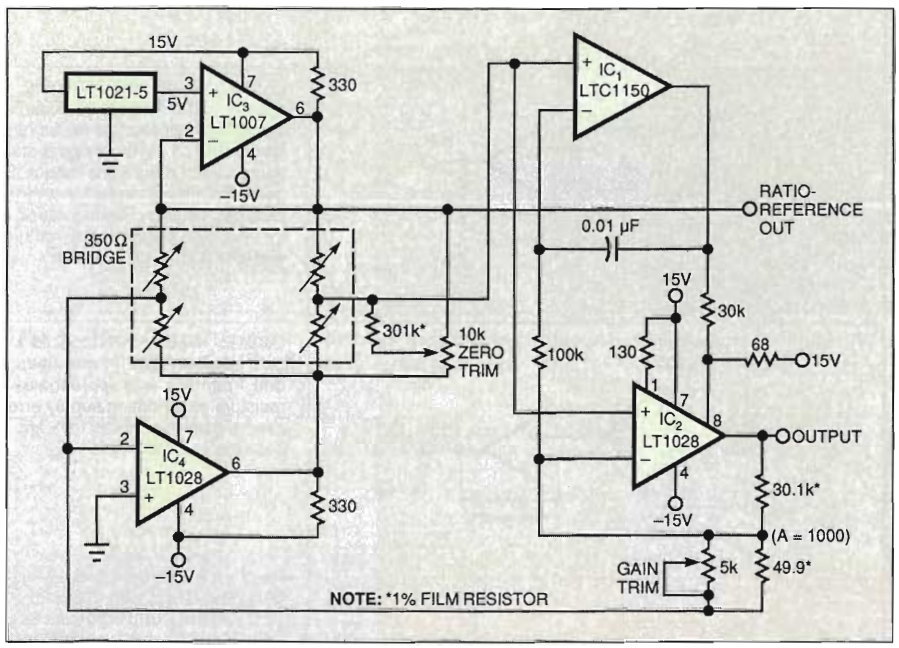



***Fig 5—This chopper-stabilized bridge amplifier*** *features low noise, common-mode suppression, and a small offset error.*

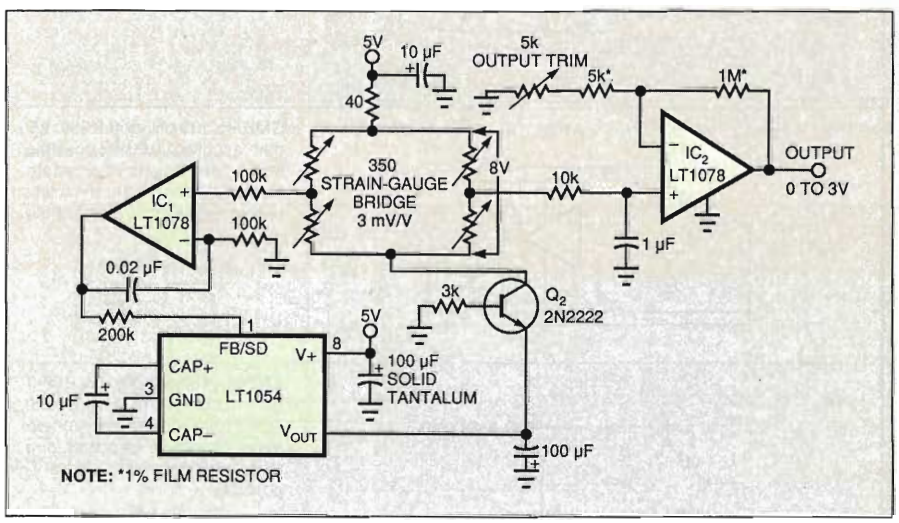



***Fig 6—Using a positive-to-negative converter,*** *this high-output bridge circuit operates from a single 5V supply.*

### Switched-capacitor amplifier

Switched-capacitor methods are another way to provide signal conditioning for bridge outputs. **Fig 7** uses such a method in a high-precision scale application. This circuit for weighing human subjects resolves 0.01 lb at 300 lbs full scale. The strain-gauge-based transducer platform is excited at 10V by the LT1021 reference, $IC_1$, and $IC_2$. The LTC1043 switched-capacitor block combines with $IC_3$ to form a differential-input, chopper-stabilized amplifier. The LTC1043 alternately connects the 1-μF capacitor between the output of the strain-gauge bridge and the input to $IC_3$. A second 1-μF capacitor stores the LTC1043 output, maintaining $IC_3$'s input at dc. The LTC1043's low charge injection maintains a differential-to-single-ended transfer accuracy of about 1 ppm at dc and low frequencies. The 0.01-μF capacitor sets the commutation rate to approximately 400 Hz. $IC_3$'s scaled gain provides 3.0000V for a 300.00-lb full-scale output.

The extremely high resolution of this scale requires filtering to produce useful results. Even slight body movement acting on the scale's platform can cause significant noise in $IC_3$'s output. This fact is dramatically apparent in **Fig 8**'s tracings. The total force on the platform is equal to gravity pulling on the body (the weight) plus any additional accelerations within or acting upon the body. Trace B of **Fig 8** shows that each time the heart pumps, the acceleration of the blood moving in the arteries shows up as weight. To prove this theory, the subject gets off the scale and runs in place for 15 seconds. When the subject returns to the platform, the

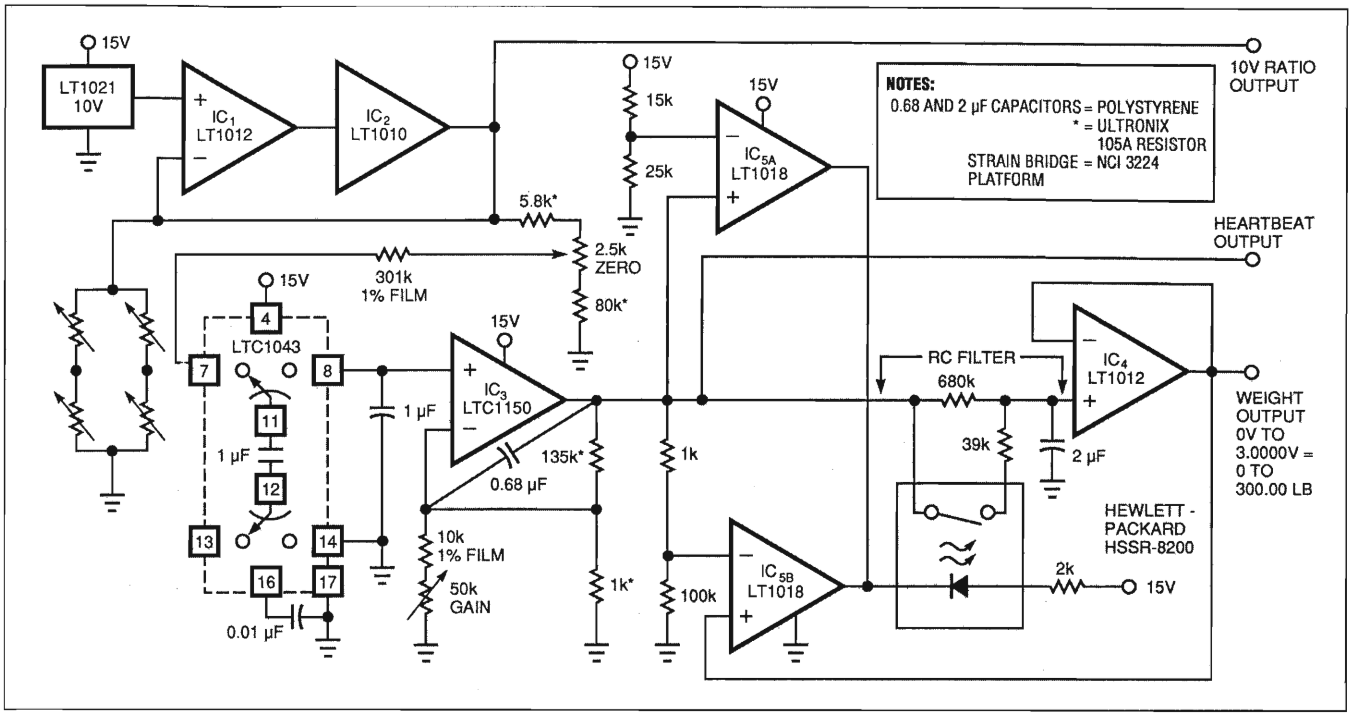



***Fig 7—Using switched-capacitor techniques,*** *this weight-scale circuit can resolve 0.01 lb at 300 lbs full scale.*

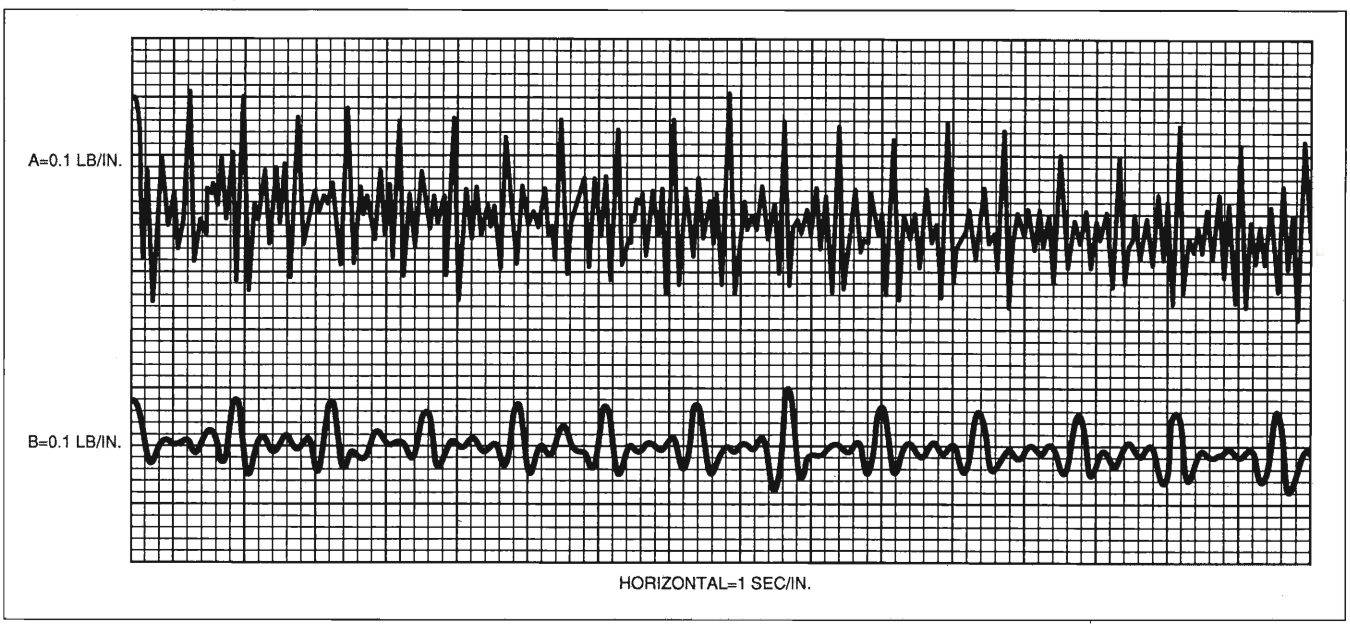



***Fig 8—These tracings show the effects of a subject*** *on the weight-scale platform of* ***Fig 7.*** *Trace B shows the subject at rest; trace A shows the effects after the subject has exercised.*

heart should be working harder. Trace A confirms this prediction. The exercise causes the heart to work harder, forcing greater acceleration per stroke.

Another source of noise is body motion. As the body moves around, its mass doesn't change but the platform picks up the instantaneous accelerations and reads them as weight shifts. These fluctuations might seem to make a 0.01-lb measurement meaningless, but filtering the noise yields a time-averaged value. A simple RC lowpass filter will do the job, but it requires excessively long settling times to filter noise fundamentals in the 1-Hz region. Another approach works much better.

In **Fig 7,** $IC_4$, $IC_5$, and their associated components form a filter that switches its time constant from short to long when the output approaches the final value. With no weight on the platform, $IC_3$'s output is zero. $IC_4$'s output is also zero, $IC_{5B}$'s output is indeterminate, and $IC_{5A}$'s output is low. The MOSFET optocoupler's LED turns on, putting the RC filter into a short-time-constant mode. When someone gets on the scale, $IC_3$'s output rises rapidly. $IC_{5A}$ goes high, but $IC_{5B}$ trips low, which keeps the RC filter in its short-time-constant mode. The 2-µF capacitor charges rapidly, and $IC_4$ quickly settles to a final value plus or minus body motion and

*Instrumentation amplifiers, which have fully differential inputs and internally determined stable gain, often make good bridge amplifiers.*

heartbeat noise. $IC_{5B}$'s negative input sees 1% attenuation from $IC_3$; its positive input does not. This condition causes $IC_{5B}$ to switch high when $IC_4$'s output arrives within 1% of its final value. The optocoupler goes off, and the filter switches into a long-time-constant mode, thus eliminating noise in $IC_4$'s output. The 39-kΩ resistor prevents overshoot, ensuring monotonic outputs from $IC_4$.

When the subject steps off the scale, $IC_3$ quickly returns to zero, and $IC_{5A}$ immediately goes low, turning on the optocoupler. This action quickly discharges the 2-μF capacitor, which rapidly returns $IC_4$'s output to zero. The bias string at $IC_{5A}$'s input maintains the scale in the short-time-constant mode for weights less than 0.50 lb. This condition permits the circuit to respond rapidly when small objects (or persons) are on the platform. To trim this circuit, adjust the zero potentiometer for a 0V output with no weight on the platform. Next, set the gain adjustment for a 3.0000V output for a 300.00-lb platform weight. Repeat this procedure until both points are fixed.

Another example of using optical techniques to enhance performance is the circuit in **Fig 9.** This switched-capacitor-based instrumentation amplifier can handle transducer signal conditioning where high common-mode voltages exist. The circuit features low offset and drift because of the LTC1150 chopper-stabilized op amp ($IC_1$). The design also incorporates a switched-capacitor front end to achieve some specifications not available in a conventional instrumentation amplifier.

The common-mode rejection ratio at dc for the front end exceeds 160 dB. The amplifier operates over a ±200V common-mode range; gain accuracy and stability are limited only by external resistors. Chopper-stabilized $IC_1$ sets the offset drift at 0.05 μV/°C. The high common-mode voltage capability of the design enables it to withstand transient and fault conditions often present in industrial environments.

The bridge's output feeds two LED-driven, optically coupled MOSFET switches, $S_1$ and $S_2$,

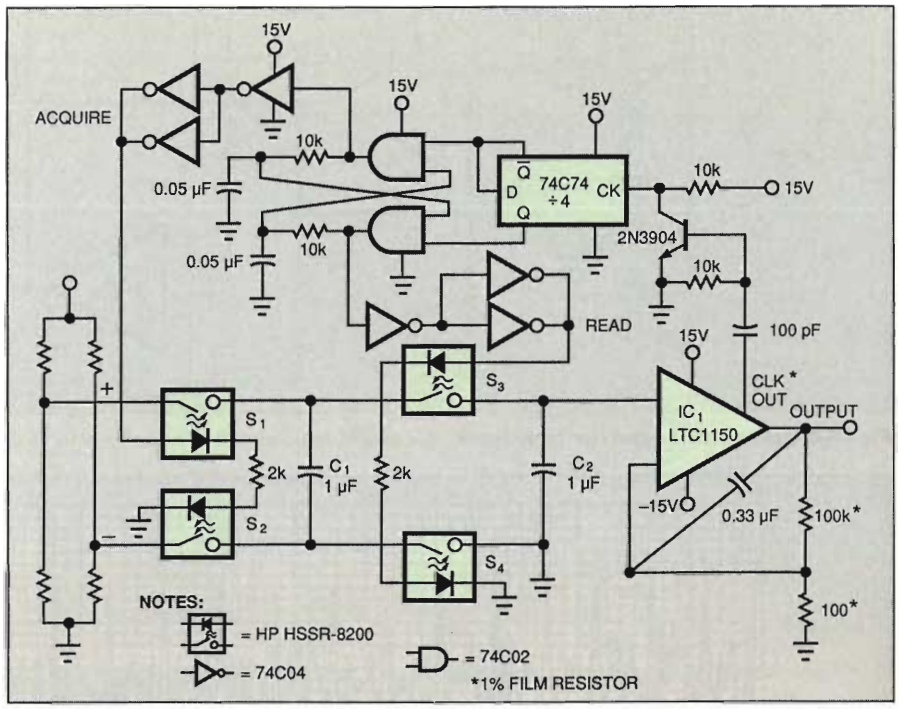



***Fig 9—This optically coupled switched-capacitor instrumentation amplifier*** *provides a floating input and features a 200V common-mode range.*

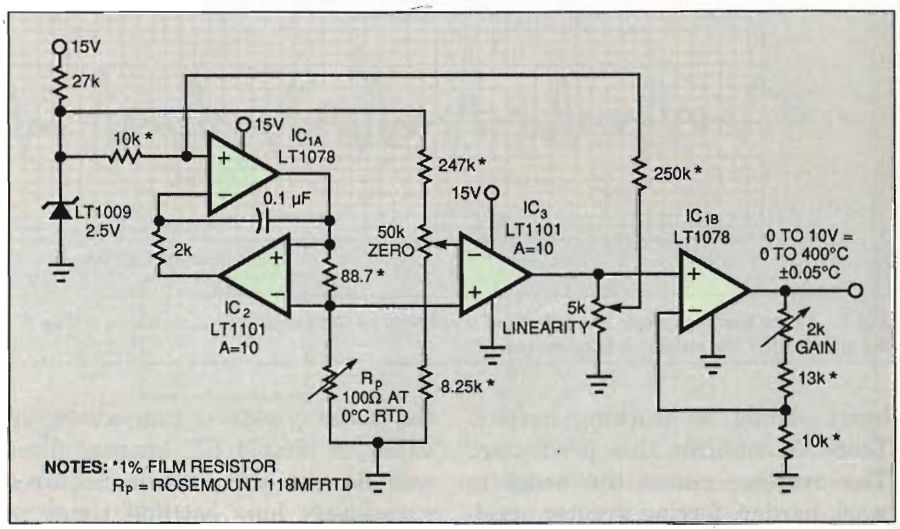



***Fig 10—Using platinum RTDs in a bridge configuration,*** *this circuit can measure temperatures over a range of 0 to 400°C.*

which are in series with two similar switches, $S_3$ and $S_4$. CMOS logic functions, clocked from $IC_1$'s internal oscillator, generate nonoverlapping clock outputs that drive the LEDs. When the acquire pulse is high, $S_1$ and $S_2$ are on, and $C_2$ acquires the differential voltage at the bridge's output. During this interval, $S_3$ and $S_4$ are off. When the acquire pulse falls, $S_1$ and $S_2$ begin to go off. After a delay to allow $S_1$ and $S_2$ to fully open, the read pulse goes high, turning on $S_3$ and $S_4$.

Capacitor $C_1$ acts as a ground-referred voltage source, which $IC_1$ reads. $C_2$ lets $IC_1$'s input retain $C_1$'s value when the circuit returns to the acquire mode. $IC_1$ provides the circuit's output; its gain is set in normal fashion by feedback resistors. The 0.33-μF feedback capacitor sets the rolloff. The differential-to-single-ended transition that the switches and capacitors perform prevents $IC_1$ from ever seeing the input's common-mode signal. The breakdown specification of the optically driven MOSFET switch enables the circuit to operate at common-mode levels of ±200V. In addition, the optical drive to the MOSFETs eliminates the charge-injection problems common to FET switched-capacitor networks.

Platinum resistance temperature detectors (RTDs) are frequently used in bridge configurations for temperature measurement. **Fig 10**'s circuit is highly accurate and features a ground-referred RTD. The ground connection is highly desirable for reducing noise. A current source drives the bridge's RTD leg; the opposing bridge branch is voltage biased. The current drive lets the voltage across the RTD vary directly with the device's temperature-induced resistance shift. The difference between this potential and the potential of the opposing bridge leg is the bridge's output.

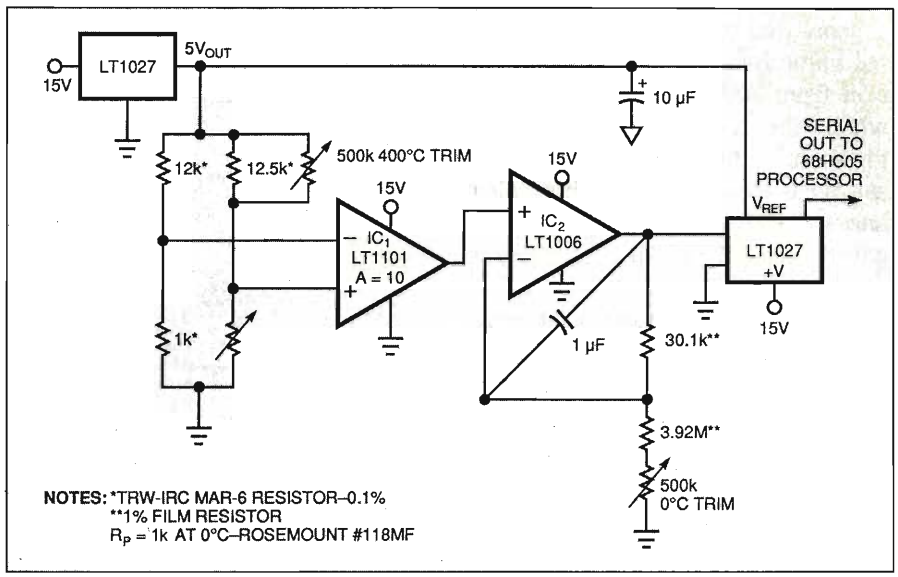



***Fig 11—Combined with a microprocessor,*** *this circuit uses digital correction to achieve a precise, linear output from the platinum RTD bridge.*

$IC_{1A}$ and instrumentation amplifier $IC_2$ form a voltage-controlled current source. $IC_{1A}$, biased by the LT1009 voltage reference, drives current through the 88.7Ω resistor and the RTD. $IC_2$ senses voltage differentially across the 88.7Ω resistor and closes a loop back to $IC_{1A}$. The 2-kΩ, 0.1-μF combination sets the amplifier rolloff for this stable configuration. Because $IC_{1A}$'s loop forces a fixed voltage across the 88.7Ω resistor, the current through $R_P$ is constant. $IC_1$'s operating point is primarily fixed by the 2.5V LT1009 reference.

The constant current through the RTD forces the voltage across it to vary with the RTD's resistance, which has a nearly linear positive temperature coefficient. The degree of nonlinearity could cause an error of several degrees over the circuit's 0 to 400°C operating range. The bridge's output feeds instrumentation amplifier $IC_3$, which provides differential gain while correcting nonlinearity. The correction is implemented by feeding a portion of $IC_3$'s output back to $IC_1$'s input via the 10- and 250-kΩ divider. This correction causes the current through $R_P$ to slightly shift with the resistor's operating point, which compensates sensor nonlinearity to within ±0.05°C. $IC_{1B}$ provides additional scaled gain and furnishes the circuit output.

To calibrate this circuit, substitute a precision decade box, such as the General Radio (Lincoln, NE) 1432K, for $R_P$. Set the box to the 0°C value (100.00Ω) and adjust the offset trim for a 0.00V output. Next, set the box for a 140°C value (154.26Ω) and adjust the gain trim for a 3.500V output reading. Finally, set the box to 400.00°C (249.0Ω) and trim the linearity adjustment for a 10.000V output. Repeat this sequence until all three points are fixed. Total error over the entire range will be within ±0.05°C. The resistance values in parentheses are for a nominal 100.00Ω (0°C) sensor. You can use

*Chopper-stabilized CMOS amplifiers can help eliminate offset drift with time and temperature.*

sensors that deviate from this nominal value by factoring in the deviation from 100.00Ω. This deviation, which the manufacturer specifies for each individual sensor, is an offset term caused by winding tolerances during RTD fabrication. The gain slope of the platinum is primarily fixed by the purity of the material and has a very small error term.

### Digitally corrected RTD bridge

The previous example relies on analog techniques to achieve a precise, linear output from the platinum RTD bridge. The circuit in **Fig 11** uses digital corrections to obtain similar results. A microprocessor corrects any residual RTD nonlinearities as well as the bridge's inherent nonlinear output.

The LT1097 drives the bridge with 5V. Instrumentation amplifier $IC_1$ extracts the bridge's differential output. $IC_1$'s output is fed to the LTC1290 12-bit A/D converter via gain-scaling stage $IC_2$. The A/D converter's raw output codes reflect the bridge's nonlinear output vs temperature. The processor corrects the converter's output and produces linearized, calibrated output data. RTD and resistor tolerances mandate zero-and full-scale trims, but no linearity correction is necessary. $IC_2$'s analog output is available for feedback-control applications. Guy M Hoover developed the complete software code for the 68HC05 processor; you can get the code from Linear Technology at no cost.

### Thermistor bridge

Another temperature-measuring bridge, **Fig 12**, uses a thermistor as a sensor. The LT1034 excites the bridge. The 3.2-kΩ and 6250Ω resistors are supplied with the thermistor sensor. The network's overall response is linearly related to the thermistor's sensed temperature. The network forms one leg of a bridge, and the resistors make up the opposing leg. Trimming this opposing leg sets the bridge output to zero at 0°C. Instrumentation amplifier $IC_1$ provides gain, and $IC_2$ provides additional trimmed gain to supply a calibrated output. You calibrate the circuit as you would the platinum RTD circuit but with the linearity trim deleted.

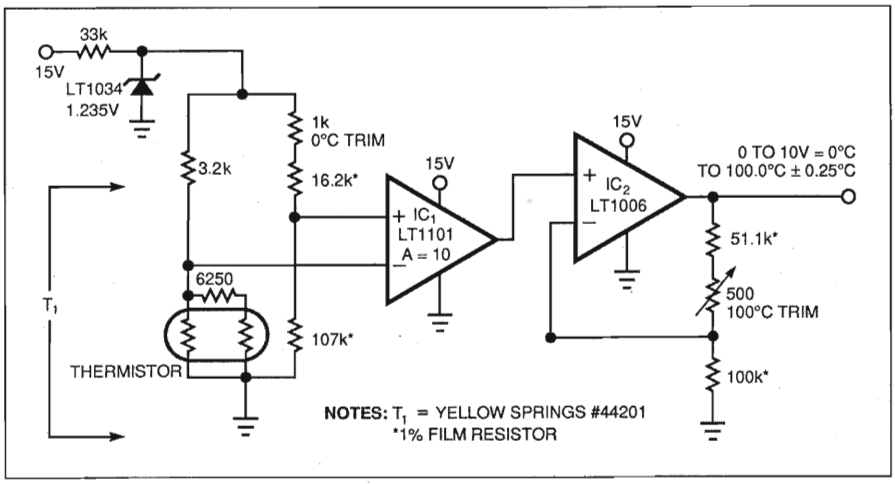



***Fig 12—This temperature-measuring bridge** uses a thermistor as a sensor to provide a linear output.*

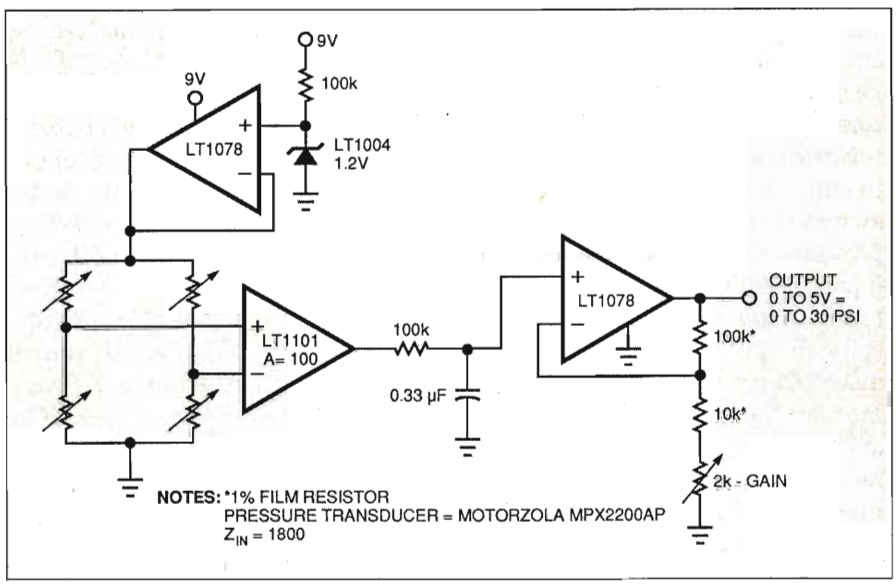



***Fig 13—Using a semiconductor-based transducer,** this low-power circuit has a bridge current less than 700 µA.*

In many cases, you'll want to operate a bridge circuit at low power. The most obvious way to minimize power consumption is by restricting the drive to the bridge. However, many bridge-based transducers are low-impedance devices, which complicates the design. Although similar to **Fig 2**, the **Fig 13** circuit re-

duces the bridge current to less than 700 μA by using a semiconductor-based bridge transducer. The input resistance of these devices is significantly higher than that of resistance-based bridges. This higher input resistance minimizes current drain and power dissipation. Semiconductor-based pressure transducers are less expensive than bonded strain-gauge types, but they have reduced accuracy and stability.

**Fig 14** was derived directly from the **Fig 6** circuit and illustrates a simple way of reducing power without sacrificing the bridge's output signal level. The technique applies when continuous output is not a requirement. This circuit can sit in the quiescent state for long periods with relatively brief on times. A typical application would be obtaining remote weight information for storage tanks where weekly readings are sufficient. Quiescent current is about 150 μA with an on-state current of 50 mA typ.

With $Q_1$'s base unbiased, all circuitry is off except the LT1054 plus-to-minus voltage converter, which draws 150 μA of quiescent current. When $Q_1$'s base is pulled low, its collector supplies power to $IC_1$ and $IC_2$. $IC_1$'s output then goes high, turning on the LT1054. The LT1054's output (pin 5) heads toward −5V, and $Q_2$ comes on, which permits the bridge current to flow. To balance its inputs, $IC_1$ servo controls the LT1054 to force the bridge's midpoint to 0V. The bridge ends up with approximately 8V across it, requiring the 100-mA-capable LT1054 to sink about 24 mA. The 0.02-μF capacitor stabilizes the loop. The $IC_1$-LT1054 loop's negative output sets the bridge's common-mode voltage to zero, allowing $IC_2$ to take a single-ended measurement. The output-trim adjustment scales the circuit for 3-mV/V strain-bridge transducers, and the 100-kΩ, 0.1-μF combination provides noise filtering.

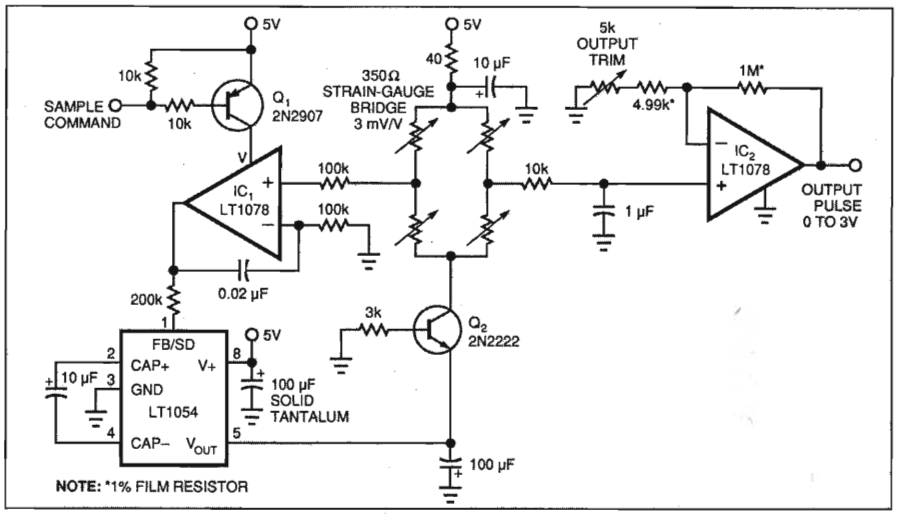



***Fig 14—Applicable where a continuous output is not required,*** *this low-power circuit conserves bridge power by turning it off when not needed. Quiescent current is typically 150 μA.*

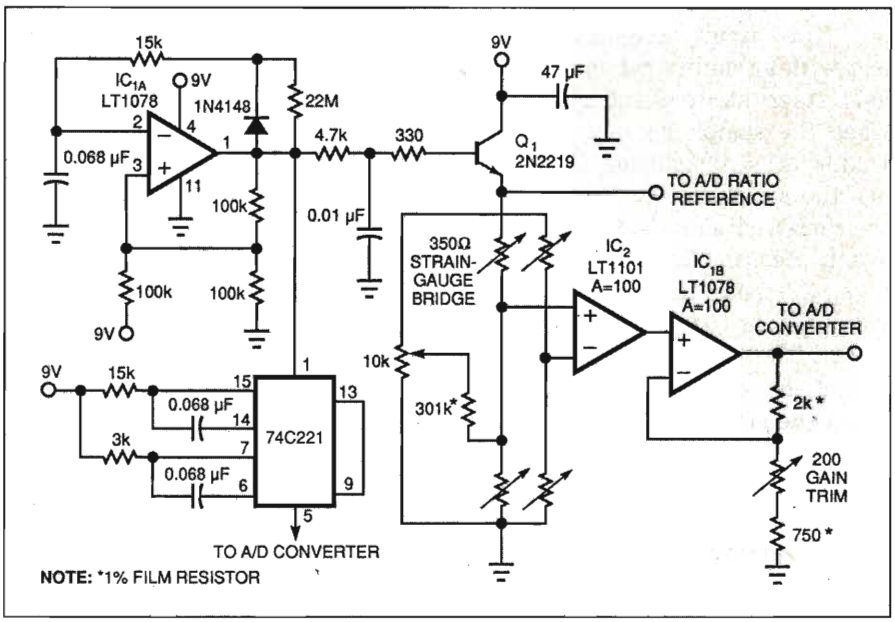



***Fig 15—This strain-gauge bridge signal conditioner*** *uses strobed-power techniques to reduce power consumption. At a clock rate of 2 Hz, the circuit's on time is restricted to 250 μsec, which limits the average current drain to about 200 μA.*

**Fig 15**, an obvious extension of **Fig 14**, automates the strobing into a clocked sequence. Circuit on time is restricted to 250 μsec at a clock rate of approximately 2 Hz. This restriction limits the average current drain to approximately 200 μA. Oscillator $IC_{1A}$ produces the 250-μsec clock pulse every 500

*Switched-capacitor instrumentation amplifiers can provide effective signal conditioning where high common-mode voltages exist.*

msec. A filtered version of this pulse feeds $Q_1$, whose emitter provides a slew-limited bridge drive. $IC_{1A}$'s output also triggers a delayed pulse produced by the 74C221's one-shot output. The timing is such that the pulse occurs well after the $IC_{1B}$-$IC_2$ bridge-amplifier output settles. A monitoring A/D converter, triggered by this pulse, can acquire $IC_{1B}$'s output.

The slew-limited bridge drive prevents the strain-gauge bridge from seeing a fast rise pulse, which could cause long-term transducer degradation. To calibrate this circuit, trim the zero and gain controls for appropriate outputs.

**Fig 16** extends the sampling approach to include a continuous output. The circuit accomplishes this end with an additional sample-and-hold stage at its output. $Q_2$ is off when the sample command is low. Under these conditions, only $IC_2$ and the LTC201 receive power, and the current drain is less than 60 μA. When the sample command pulses high, $Q_2$'s collector goes high, providing power to all other circuit elements. The 10Ω, 1-μF RC combination at the input of the LT1021 prevents the strain-gauge bridge from seeing a fast-rise pulse, which could cause long-term transducer degradation. The LT1021-5 reference's output drives the strain-gauge bridge, and instrumentation amplifier $IC_1$ provides gain for the bridge's output signal. Simultaneously, $S_1$'s switch-control input ramps toward $Q_2$'s collector. At approximately half $Q_2$'s collector voltage, $S_1$ turns on, and $C_1$ stores $IC_1$'s output.

When the sample command drops low, $Q_2$'s collector falls, the bridge and its associated circuitry shut down, and $S_1$ goes off. $C_1$'s stored value appears at gain-scaled $IC_2$'s output. The RC delay at $S_1$'s control input ensures glitch-free operation by preventing $C_1$ from updating until $IC_1$ has settled. During the 1-msec sampling phase, the supply current approaches 20 mA; a 10-Hz sampling rate cuts the effective drain to less than 250 μA. Slower sampling rates will further reduce drain, but $C_1$'s droop rate (about 1 mV/100 msec) sets an accuracy constraint. The 10-Hz rate provides adequate bandwidth for most transducers. The gain trim lets you calibrate 3-mV/V slope-factor transducers. You should rescale this trim for other transducer types. This circuit's effective current drain is about 250 μA, and $IC_2$'s output is accurate enough for 12-bit systems.

Remember that this circuit is a sampled system. Although the output is continuous, information is collected at a 10-Hz rate. You should keep the Nyquist limit in mind when interpreting results.

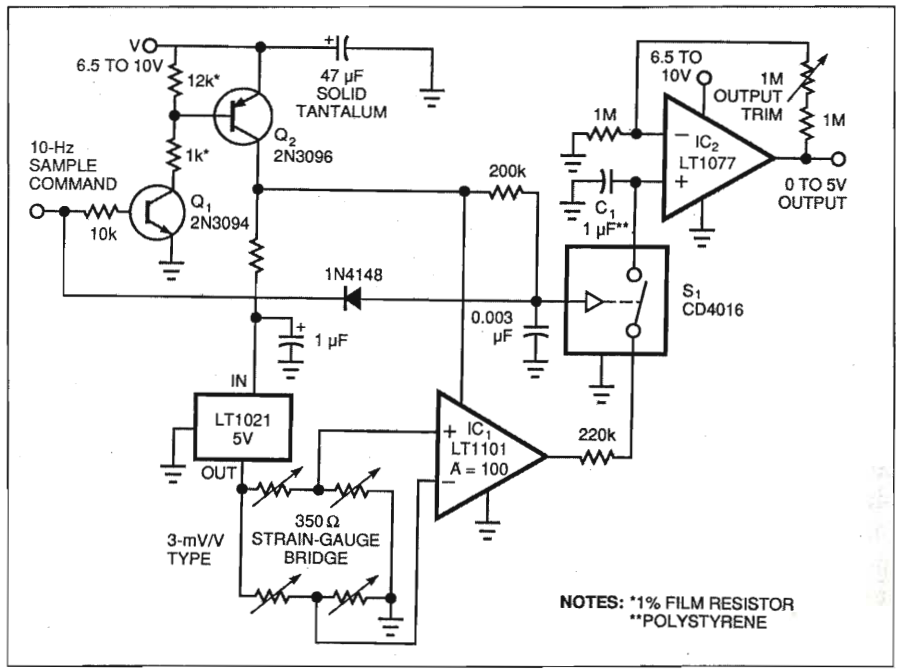



***Fig 16—This pulse-excited bridge-signal conditioner*** *uses a sample-and-hold circuit to provide a dc output.*

**Fig 17** is a special case of a continuous-output sampled-bridge drive. The circuit is intended for applications requiring extremely high-resolution outputs from a bridge transducer. This circuit puts 100V across a 10V, 350Ω strain-gauge bridge for short periods of time. The high pulsed-voltage drive proportionally increases the bridge output without forcing excessive dissipation. In fact, although this circuit is not intended to reduce power, the average bridge current is far below the normal 29 mA obtained with 10V dc excitation.

The key to the high resolution obtainable with this circuit is combining the 10× higher bridge gain (300 mV full scale vs the normal 30 mV) with a chopper-stabilized amplifier in the sample-and-hold output stage.

When oscillator $IC_{1A}$'s output is high, $Q_6$ turns on, and $IC_2$'s negative input is pulled above ground.

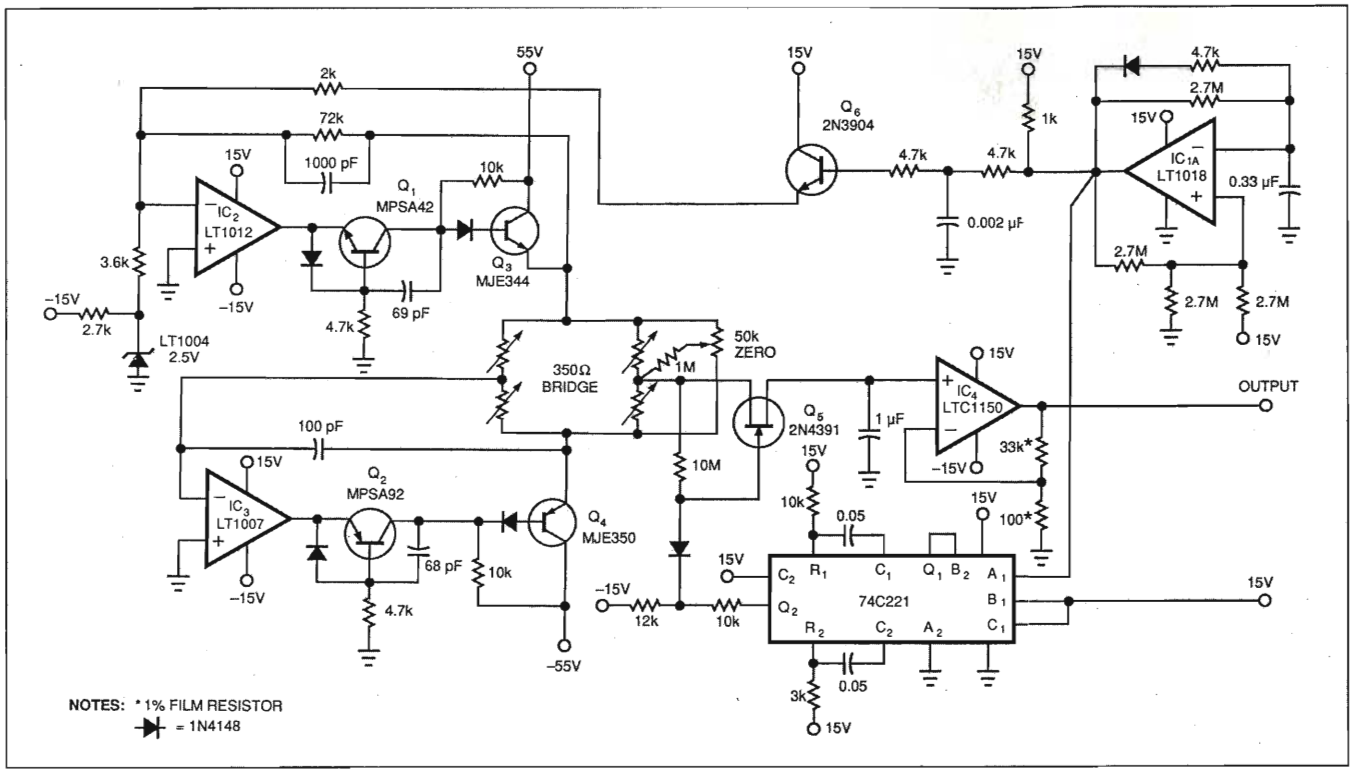



***Fig 17—A special case of sampled drive,*** *this circuit puts 100V across a 10V, 350Ω strain-gauge bridge for short periods of time. The circuit is intended for applications requiring high-resolution outputs from a bridge transducer.*

$IC_2$'s output goes negative, which turns on $Q_1$. $Q_1$'s collector then goes low, robbing $Q_3$'s base drive and cutting it off. Simultaneously, $IC_3$ enforces its loop by biasing $Q_2$ into conduction, which turns on $Q_4$. Under these conditions, the voltage across the bridge is essentially zero.

When $IC_{1A}$'s output is low, RC-filter-driven $Q_6$ responds by cutting off slowly. Now, only the current through the 3.6-kΩ resistor affects $IC_2$'s negative input. The input begins to head negative, causing $IC_2$'s output to rise. $Q_1$ comes out of saturation, and $Q_3$'s emitter voltage rises. Initially, this action is rapid, but feedback to $IC_2$'s negative input closes a control loop, and a 1000-pF capacitor restricts the rise time. The 72-kΩ resistor sets $IC_2$'s gain at 20 with respect to the LT1004 2.5V reference, and $Q_3$'s emitter servo controls to 50V.

$IC_3$ responds to the bridge's biasing by moving its output in the negative direction. $Q_2$ tends toward cutoff, increasing $Q_4$'s conduction. $IC_3$ biases its loop to maintain the bridge midpoint at zero. To bias its loop, $IC_3$ must produce a complementary output to $IC_2$'s loop. $IC_3$'s loop rolloff is considerably faster than $IC_2$'s, ensuring that it will faithfully track $IC_2$'s loop action. Similarly, $IC_3$'s loop is slaved to $IC_2$'s loop output and produces no other outputs. Under these conditions, the bridge sees 100V for the 1-msec duration of the clock pulse.

$IC_{1A}$'s clock output also triggers the 74C221 one-shot circuit. This circuit delivers a delayed pulse to $Q_5$, which turns on and charges the 1-µF capacitor to the bridge's output voltage. With $IC_3$ forcing the bridge's left-side midpoint to zero, $Q_5$, the 1-µF capacitor, and $IC_4$ see a single-ended, low-voltage signal. The complementary, controlled rise times of the control loops prevent high-transient common-mode voltages.

$IC_4$, which has gain, provides the circuit output. The 74C221's pulse width ends during the bridge's on time, thus preserving the integrity of the sampled data. When oscillator $IC_1$ goes high, the control loops remove the bridge's drive, returning the circuit to quiescence. The 1-µF capacitor maintains $IC_4$'s output at dc. $IC_{1A}$'s 1-Hz clock rate is adequate to prevent a deleterious charge droop on the 1-µF capacitor, but slow enough to limit the bridge's power dissipation. The controlled rise and fall times across the bridge prevent possible long-term transducer degradation by eliminating high ΔV\ΔT-induced effects.

When using this circuit, remember that it is a sampled system. Although the output is continuous, information is collected at a 1-Hz rate. The Nyquist limit applies and must be taken into account when interpreting results. EDN

## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

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EDN DESIGNERS' GUIDE TO

bridge circuits
Part 2

# AC-driven bridge circuits suit specific applications

*Part 1 of this 2-part series covered basic bridge circuits and their use in dc- and pulse-driven applications. The series concludes with a discussion of ac-driven circuits, which are useful in specialized applications. Also included in this final part are guides to distortion measurements and bridge interfaces.*

Jim Williams, *Linear Technology Corp*

Many bridge circuits work well with dc excitation of the transducer or detector; others require or benefit greatly from an ac drive. An extension of dc pulse-excited bridges, **Fig 1** uses synchronous demodulation to achieve very high noise rejection. An ac carrier excites the bridge and synchronizes the gain-stage demodulator. In this application, the signal source is a thermistor bridge that detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber.

The 500-Hz carrier signal (**Fig 2**, trace A) is applied at the input of transformer $T_1$. The transformer's floating output drives the thermistor bridge. The bridge's single-ended output drives $IC_1$, which operates at an ac gain of 1000. A 60-Hz broadband noise source is also deliberately injected into $IC_1$'s output (trace B). $C_1$ detects the carrier's zero crossings, and its output clocks the LTC1043 (trace C). $IC_1$'s output (trace D) shows the desired 500-Hz signal buried within the 60-Hz noise source.

The LTC1043's zero-cross-synchronized switching at $IC_2$'s positive input (trace E) causes $IC_2$'s gain to alternate between $\pm 1$. As a result, $IC_2$ synchronously demodulates $IC_1$'s output. $IC_2$'s output (trace F) consists of the demodulated carrier signal and noncoherent components. The desired carrier amplitude and polarity information is discernible in $IC_2$'s output and is extracted by filter averaging at $IC_3$.

To trim this circuit, adjust the phase potentiometer so that $C_1$ switches when the carrier crosses through zero.

Level transducers measure the angle from an ideal level and are used in road construction, machine tools, inertial navigation systems, and other applications requiring a gravity reference. One of the most elegantly simple level transducers is a small tube nearly filled with a partially conductive liquid. If the tube is level with respect to gravity, the bubble resides in the tube's center, and the electrode resistances to a common reference are identical. As the tube shifts away from level, the electrode resistances increase and decrease proportionally. By controlling the tube's shape at manufacture, obtaining a linear

TEST & MEASUREMENT

*The signal conditioning of bridge circuits requires circuitry that provides bridge excitation and a means to extract and modify the bridge's output signal.*

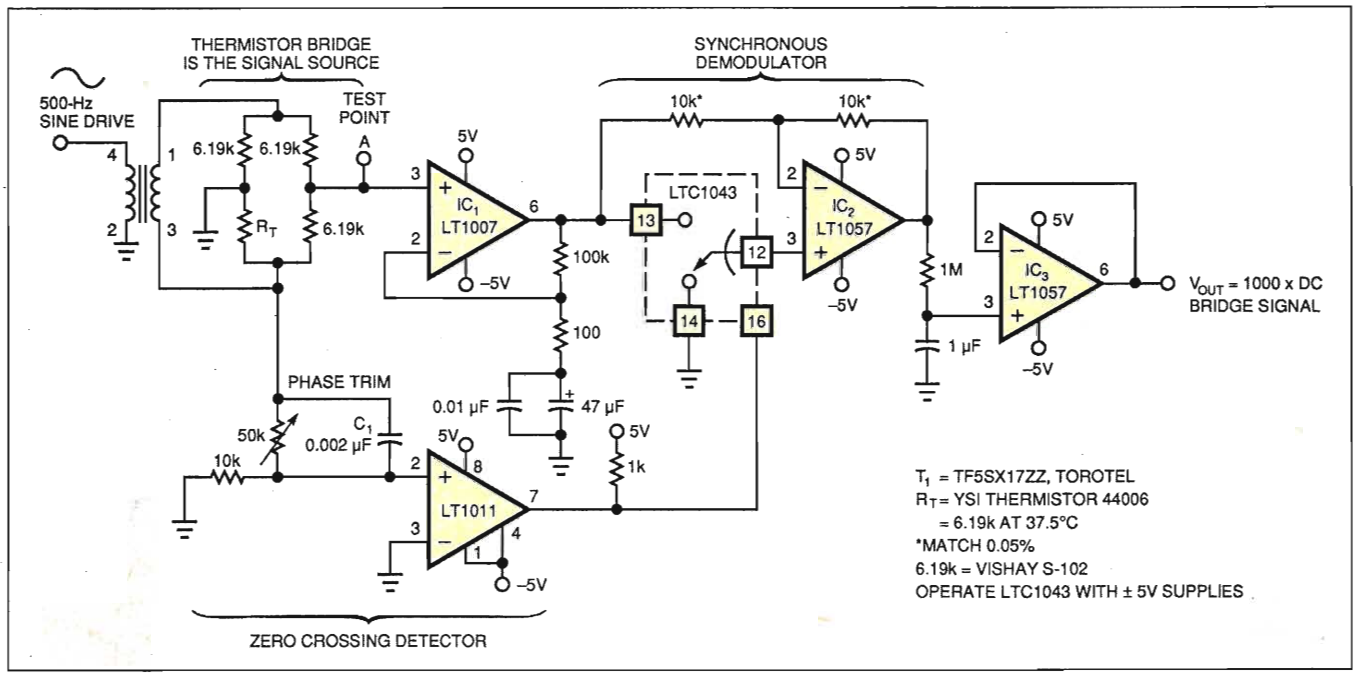


***Fig 1—This lock-in bridge amplifier uses synchronous detection*** *to achieve narrow-band gain and extremely high noise rejection.*

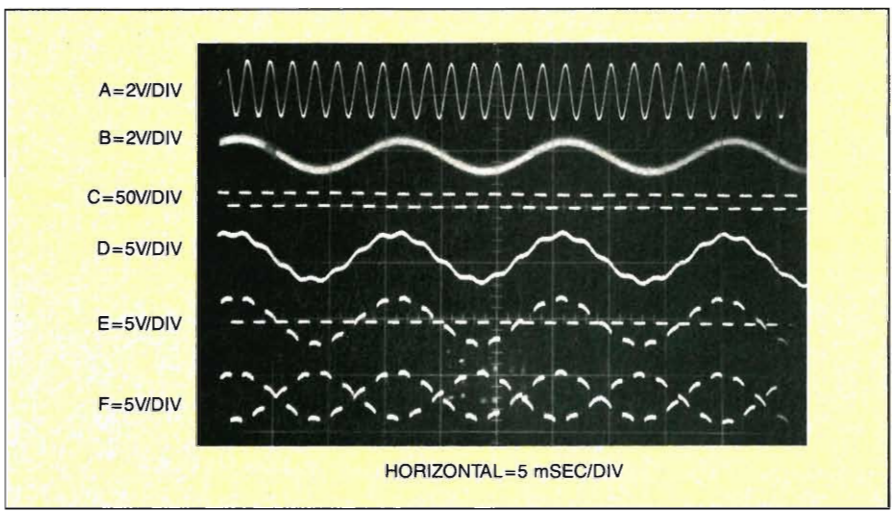


***Fig 2—These scope traces show details of Fig 1's performance.*** *A 500-Hz carrier signal (trace A) is applied at the input of transformer $T_1$, and a 60-Hz broadband noise source is injected into $IC_1$'s output (trace B). The traces also show $C_1$'s output (trace C), $IC_1$'s output (trace D), $IC_2$'s positive input (trace E), and $IC_2$'s output (trace F). Narrow-band synchronous detection permits extraction of extremely low-level coherent signals.*

output signal when the transducer is incorporated in a bridge circuit is possible.

To avoid damaging the partially conductive liquid inside the tube, you must excite these types of transducers with an ac waveform. Signal conditioning involves generating this excitation, extracting angle information, and determining polarity—that is, which side of level the tube is on. The **Fig 3** circuit provides these functions. It directly produces a calibrated frequency output corresponding to the level. A sign-bit output gives polarity information.

The level transducer and a pair of 2-kΩ resistors form the bridge. The ac bridge excitation develops at comparator $IC_{1A}$, which is configured as a multivibrator. $IC_{1A}$ biases $Q_1$, which switches the LT1009's 2.5V potential through the 100-µF capacitor to provide the ac bridge drive. $IC_{3A}$, which operates as a Howland current pump, converts the bridge's differential output ac signal to a current. The diode bridge rectifies this current, whose polarity reverses as the bridge-drive polarity switches. Thus, the 0.03-µF capacitor receives a unipolar charge.

Instrumentation amplifier $IC_2$ measures the voltage across the capacitor and presents its single-ended output to $IC_{1B}$. When the voltage across the 0.03-µF capaci-

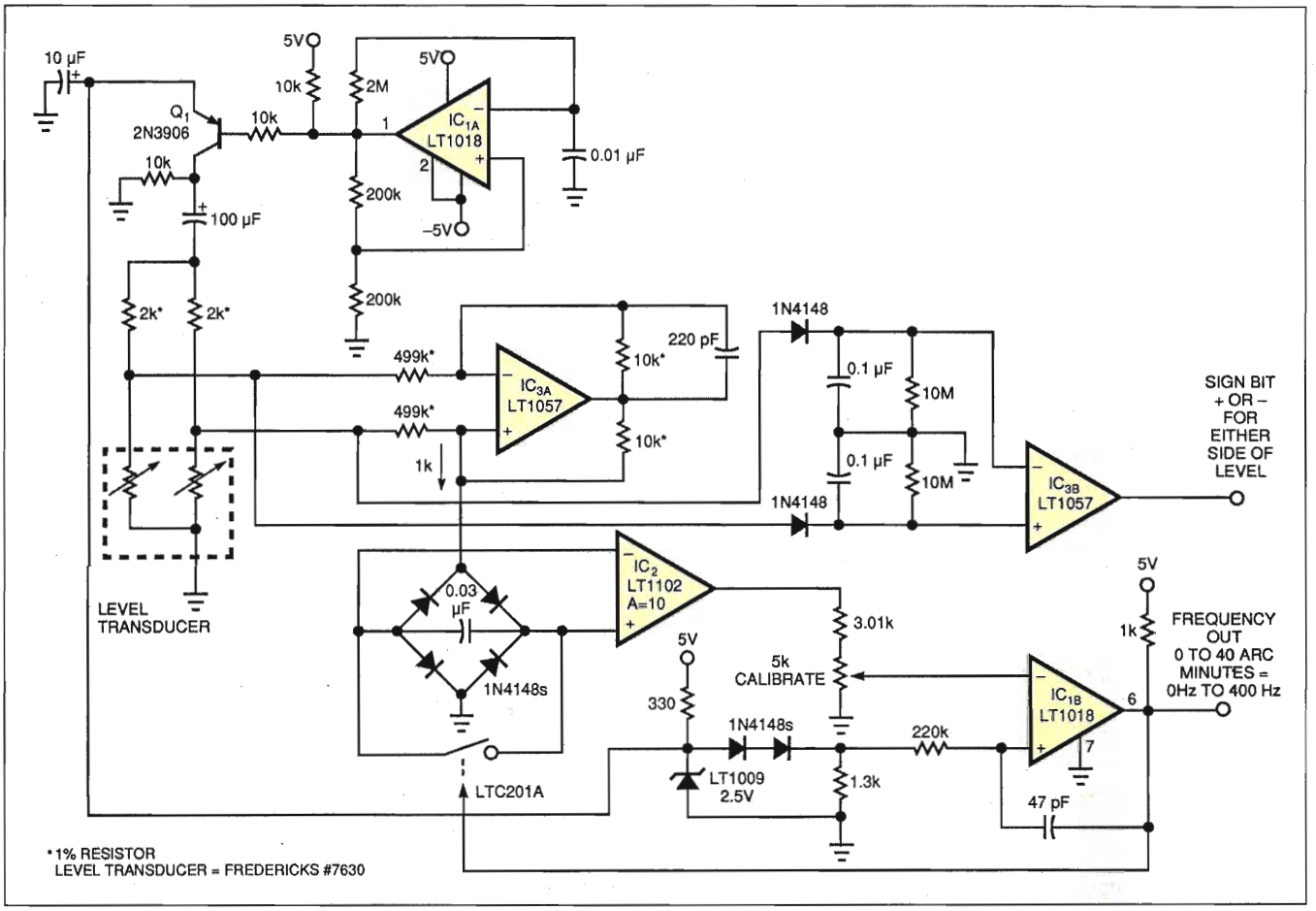


***Fig 3—To prevent damage to the partially conductive liquid*** *in the bubble-based level transducer, this circuit excites the bridge with an ac waveform. Signal conditioning also includes the extraction of angle and polarity information.*

tor becomes high enough, $IC_{1B}$'s output goes high. The high output turns on the LTC201A switch, which discharges the capacitor. When $IC_{1B}$'s ac positive feedback ceases, its output goes low, and the switch goes off. The 0.03-µF capacitor again receives constant-current charging, and the entire cycle repeats. The magnitude of the constant current delivered to the bridge-capacitor configuration determines the frequency of this oscillation. This current's magnitude is set by the transducer bridge's offset, which varies directly with level.

**Fig 4** shows circuit waveforms.

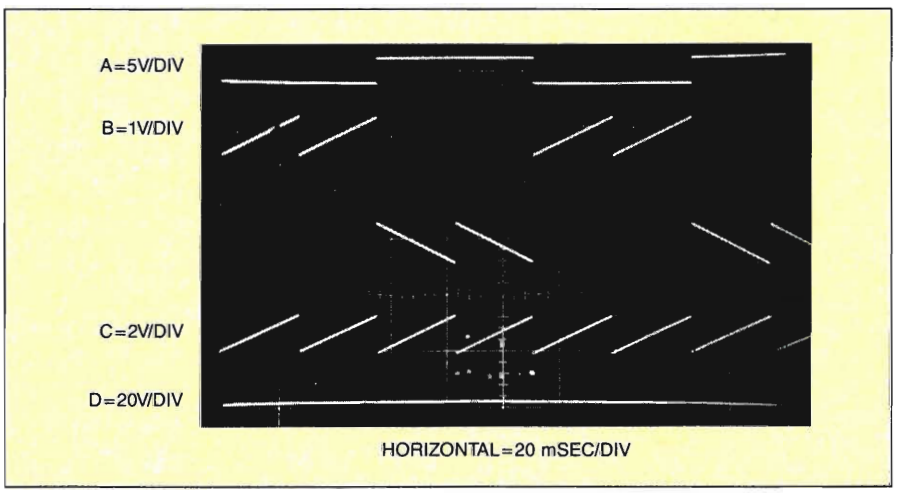


***Fig 4—Level-transducer bridge-circuit waveforms*** *for the circuit in* ***Fig 3*** *correspond to the ac bridge drive (trace A), $IC_{3A}$'s output (trace B), $IC_2$'s output (trace C), and $IC_{1B}$'s output pulse and the circuit's output (trace D).*

*Level transducers that incorporate a partially conductive liquid usually require ac drive to prevent damage.*

Trace A is the ac bridge drive; trace B is $IC_{3A}$'s output. When the bridge drive changes polarity, $IC_{3A}$'s output rapidly changes sign to maintain a constant current into the bridge-capacitor combination. $IC_2$'s output (trace C) is a unipolar, ground-referred ramp. Trace D is $IC_{1B}$'s output pulse and the circuit's output. The diodes at $IC_{1B}$'s positive input provide temperature compensation for the sensor's positive temperature coefficient. This compensation lets $IC_{1B}$'s trip voltage ratiometrically track the bridge's output as a function of temperature. Operating open loop, $IC_{3B}$ determines polarity by comparing the rectified and filtered bridge output signals to ground.

To calibrate this circuit, place the level transducer at a known 40-arcminute angle and adjust the 5-kΩ trimmer at $IC_{1B}$ for a 400-Hz output. The transducer limits the circuit's accuracy to approximately 2.5%.

### Time-domain bridge circuit

The **Fig 5**'s circuit is another ac-based bridge, but it works in the time domain rather than the frequency domain. This circuit particularly suits capacitance measurement, and its operation is straightforward. When switch LTC201A is closed, the comparator's output is high. When the switch opens, capacitor $C_X$ charges. When $C_X$'s potential crosses the voltage the bridge's left-side resistors establish, the comparator trips low. The elapsed time between the switch opening and the comparator going low is proportional to the value of $C_X$.

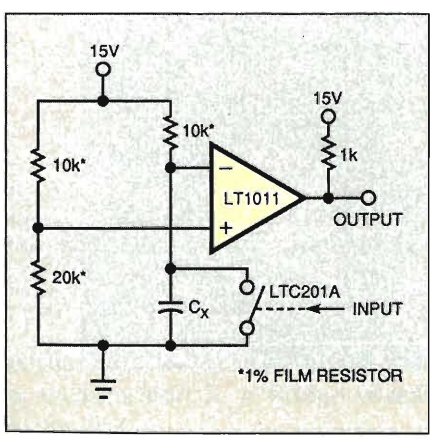


***Fig 5—Particularly applicable to capacitance measurements,*** *this ac-based bridge circuit works in the time domain.*

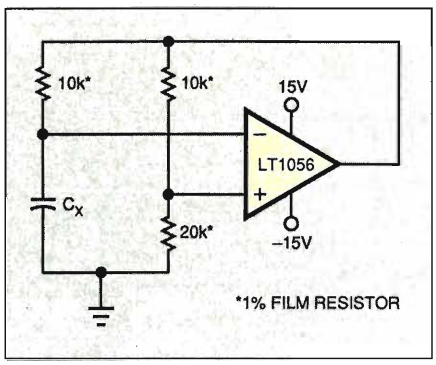


***Fig 6—Recognizable as the classic op amp multivibrator,*** *this bridge-type oscillator circuit generates a square-wave output.*

This circuit is insensitive to supply and repetition-rate variations and can provide good accuracy if you keep the time constants much larger than the comparator and switch delays. For example, the LT1011's delay is about 200 nsec; the LTC201A contributes 450 nsec. To ensure 1% accuracy, the bridge's right-side time constant should not drop below 65 μsec. Switching-charge injection can affect extremely low values of capacitance. In such cases, you should implement the switching by alternating the bridge drive between ground and the 15V supply.

Only someone with an inattentive outlook could resist folding **Fig 5**'s bridge back upon itself to make an oscillator. **Fig 6** is such a circuit—a bridge oscillator. This circuit is also recognizable as the classic op-amp multivibrator. In this version, the 10-and 20-kΩ bridge leg provides switching-point hysteresis; $C_X$ charges via the remaining 10-kΩ resistor. When $C_X$ reaches the switching point, the amplifier's output changes state and abruptly reverses the sign of its positive input voltage. $C_X$'s charging direction also reverses, and oscillations continue. At frequencies that are low compared with amplifier delays, the output frequency is almost entirely dependent on the bridge components. Amplifier input errors tend to ratiometrically cancel; supply shifts similarly cancel. Output saturation and supply asymmetries influence the duty cycle.

### Quartz-stabilized oscillators

Generically similar to **Fig 6**, the **Fig 7** circuit replaces one of the bridge arms with a resonant element. With the crystal removed and a grounded input, the familiar circuit has a noninverting gain of two. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency. The amplifier output swings in an attempt to maintain input balance. Excessive circuit gain prevents linear operation. Oscillations commence as the

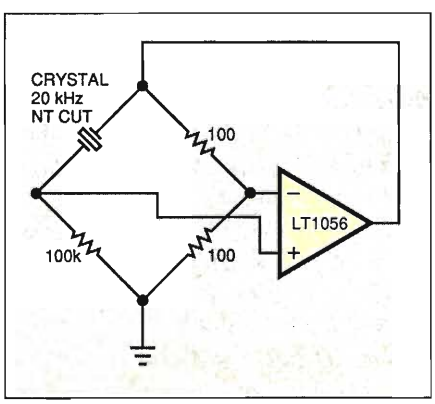


***Fig 7—This bridge-based oscillator circuit*** *uses a quartz crystal as the frequency-determining element.*

## Practical considerations for bridge interfaces

Routing bridge outputs over long lengths of cable is often desirable. You should approach these applications with caution. Even shielded cables are susceptible to picking up noise, and you'll often need input protection. Simple RC filters, such as those in **Fig Aa**, often suffice. The amplifier bias current sets the upper limit on resistor values. FET input amplifiers allow large values of resistance, which minimizes capacitance size.

Leakage eliminates electrolytic capacitors as candidates, which restricts maximum capacitance values to approximately 1 μF. Often, a single capacitor (dashed lines) is all you'll need. Diode clamps prevent high voltage spikes, which are common in industrial environments, from damaging the amplifier. **Fig Ab** summarizes some clamp alternatives.

**Fig Ac** shows a high-order, switched-capacitor-based filter. The LTC1062 has no dc error and offers much better rolloff characteristics than simple RC types. LTC Application Note 20, "Application Considerations for an Instrumentation Lowpass Filter," presents details.

**Fig Ad** shows a preamplifier ahead of a remotely located instrumentation amplifier. The preamplifier raises the signal level on the cable while lowering the drive impedance. When using this circuit, you should evaluate the asymmetrical bridge loading. Usually, you can make the input resistor to the amplifier large enough to minimize any loading effect.

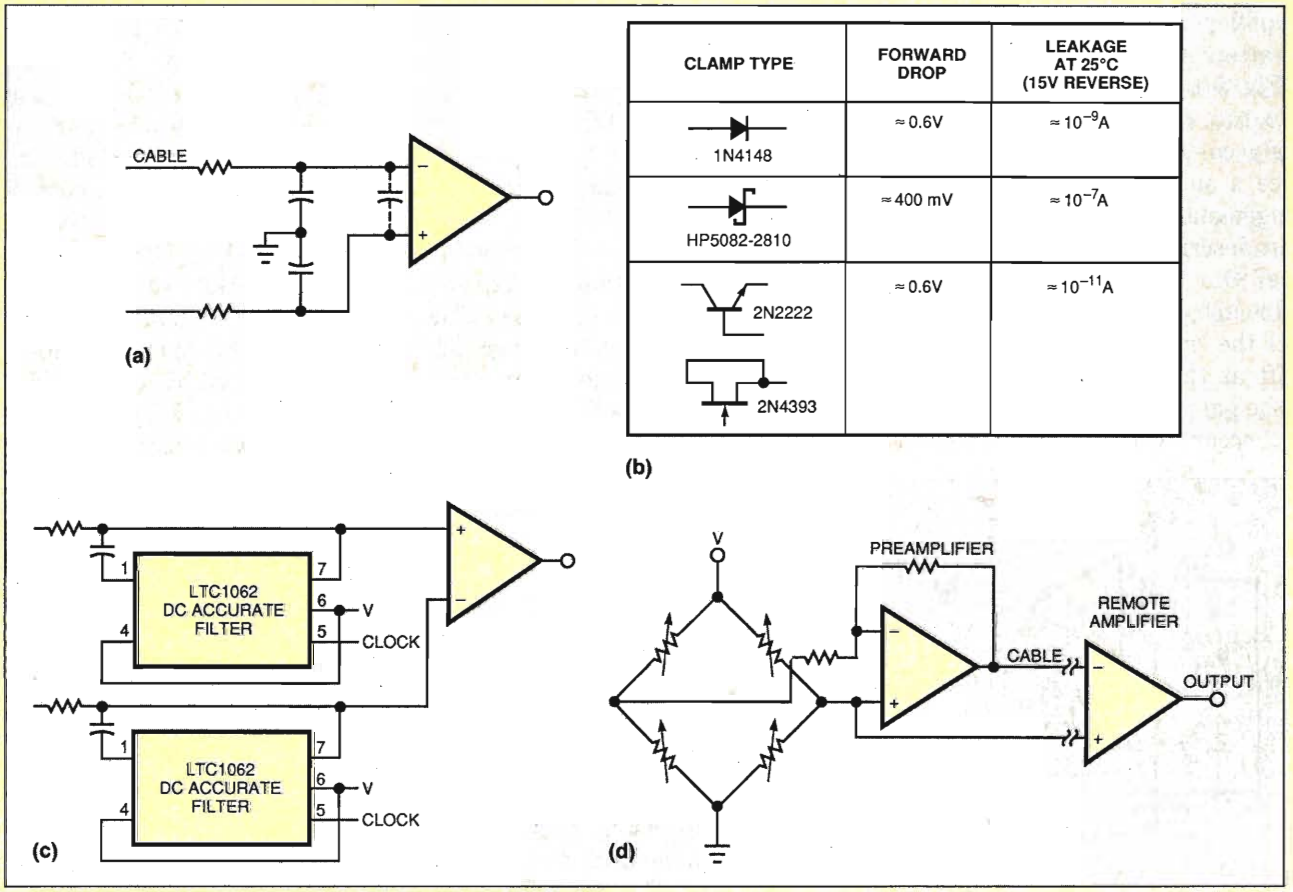


***Fig A—RC filters protect against input noise*** *when routing bridge outputs over long lengths of cable* ***(a)****. Diode clamps prevent high-voltage spikes from damaging the amplifier. The clamping characteristics depend on the device* ***(b)****. This switched-capacitor-based circuit uses fifth-order lowpass filter ICs that have no dc error* ***(c)****. Adding a preamplifier provides gain for the bridge's output signal and a low-impedance drive to the cable* ***(d)****.*

*Some ac-based bridge circuits, such as those used for capacitance measurements, work in the time domain rather than the frequency domain.*

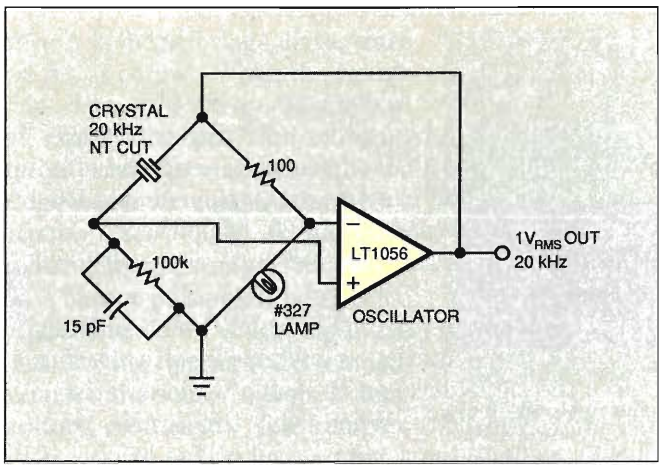


***Fig 8—Offering better linearity than the Fig 7 circuit,*** *this crystal-controlled oscillator uses the current variations in a small lamp to stabilize amplitude variations.*

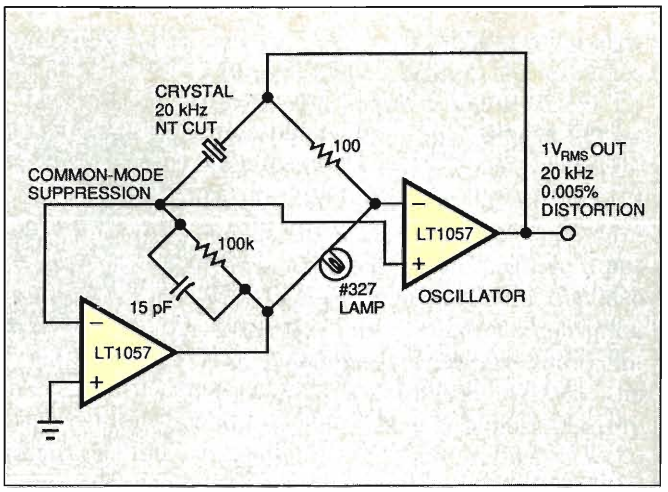


***Fig 9—Similar to the Fig 8 circuit,*** *this oscillator adds a second amplifier stage to provide common-mode suppression.*

amplifier repeatedly overshoots in its attempts to null the bridge.

**Fig 8** takes the previous circuit into the linear region by continuously controlling the gain to produce a sine-wave output. This arrangement uses a classic technique first described by Meacham in 1938 **(Ref 9)**.

In any oscillator, you must control the gain as well as the phase shift at the frequency of interest. If the gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting. In the **Fig 8** circuit, the positive temperature coefficient of the lamp controls the gain. When power is applied, the lamp is at a low-resistance value, the gain is high, and the oscillation amplitude builds. As the amplitude builds, the lamp current increases, heating occurs, and the lamp's resistance increases. The increased resistance reduces the amplifier gain, and the circuit finds a stable operating point. The 15-pF capacitor suppresses spurious oscillation.

As a result of this stabilizing action, the amplifier's output is a sine wave with approximately 1.5% distortion. This relatively high distortion is primarily caused by the common-mode swing seen by the amplifier. Op-amp common-mode rejection suffers at high frequencies, thus distorting the output. The **Fig 9** circuit eliminates the common-mode swing by using a second amplifier to force the bridge's midpoint to virtual ground. It measures the midpoint value, compares it to ground, and maintains the input of the formerly grounded end at zero. Because the bridge drive is complementary, the oscillator amplifier does not see any common-mode swing, which dramatically reduces distortion to less than 0.005%.

Crystals are not the only resonant elements a gain-controlled bridge can stabilize. The oscillator circuit of **Fig 10** uses a Wien bridge; the configuration was originally developed for telephony applications. The circuit is a modern adaptation of one described by a Stanford University student, William R Hewlett, in his 1939 master's thesis (see **box,** "The Wien Bridge and Mr Hewlett").

In the **Fig 10** circuit, the Wien-bridge network provides phase shift, and the lamp regulates the amplitude of the oscillations. The smooth, limiting nature of the lamp's operation, in combination with its simplicity, gives good results. Harmonic distortion is below 0.003%. Most of the distortion is caused by second-harmonic content and some crossover disturbance. The low values of resistance in the Wien network and the 3.8-nV/$\sqrt{\text{Hz}}$ noise specification of the LT1037 eliminate amplifier noise as an error term.

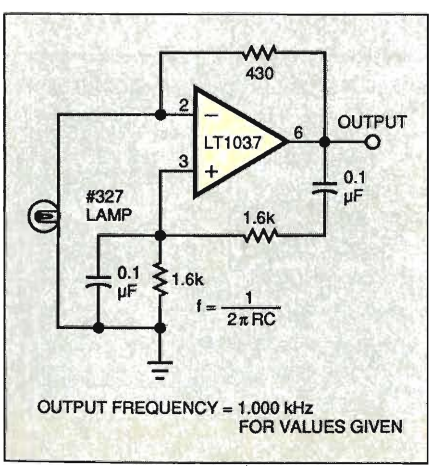


***Fig 10—Based on the Wien bridge,*** *this oscillator circuit generates low-distortion sine waves.*

At low frequencies, the thermal time constant of the small lamp begins to introduce distortion levels above 0.01%. The distortion is caused by a hunting effect as the oscillator's frequency approaches the lamp's thermal time constant. You can eliminate this effect by using more or larger lamps—but at the expense of reduced output amplitude and longer settling time.

The **Fig 11** circuit replaces the lamp with an electronic amplitude-stabilization loop. The LT1055 compares the oscillator's positive output peaks with a dc reference. The diode in series with the LT1004 reference provides temperature compensation for the rectifier diode. The op amp biases $Q_1$, controlling the FET's channel resistance and influencing loop gain, which is reflected in the oscillator's output amplitude. Loop closure around the

## The Wien bridge and Mr Hewlett

The Wien bridge is the most popular basis for constructing sine-wave oscillators. Circuits constructed around the Wien network offer simplicity, wide dynamic range, ease of tuning, amplitude stability, and low distortion. Wien described his network **(Fig Aa)** in 1891. Unfortunately, he had no source of electronic gain and couldn't have made the network oscillate even if he wanted to. Wien developed the network for ac bridge measurement and only used it for that purpose.

Forty-eight years later, William R Hewlett combined Wien's network with controlled electronic gain for his masters thesis. The results were the now familiar Wien bridge-oscillator architecture and the Hewlett-Packard Company. Hewlett's circuit **(Fig Ab)** utilized the relatively new concepts of feedback theory to control oscillation. The circuit used two feedback loops; one to generate the oscillations and a second to maintain stability.

A positive-feedback loop from the amplifier's output (the plate of the 6F6) back to its positive input (the control grid of the 6J7) via the Wien bridge provides circuit oscillation. A second, negative-feedback loop stabilizes the oscillations. This loop is closed from the output (again, the plate of the 6F6) back to the amplifier's negative input (the cathode of the 6J7). The now famous lamp supplied a slight positive temperature coefficient to maintain gain at the proper value.

For reference in interpreting the vacuum-tube configuration, look at a modern version of Hewlett's circuit **(Fig Ac)**. Most contemporary oscillators replace the lamp's action with an electronic equivalent to control the loop's settling time.

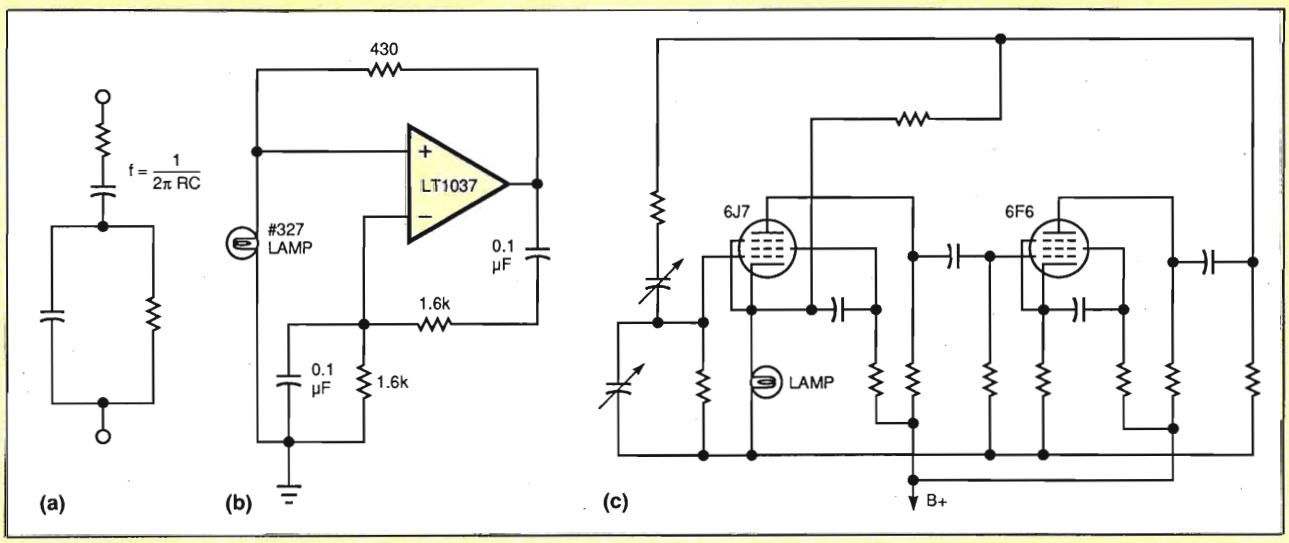


***Fig A—Wien developed his original network*** *for use in ac bridge measurements* ***(a).*** *William Hewlett's Wein-bridge oscillator circuit* ***(b)*** *used pentode vacuum tubes (Figure courtesy Stanford University archives). A modern version of Hewlett's circuit used a low-noise precision op amp* ***(c).***

*Replacing one of the bridge arms in an oscillator circuit with a quartz crystal provides more accurate frequency control.*

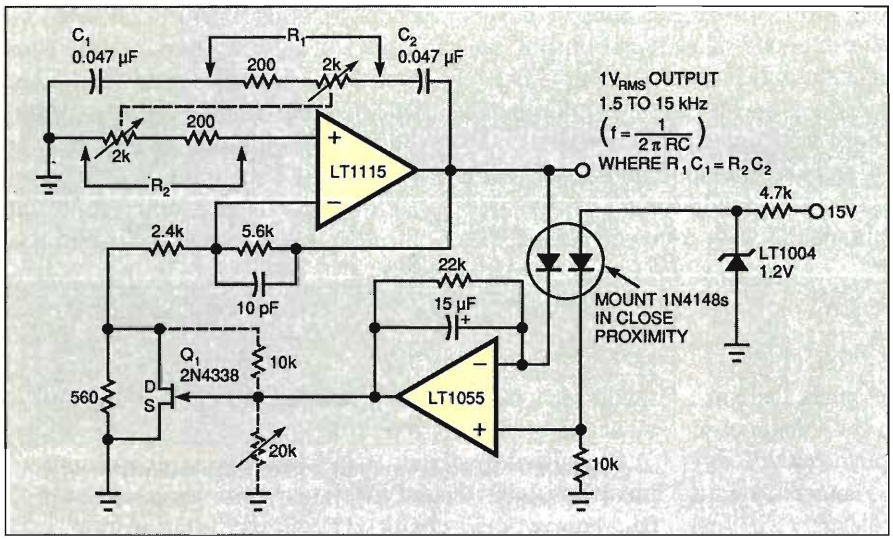


***Fig 11—This oscillator circuit replaces the lamp*** *in the traditional Wien bridge with an electronic equivalent.*

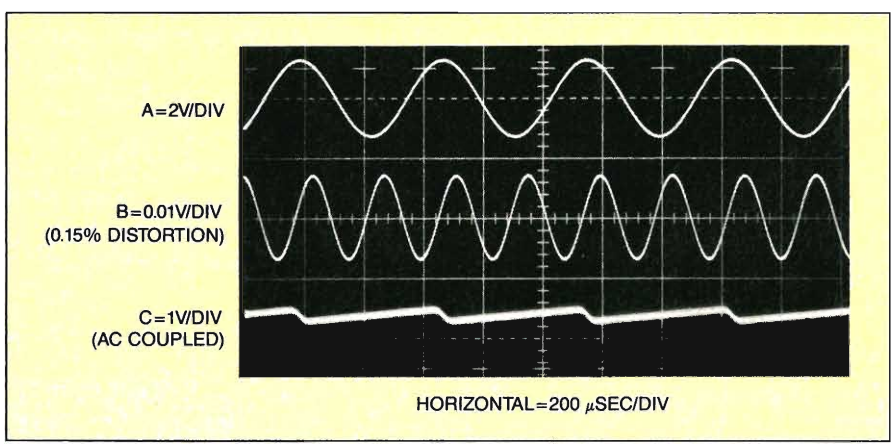


***Fig 12—These waveforms for the circuit of Fig 11*** *show excessive distortion caused by modulating the FET's channel resistance. A 0.15% second-harmonic distortion (trace B) is present in the output (trace A). This distortion does not correlate with the rectifier-peaking residue present at $Q_1$'s gate (trace C).*

LT1055 occurs, which stabilizes the oscillator's amplitude. The 15-µF capacitor stabilizes the loop, and the 22-kΩ resistor settles its gain.

The distortion performance of this circuit is quite disappointing. **Fig 12** shows 0.15% second-harmonic distortion (trace B) in the output (trace A)—a huge increase over the lamp-based approach. This distortion does not correlate with the rectifier-peaking residue present at $Q_1$'s gate (trace C). What is the villain in this scheme?

The culprit is actually $Q_1$. In an FET, gate voltage theoretically sets the channel resistance. In fact, the channel voltage also slightly modulates the channel resistance. In this circuit, $Q_1$'s channel sees large swings at the fundamental frequency. This swing combines with the channel voltage-resistance modulation effect to produce distortion.

The cure for this difficulty is local feedback around $Q_1$. Properly scaled, this feedback nicely cancels out the parasitic. The resistors shown in dashed lines provide the feedback. You adjust the 20-kΩ trimmer to minimize distortion. Distortion products, which include the second harmonic, rectification artifacts and noise, now drop to 0.0018%.

The Wien-bridge-based circuit of **Fig 13** uses a common-mode suppression technique to reduce distortion to vanishingly small levels. The LT1022 amplifier forces the midpoint of the bridge to virtual ground by servo biasing the formerly grounded bridge legs of **Fig 11**'s circuit. This action eliminates common-mode swing and reduces distortion.

Compared with the **Fig 11** circuit, the **Fig 13** circuit provides increased voltage and current output. In addition, this circuit replaces $Q_1$ with an optically driven CdS photocell, which has no parasitic resistance-modulation effects. A ground-sensing op amp running in a single-supply mode replaces **Fig 11**'s LT1055. This arrangement permits true integrator operation and eliminates any possibility of reverse biasing the downsized feedback capacitor. Additional feedback components aid step response. The circuit's output contains less than 0.0003% distortion, a level that is below the uncertainty floor of most distortion analyzers and requires specialized equipment to measure meaningfully (see **box,** "Understanding distortion measurements," pg 240).

Although this 2-part series has covered a wide range of bridge circuits and signal-conditioning methods, many other possibilities exist. An application note derived from

*Most contemporary Wien-bridge oscillator circuits replace the traditional lamp with an electronic equivalent.*

this manuscript is available from Linear Technology Corp (Milpitas, CA). Application note No. 43, "Bridge Circuits—Marrying Gain and Balance," contains several additional circuits as well as more extensive supplementary material.

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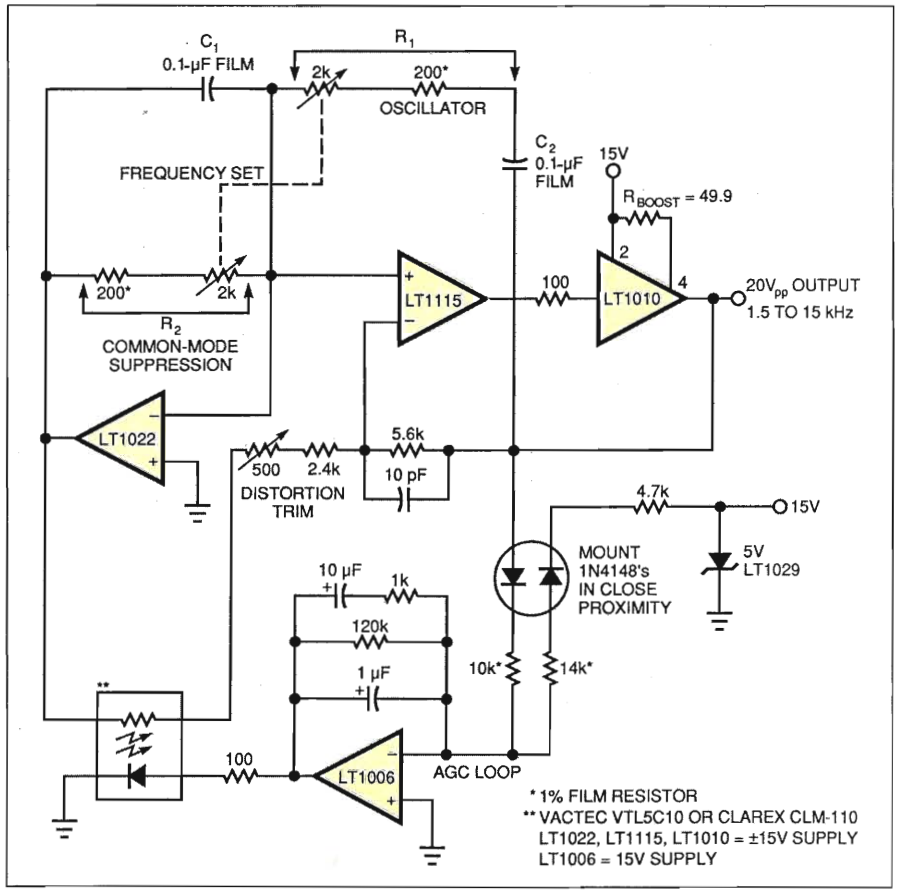


***Fig 13—This complex oscillator circuit*** *uses a photocell and common-mode-suppression circuitry to achieve distortion of 0.0003%.*

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## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

## Understanding distortion measurements

Any effect or process that causes an analog signal to deviate from an ideal condition creates distortion. The term distortion can mean significantly different things to different people, so it's important to distinguish between the two general categories, linear and nonlinear, before concentrating on the measurement and meaning of nonlinear distortion.

Linear distortion changes the amplitude and phase relationship between the existing spectral components of a signal without adding new components. Frequency- and phase-response errors are the most common examples. Both types can significantly alter the time-domain waveform.

Nonlinear distortion adds frequency components to the signal that were not originally present. Nonlinear distortion alters both the time- and frequency-domain representations of a signal. For example, noise is often a source of nonlinear distortion.

In general, nonlinear distortion is more serious than linear distortion because determining if a specific frequency component in the output signal was present in the input signal is impossible.

### Measures of distortion

One of the best and oldest methods of qualifying distortion is to excite a circuit or system with a relatively pure sine wave and analyze the output for the presence of signal components at frequencies other than that of the input sine wave. The sine wave is an ideal test signal for measuring nonlinear distortion because it is virtually immune to linear forms of distortion. With the exception of a perfectly tuned notch filter, the output of a sine wave after any linear distortion process will still be a sine wave.

Nth harmonic distortion is the amplitude of any output signal at exactly N times the frequency of the sine-wave fundamental. If the input sine wave is 400 Hz, any second-harmonic distortion will show up at 800 Hz, third harmonic at 1200 Hz, and so on. Spectrum analyzers, wave analyzers, and FFT analyzers are the typical instruments used to measure harmonic distortion. These instruments function by acting as highly selective voltmeters that measure the signal amplitude over an extremely narrow bandwidth centered at a specific frequency.

THD, or total harmonic distortion, is the rms summation of the amplitudes of all possible harmonics. In some cases, the definition is restricted to include only the second through the fifth harmonics. However, assuming that higher-order harmonic content is insignificant in the computation of THD can be quite invalid. The sine-wave distortion of many function generators is dominated by high-order harmonic products with only relatively small amounts of products below the fifth harmonic. The crossover distortion characteristic of class AB and B amplifiers can often exhibit significant harmonic content above the fifth order.

A far better definition of THD includes all harmonics up to some prescribed frequency limit. Usually the specific application will suggest a relevant harmonic-frequency limit. In audio circuits, this frequency limit might be 20 or 25 kHz because few people can perceive signals above that limit. In practice, using a somewhat higher limit (typically 80 kHz) is usually desirable because nonlinear distortion products above 20 kHz can provoke intermodulation problems in subsequent audio stages. In the world of FM and TV broadcast measurements, using a 30-kHz bandwidth limit is common practice even though the signals are inherently limited to 15 kHz.

THD + N, or total harmonic distortion plus noise, is the rms summation of all signal components, excluding the fundamental, over some prescribed bandwidth. Distortion analyzers make this measurement by removing the fundamental sine wave with a notch filter and measuring the leftover signal. Unfortunately, some popular analyzers have excessive measurement bandwidth greater than 1 MHz) with no provision for limiting. For the vast majority of applications, a measurement bandwidth of greater than 500 kHz serves little purpose other than to increase noise contribution and sensitivity to AM radio stations. Better distortion analyzers offer a selection of measurement bandwidths, which typically include 20, 30, and 80 kHz, as well as wideband (300 to 500 kHz).

At first glance, you might think that THD + N measurements are inferior to THD-only measurements because of their sensitivity to wideband noise. Even with their noise contribution, distortion analyzers offer the lowest residual distortion compared with other analyzers, and hence the most accuracy for making ultralow distortion measurements. At least one manufacturer of distortion analyzers claims a typical distortion figure of 0.0001%. The typical residual contribution of spectrum analyzers is usually limited by their internal mixer stages to about

0.003% (−90 dB). FFT analyzers do not fare much better because of A/D converter nonlinearities. The best 16-bit converters have a residual distortion of about 0.002%.

IMD, or intermodulation distortion, is yet another parameter for quantifying nonlinearity. The specialized IMD tests require a multitone test signal. IMD tests are often more sensitive than THD or THD + N tests because you can choose the test frequencies and the analyzer measurement technique to optimize response to certain forms of nonlinearity. These options are also one of the biggest disadvantages of IMD testing because of the many corresponding test standards: SMPTE, CCIF, TIM, DIM, and MTM, to name a few.

Nonlinear distortion is not a traceable characteristic in the sense that you can make an unbroken chain of comparisons to a truly distortionless standard. Such a standard does not exist. Real-world distortion measurements will always include nonzero contributions from both the sine-wave source and the analyzer.

Accurately measuring distortion below approximately 0.01% (−80 dB) is a truly challenging task. Distortion measurement errors can become quite large near residual levels. Harmonic contributions from the original sine wave and the analyzer can add algebraically, vectorially, or even cancel, depending on their relative phases. In short, making general assumptions regarding how two residual contributions will add or subtract is not possible.

A typical example illustrates how the residual distortion of the analyzer influences the measured distortion. In the following equation, M is the measured value of the Nth harmonic, X is the magnitude of the distortion contributed by the analyzer, and D is the true distortion magnitude of some signal.

$$M \cdot \sin(N\omega t + \phi) = D \cdot \sin(N\omega t) + X \cdot \sin(N\omega t + \Theta).$$

If the phase angle ($\Theta$) is 0°, $M = D + X$; if $\Theta$ is ±90°, $M = \sqrt{D^2 + X^2}$; if $\Theta$ is 180°, $M = D - X$.

Depending on the relative phase between the distortion components ($\Theta$), a true distortion factor (D) of 0.0040% could be read as anything between 0.0025% to 0.0055% if the analyzer's internal distortion contribution (X) was 0.0015%. Conversely, a 0.0040% reading could have resulted from a true distortion factor of 0.0025% to 0.0055% with the same 0.0015% analyzer contribution.

You should understand this concept when making distortion readings near the specified residual levels of the test equipment. A low reading may not always signify lower distortion; it could be the result of a fortuitous cancellation of two larger contributions. Concluding that the true value of distortion is always less than the reading is also illogical because of the nonzero residual contributions of the analyzer and sine wave.

All these distortion measurement techniques give 0.5- to 1.0-dB (5 to 10%) reading accuracies at high reading levels. Some distortion analyzers provide average vs true-rms detection. Average detection is a carryover from the past. You should avoid average detection because it will give erroneously low readings when multiple harmonics are present.

Both THD and THD + N are measures of signal impurity. Distortion analyzers measure THD + N, not THD. Spectrum, wave, and FFT analyzers measure individual harmonic distortion from which you can calculate THD, but not THD + N.

For most applications, THD + N is the more meaningful measurement because it quantifies total signal impurity. As we enter the age of A/D- and D/A-based systems (for example, digital audio) the engineer is increasingly confronted with effects and imperfections that introduce nonharmonic components to a signal. Wideband noise itself is an imperfection that calls for reduction. When determining signal quality, it is myopic to exclude potentially undesirable signal components just because they are not a harmonic of the test signal. If a 60-Hz component is acceptable when calculating 20-Hz THD it should be acceptable when testing with a 1-kHz fundamental.

Although THD + N measurements are generally more meaningful, THD-only measurements are distinctly better if you want to quantify a simple transfer function's nonlinearity. These simple forms of nonlinearity do not introduce noise, hum, or other interference products, and should not influence the measurement. Examples of these transfer functions include the distortion caused by component voltage-coefficient effects and non-ohmic contact behavior.

Given that all real signals contain some distortion, determining how much THD or THD + N is acceptable in a particular application is best left to the designer. —***Bruce E Hofer,*** *Audio Precision Inc*

# Transistor sensor needs no compensation

Jim Williams
*Linear Technology Corp, Milpitas, CA*

The thermometer circuit in **Fig 1** uses an inexpensive transistor to accurately measure temperature without compensation or calibration. Almost all transistor sensors use the base-emitter diode's voltage-shift with temperature as their sensing mechanism. Unfortunately, the *absolute* diode voltage is unpredictable, necessitating circuit calibration each time you fit a new transistor sensor.

The circuit in **Fig 1** overcomes this limitation. The circuit provides a 0-to-10V output corresponding to a 0-to-100°C input. Unadjusted error is $< \pm 1\%$.

The basis for the circuit is the predictable relationship between current and voltage in a transistor's $V_{BE}$ junction. At room temperature, the $V_{BE}$ junction diode shifts 59.16 mV per decade of current. The temperature dependence of this constant is 0.33%/°C, or 198 μV/°C. The $\Delta V_{BE}$-vs-current relationship holds, regardless of the $V_{BE}$ diode's *absolute* value.

An internal oscillator controls the state of the switches in $IC_1$, the LTC1043. The 0.01-μF capacitor at pin 16 sets the IC's oscillator frequency at about 500 Hz. $Q_1$ operates as a switched-value current source, alternating between about 10 and 100 μA as $IC_1$ commutates switch pins 12 and 14. The two currents' exact values are unimportant, so long as their *ratio* remains constant.

Because of this constant ratio, $Q_1$ requires no reference, although its emitter resistor's ratio must be precise. The alternating 10/100-μA stepped current drive

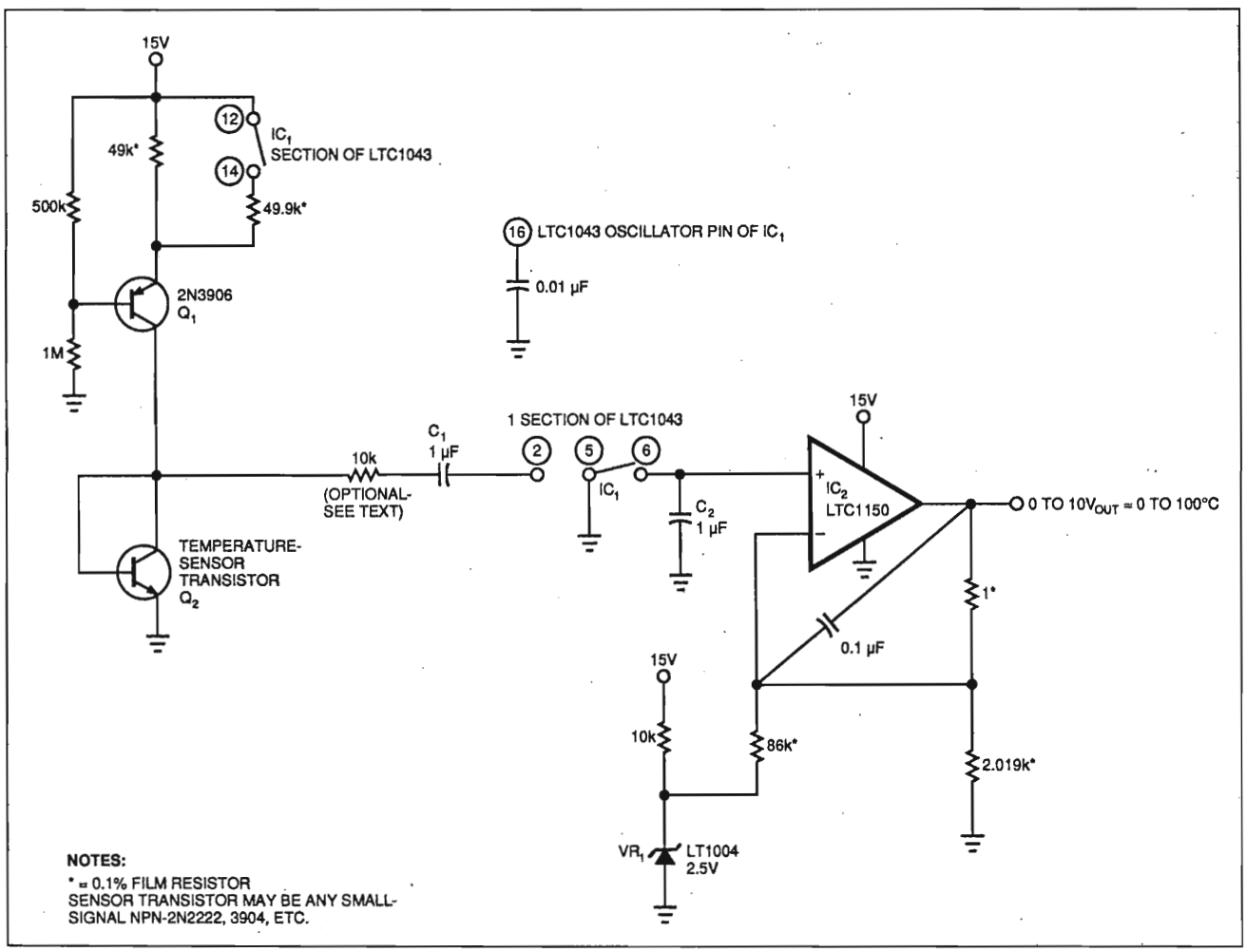


***Fig 1—The transistor $Q_2$ senses temperature.*** *This circuit requires no compensation, even if you change transistors.*

to the sensor transistor, $Q_2$, causes the theoretical 59.16-mV excursion at 25°C to appear across the $V_{BE}$ junction.

$C_1$ couples this signal to a switched demodulator that strips off $Q_2$'s dc bias. Thus $IC_1$'s pin 2 sees only the 59-mV waveform, which the demodulator action at pins 5 and 6 references to ground. Pin 5, connected to capacitor $C_2$, sits at pin 2's peak dc value. $IC_2$ amplifies this dc signal, with $VR_1$ providing offset so that 0°C equals 0V output. The optional 10-kΩ resistor protects against ESD (electrostatic discharge) events, which may occur if $Q_2$ is at the end of a cable.

Using the components in **Fig 1**, the circuit achieves ±1% error over a sensed 0-to-100°C range. Substituting randomly selected 2N3904s and 2N2222s for $Q_2$ showed less than 0.4°C spread over 25 devices from various manufacturers. **(EDN BBS /DI_SIG #945)**

EDN

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# Thermocouple conditioner draws μA

Jim Williams
*Linear Technology Corp*

This complete digital output, thermocouple signal conditioner (**Fig 1a**) produces a 0- to 1-kHz output in response to sensing a 0 to 100°C temperature excursion. The circuit includes cold-junction compensation, and accuracy is within 1°C with stable 0.1°C resolution. Additionally, the circuit operates from a single supply that can range from 4.75 to 10V. The circuit consumes a maximum of 360 μA.

The LT1025 provides an appropriately scaled cold-junction compensation voltage to the type K thermocouple. As a result, the voltage at point A in **Fig 1a** varies from 0 to 4.06 mV over a sensed 0 to 100°C range (type K thermocouples have a slope of 40.6 μV/°C). The remaining components form a voltage-to-frequency converter that directly converts this mV level signal without the usual dc gain stage. The thermocouple biases the negative input of $IC_1$, a chopper-stabilized op amp. $IC_1$'s output drives a crude V/F converter, comprised of $Q_2$, a series of 74C14 inverters,

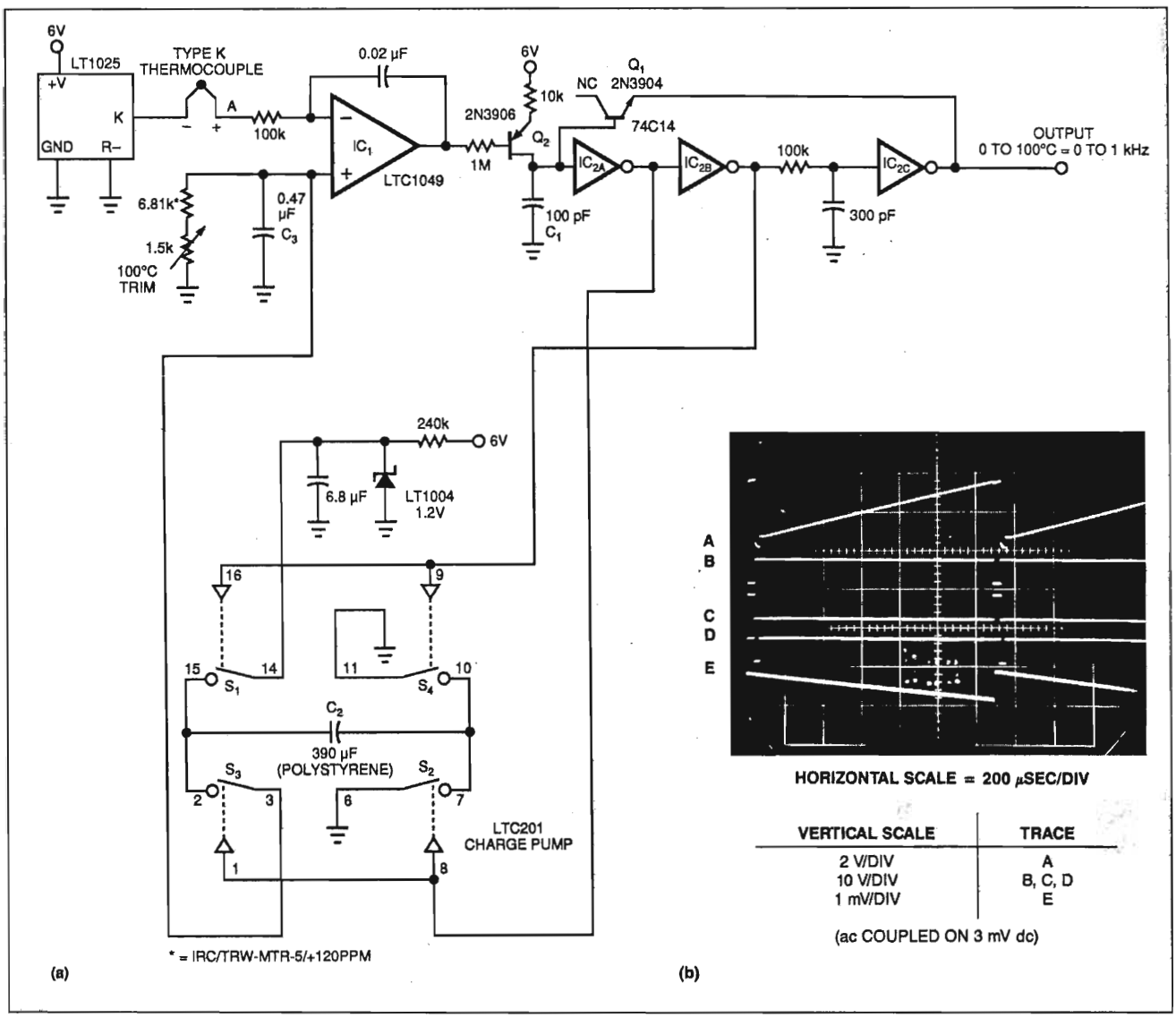


***Fig 1—This temperature-to-frequency converter (a) outputs** a signal with frequencies ranging from 0 to 1 kHz in response to temperatures between 0 and 100°C. The waveforms in **b** illustrate the circuit's operations at various points.*

and other associate components. Each V/F output pulse dispenses a fixed quantity of charge into $C_3$ from $C_2$ via the LTC201-based charge pump. $C_3$ integrates the charge packets, producing a voltage at $IC_1$'s positive input. $IC_1$'s output forces the V/F converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action eliminates error terms caused by drift and nonlinearities in the V/F converter. The output frequency is solely a function of the dc conditions at $IC_1$'s inputs. The 0.02-μF capacitor forms a dominant response pole at $IC_1$, which stabilizes the loop.

**Fig 1b** demonstrates the circuit's operation. $IC_1$'s output biases current source $Q_2$ producing a ramp (Trace A) across $C_1$. When the ramp crosses $IC_{2A}$'s threshold, the cascaded inverter chain switches, producing complementary outputs at $IC_{2A}$ (Trace B) and $IC_{2B}$ (Trace C). $IC_{2C}$'s RC delayed response (Trace D) turns on diode-connected $Q_1$, thereby discharging $C_1$ and resetting the ramp. The ramp aberrations that occur just before the reset in Trace A are due to transient input current from $IC_{2A}$ during switching (near top of ramp). $Q_1$'s $V_{BE}$ diode rounding and reverse-charge transfer (bottom of ramp) account for the discontinuities during the ramp's low point.

The complementary inverter outputs from $IC_{2A}$ and $IC_{2B}$ clock the LTC201 switched-based charge pump. $S_1$ and $S_4$ alternately charge $C_2$ to the LT1004's reference voltage. $C_2$ discharges into $C_3$ through $S_2$ and $S_3$. Each time this cycle occurs, $C_3$'s voltage is forced up (Trace E). $C_3$'s average voltage is set by the 6.81k and 1.5k resistors in parallel with it. $IC_1$ servo controls the repetition rate of the V/F converter to bring its inputs to the same value, closing the control loop.

To calibrate this circuit, disconnect the thermocouple and drive point A with 4.06 mV. Next, set the 1.5k potentiometer for exactly a 1-kHz output. Connect the thermocouple, and the circuit is ready for use. If you have to replace the thermocouple, recalibration isn't necessary. Also note that this circuit can directly digitize any mV-level signal by deleting the LT1025/ thermocouple pair and directly driving point A.

**(EDN BBS /DL_SIG #960)** EDN

THE JIM WILLIAMS PAPERS

# Correcting power-supply problems

To ensure proper operation of circuits that use high-speed op amps, you need to pay careful attention to power-supply bypassing. Of equal importance are layout techniques and the need to establish a proper ground plane.

Jim Williams, *Linear Technology Corp*

Two of the most common problems encountered in any circuit design that uses high-speed op amps are those of power-supply bypassing and pc-board layout techniques. Of these two problems, power-supply bypassing is by far the most common. Bypassing is necessary to maintain a low supply impedance. Any dc resistance or inductance in supply wires and pc-board traces can quickly raise this impedance to unacceptable levels. A high-impedance supply lets the supply voltage vary as the current levels of the devices connected to it change. Such a situation almost always causes unruly operation of the individual devices. Moreover, several devices connected to an unbypassed supply can "communicate" through the finite-supply impedances, causing erratic operating modes.

Bypass capacitors furnish a simple way to eliminate these problems by providing a local reservoir of energy at the device. A bypass capacitor acts like an electrical flywheel to keep supply impedance low at high frequencies. The choice of the type of capacitor to use for bypassing is a critical issue. **Fig 1** shows the output of an unbypassed amplifier driving a 100Ω load. The power supply the amplifier sees at its terminals has a high impedance at high frequencies. This impedance forms a voltage divider with the amplifier and its load, letting the supply move as internal conditions in the amplifier change. As shown, this action causes local feedback, and oscillation occurs. Therefore, always use bypass capacitors at appropriate supply-rail points.

In **Fig 2** the 100Ω load is removed, and the amplifier

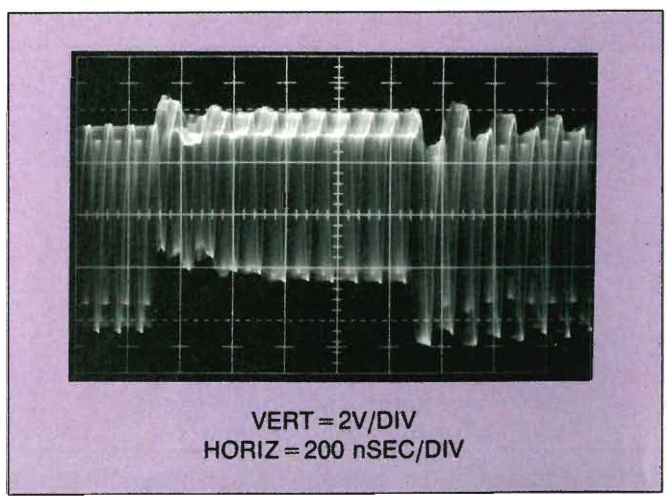


***Fig 1—The output of an amplifier*** *drives a 100Ω load without bypass capacitors.*

displays a pulse output. The unbypassed amplifier responds surprisingly well, but overshoot and ringing dominate. Always use bypass capacitors to avoid overshoot and ringing. In **Fig 3**, the settling is noticeably better, but some ringing remains. This response is typical of lossy bypass capacitors, or good ones placed too far away from the amplifier. Use good quality, low-loss bypass capacitors, and place them as close to the amplifier as possible.

The multiple-time-constant ringing in **Fig 4** often indicates a poor grade of paralleled bypass capacitors or excessive trace length between the capacitors. Although paralleling capacitors of different characteristics is a good way to get wideband bypassing, you need to consider such action carefully. Resonant interaction between the capacitors can also cause such a waveform after a step input. This type of response is often aggravated by heavy amplifier loading. When paralleling bypass capacitors, plan the layout and breadboard with the units you plan to use in production.

**Fig 5** addresses a more subtle bypassing problem. The trace shows the last 40-mV excursion of a 5V step almost settling cleanly in 300 nsec. The slight overshoot is due to a loaded (500Ω) amplifier without quite enough bypassing. Increasing the total supply bypassing from 0.1 to 1 μF cured this problem. Use large-value paralleled bypass capacitors when you need very fast settling, particularly if the amplifier is heavily loaded, or sees fast load steps.

The problem of peaking on the leading and trailing corners (**Fig 6**) is typical of poor layout practice. Depicted here, a unity-gain inverter suffers from excessive trace area at the summing point. Only 2 pF of stray capacitance caused the peaking and ringing. Minimize trace area and stray capacitance at critical nodes. Consider layout as an integral part of the circuit, and plan it accordingly.

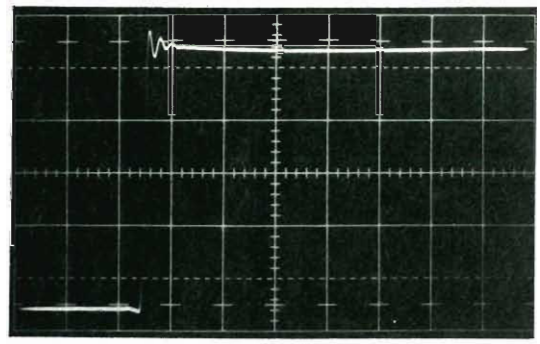


***Fig 3—A poor-quality bypass capacitor*** *allows some ringing in the amplifier's output.*

## About bypass capacitors

Bypass capacitors are used to maintain low power-supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power-supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing

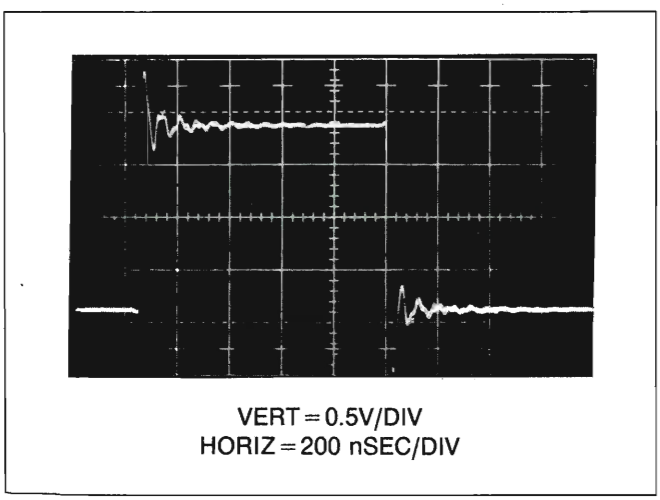


***Fig 2—An unbypassed amplifier with no load*** *can be surprisingly stable—temporarily.*

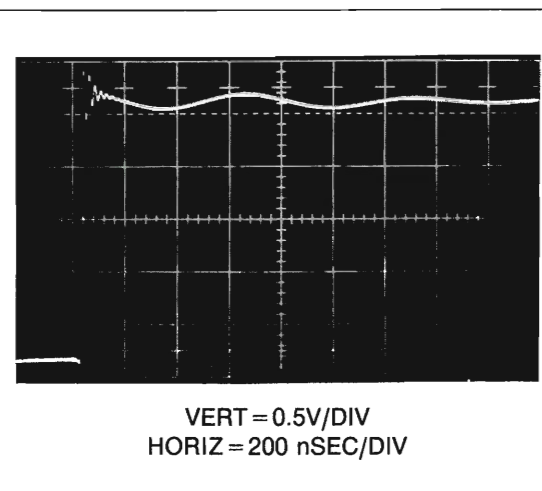


***Fig 4—Paralleled bypass capacitors*** *form a resonant network, which produces ringing.*

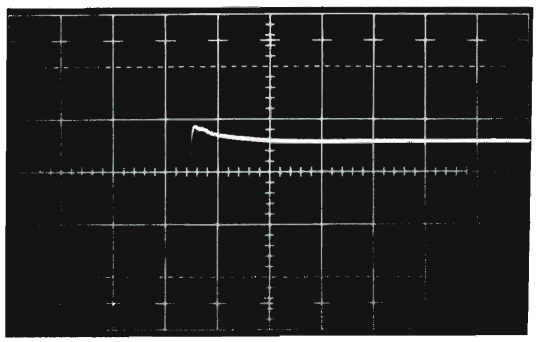


***Fig 5—This waveform shows a more subtle bypassing problem.*** *Not-quite-good-enough bypassing causes a few millivolts of peaking.*

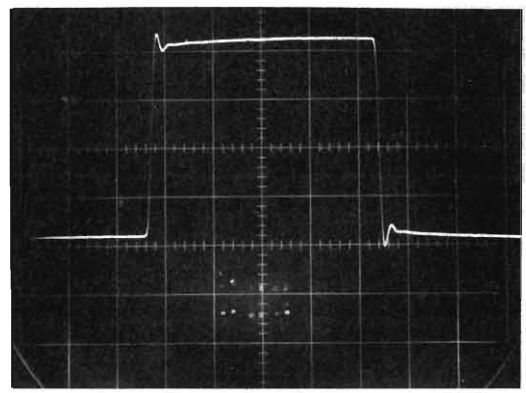


***Fig 6—This waveform is a typical result of poor layout.*** *Only 2 pF of capacitance at the summing point introduces peaking on the leading and trailing corners.*

is still necessary because no power supply or regulator has zero output impedance at 100 MHz. You determine the type of capacitor to use by its application, the frequency domain of the circuit, cost factors, board space, and many other considerations. It is possible, however, to make some useful generalizations.

All capacitors contain parasitic terms (some examples of which appear in **Fig 7**). In bypass applications, leakage and dielectric absorption are second-order terms, but series resistance (R) and inductance (L) are not. These latter terms limit the capacitor's ability to damp transients and maintain low power-supply impedance. Bypass capacitors must often be large in value to absorb long transients, necessitating electrolytic types that have large values of series R and L.

Different types of electrolytics and combinations of electrolytic and nonpolarized capacitors have markedly different characteristics. Which type (or types) to use is a matter of passionate debate in some circles. The test circuit of **Fig 8** and accompanying photos are useful in evaluating the choices. The photos show the response of five bypassing methods to the transient generated by the test circuit. **Fig 9a** shows an unbypassed line that sags and ripples badly at large amplitudes. **Fig 9b** uses a 10-μF aluminum electrolytic to considerably cut the disturbance, but there is still plenty of potential trouble. A 10-μF tantalum unit (**Fig 9c**) offers cleaner response, and the 10-μF aluminum electrolytic combined with a 0.01-μF ceramic type (**Fig 9d**) is even better. Combining electrolytics with nonpolarized ca-

## Acronyms used in this article

**air wire**—A connection from lead-to-lead without going to a specific terminal or point.
**BNC**—BNC coax connector. A twist-lock connector for various types of RG-type coaxial cables.
**DAC**—Digital-to-analog converter
**IC**—Integrated circuit
**pc board**—Printed-circuit board
**pc card**—Printed-circuit card

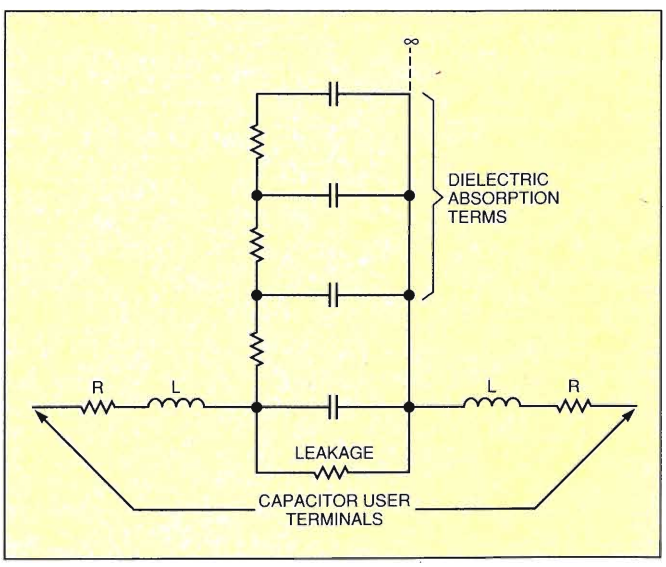


***Fig 7—All capacitors have parasitics.*** *In bypass applications, the series resistance (R) and inductance (L) limit the capacitor's ability to maintain a low supply impedance.*

pacitors is a popular way to get good response, but beware of picking the wrong pair. The wrong combination of supply-line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as illustrated in **Fig 10**.

### About ground planes

Similar to that resulting from a poorly grounded probe, the **Fig 11** waveform shows the result of not using a ground plane. A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (ac currents travel along the surface of a conductor) and covers the entire area of the board, a ground plane provides a way to access a low-inductance ground from

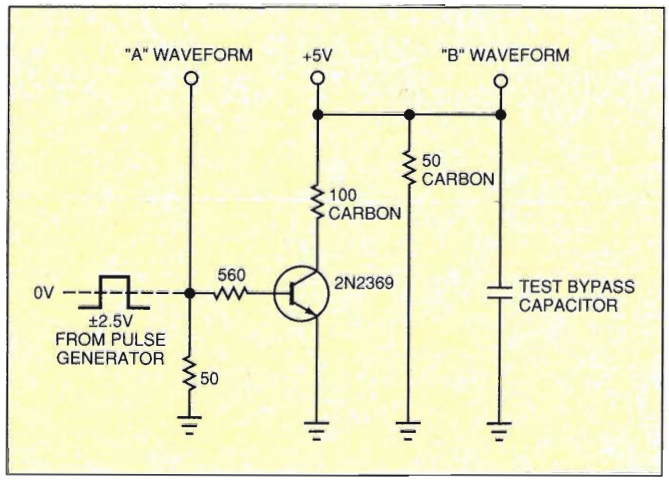


***Fig 8—This test circuit,*** *together with various types of bypass capacitors, produced the waveforms shown in* ***Figs 9a*** *through* ***d****.*

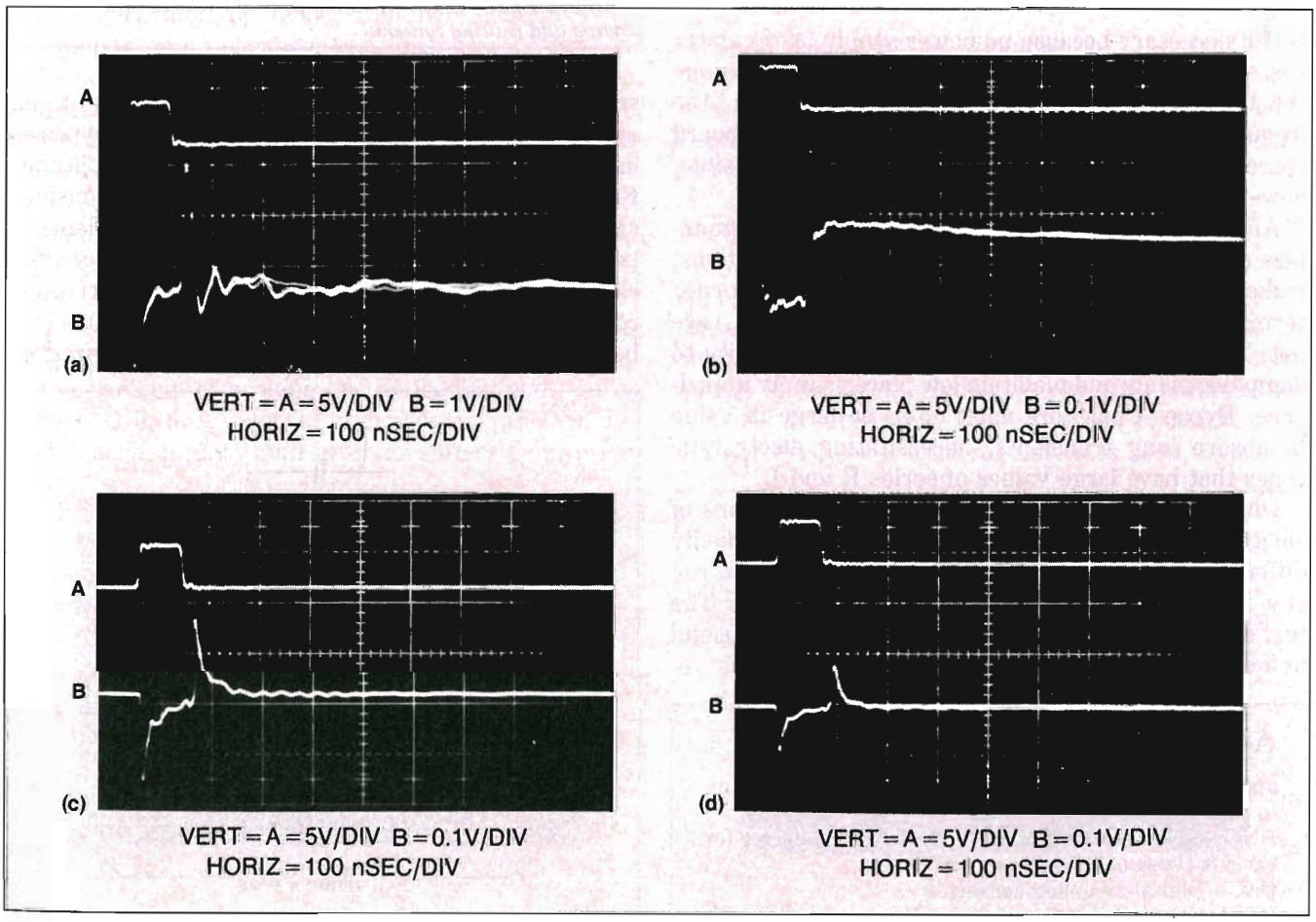


***Fig 9—The response of this unbypassed line*** **(a)** *sags and has a high ripple content. A 10-μF aluminum-electrolytic capacitor* (**b**) *somewhat reduces that disturbance. A 10-μF tantalum capacitor* (**c**) *offers cleaner response than that shown in* **b**. *Combining different capacitor types provides further improvement. A 10-μF aluminum capacitor and a 0.01-μF ceramic type* (**d**) *substantially smooth out the disturbance.*

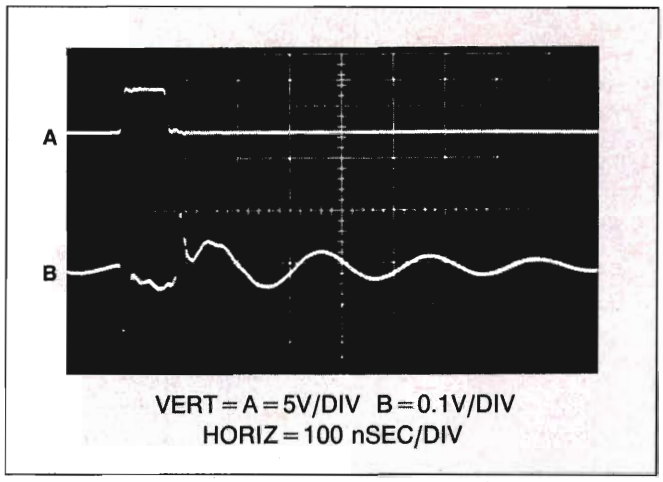


***Fig 10—Some paralleled combinations can cause ringing.*** *Always try various types before specifying.*

anywhere on the board. A ground plane also minimizes the effects of stray capacitance in the circuit by referring them to ground. This reference breaks up potential unintended and harmful feedback paths. Always use a ground plane with high-speed circuitry.

Although the term ground plane is often used as a mystical and ill-defined cure for spurious circuit operation, there is actually little mystery to the usefulness and operation of a ground plane. Like many phenomena, the operational principle of a ground plane is surprisingly simple.

As previously mentioned, ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a current-carrying wire (**Fig 12a**) surrounded by radii of a magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the current flowing through the wire. To compute the wire's inductance requires integrating the field over the wire's length and the total radial area of the field. This computation implies integrating on the radius from $R = R_W$ to infinity—a very large number. However, consider the case that **Fig 12b** illustrates, where two wires in space carry the same current in either direction. The fields produced cancel.

When the fields cancel, the inductance is much smaller than in the single-wire case and can be made arbitrarily small by reducing the distance between the two wires. This reduction of inductance between current-carrying conductors is the underlying reason for ground planes. In a normal circuit, the current path from the signal source, through its conductor and back to ground, includes a large loop area. This path produces a large inductance for the conductor and can cause ringing because of LRC effects. It is worth noting that, at 100 MHz, a 10-nH inductor has an impedance of 6Ω. At 10 mA, a 60-mV drop results.

A ground plane provides a return path directly under

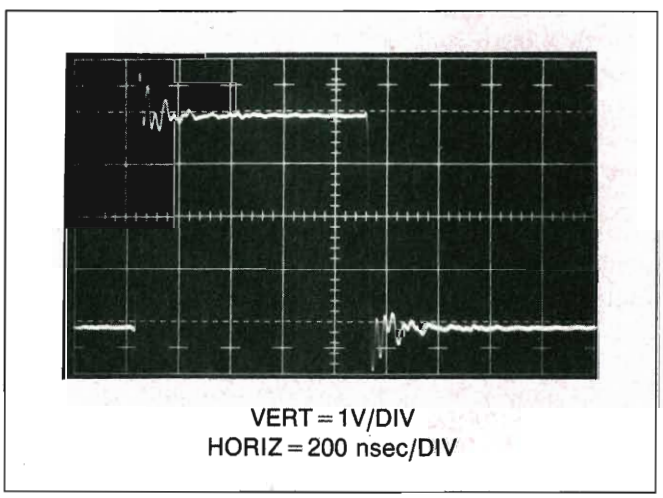


***Fig 11—Instabilities caused by the lack of a ground plane*** *can produce a result similar to that of a poorly grounded test probe.*

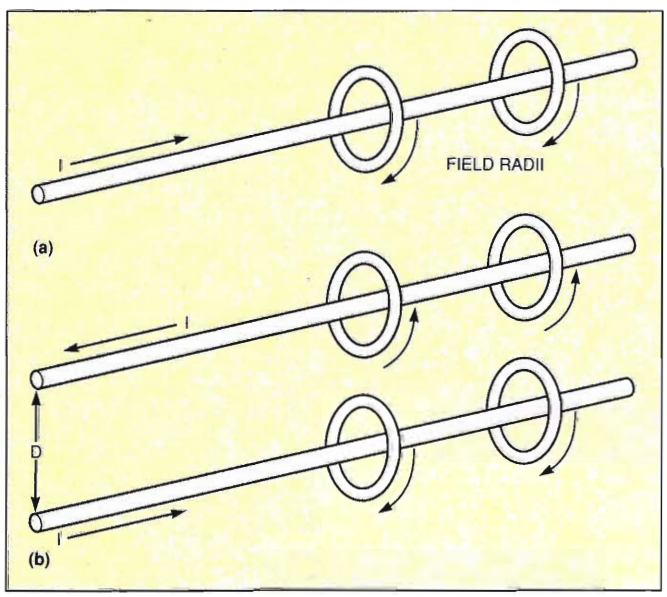


***Fig 12—A current-carrying wire*** *produces a magnetic field (***a***). Two wires in space, carrying the same current in opposite directions, produce a cancellation of the magnetic field (***b***).*

the signal-carrying conductor through which the return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Current will always flow through the return path of lowest impedance. In a properly designed ground plane, this path is directly under the signal conductor. In a practical circuit, it is desirable to "ground plane" one whole side of the pc card (usually the component side for wave-solder considerations) and run the signal conductors on the other side. This procedure will provide a low-inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to ac skin effects (ac currents travel along a conductor's surface). Moreover, ground planes aid the circuit's high-frequency stability by referring stray capacitances to ground.

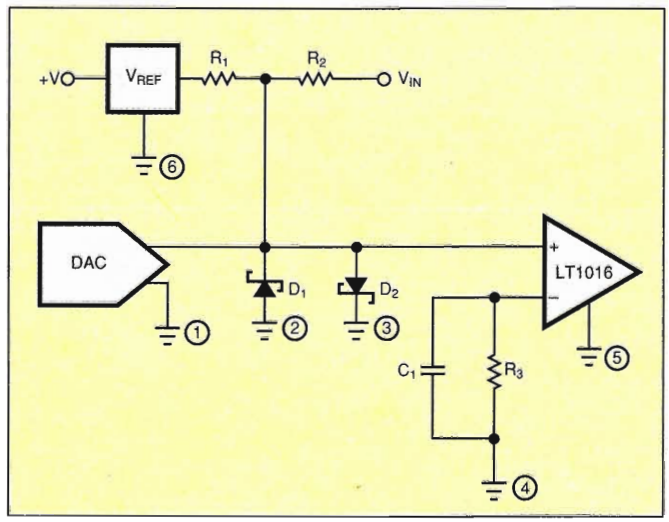


***Fig 13—In this combination analog-digital circuit**, good practice dictates that grounds 2, 3, 4, and 6 be as close to a single point as possible.*

### Practical hints for ground planes

The following guidelines are useful in the establishment and use of a ground plane.

- Ground-plane as much area as possible on the component side of the board, especially under traces that operate at high frequency.
- Mount components that conduct substantial fast-rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
- Where a common ground potential is important, such as at comparator inputs, try to connect the critical components to a single point in the ground plane to avoid voltage drops. For example, in **Fig 13**'s common DAC-comparator circuit, good practice dictates that grounds 2, 3, 4, and 6 be as close to a single point as possible. Fast, large currents flow through $R_1$, $R_2$, $D_1$, and $D_2$ during the DAC's settling time. Therefore, you should mount these components close to the ground plane to minimize their inductance. Because $R_3$ and $C_1$ don't carry any current, their inductance is less important; they could be vertically inserted to save space and to let point 4 be single-point common with 2, 3, and 6.
- In critical circuits, the designer must often trade off the beneficial effects of lowered inductance versus the loss of a single-point ground. In general, however, keep trace lengths short. Inductance varies directly with length, and no ground plane will achieve perfect cancellation.

Putting the guidelines for capacitor choices and the establishment of a proper ground plane to practical use usually starts with a breadboard. The breadboard is both the designer's playground and proving ground. It is there that reality resides, and where paper (or computer) designs meet their master. More than anything else, breadboarding is an iterative procedure, an odd amalgam of experience guiding an innocent, ignorant, explorative spirit. A key is to be willing to try things out, sometimes for not very good reasons. Invent problems and solutions, guess both carefully and wildly, throw rocks and see what comes loose. Invent and design experiments, and follow them wherever they lead. Reticence to try things is probably the number one cause of breadboards that don't work. Implementing the above approaches begins with the physical construction methods used to build the breadboard.

A breadboard for a high-speed circuit must start with a ground plane. In addition, bypassing, component layout, and connections should be consistent with high-speed operations. Because of these considerations, there is a common misconception that breadboarding high-speed circuits is time consuming and difficult. This is simply not true. You can assemble a complete and electrically correct breadboard for high-speed circuits of moderate complexity in 10 minutes if all necessary components are on hand. The key to rapid breadboarding is to identify critical circuit nodes and design the layout to suit them.

This procedure permits most of the breadboard's construction to be fairly sloppy, saving time and effort. Use all degrees of freedom in making connections and mounting components. Don't be bashful about bending IC pins to suit desired low-capacitance connections, or air-wiring components to achieve rapid or electrically optimum layout. Save time by using components, such as bypass capacitors, as mechanical supports for other components. It's true that printed-circuit construction is eventually required, but when initially breadboarding forget about pc boards and production constraints. Later, when the circuit works and is well understood, you can take care of pc-board adaptations.

The **Fig 14** amplifier circuit is a good working example of breadboarding techniques. This circuit is a high-impedance, wideband amplifier that has low-input capacitance. $Q_1$ and $IC_1$ form the high-frequency path, with the 900 to 100Ω feedback divider setting the gain. $IC_2$ and $Q_2$ close a dc stabilization loop, minimizing the dc offset between the circuit's input and output. Critical nodes in this circuit include $Q_1$'s gate (because of the desired low-input capacitance) and $IC_1$'s input-related connections (because of their high-speed operation). Note that the connections associated with $IC_2$ handle only dc, and are much less sensitive to layout. These determinations dominate the breadboard's construction.

**Fig 15a** shows the initial breadboard construction. The copper-clad board is equipped with banana-type connectors. The connector's mounting nuts are simply soldered to the board, securing the connectors. After adding $IC_1$ and the bypass capacitors (**Fig 15b**), observe that $IC_1$'s leads have been bent out. Bending the leads permits the amplifier to sit down on the ground plane, minimizing parasitic capacitance. Also, the bypass capacitors are soldered to the amplifier power pins right at the capacitor's body. The capacitor's leads are returned to the banana power jacks. This connection method provides good amplifier bypassing, while mechanically supporting the amplifier. It also eliminates separate wire runs to the power pins.

**Fig 15c** shows the addition of discrete components in the high-speed path. $Q_1$'s gate is connected directly to the BNC input socket, as is the 10-MΩ resistor associated with $IC_2$'s negative input. Note that the end of this resistor that sees a high frequency is cut very short, while the other end is left uncut. The 900 to 100Ω divider is installed at $IC_1$, with very short connections to $IC_1$'s negative input. $IC_1$'s 10-MΩ resistor receives similar treatment to that of the BNC-connected 10-MΩ resistor; the high-frequency end is cut short, while the end destined for connection to $IC_2$ remains uncut. $Q_2$'s collector and $Q_1$'s source, both high-speed points, are tied closely together with $IC_1$'s positive input.

Finally, dc amplifier $IC_2$ and its associated components are air-wired into the breadboard (**Fig 15d**). Their dc operation permits this, while the construction technique makes connections to the previously wired nodes easy. You can bend the previously uncommitted ends of the 10-MΩ resistors in any way necessary to make connections. All other components associated with $IC_2$ receive similar treatment, and the circuit is ready for experimentation.

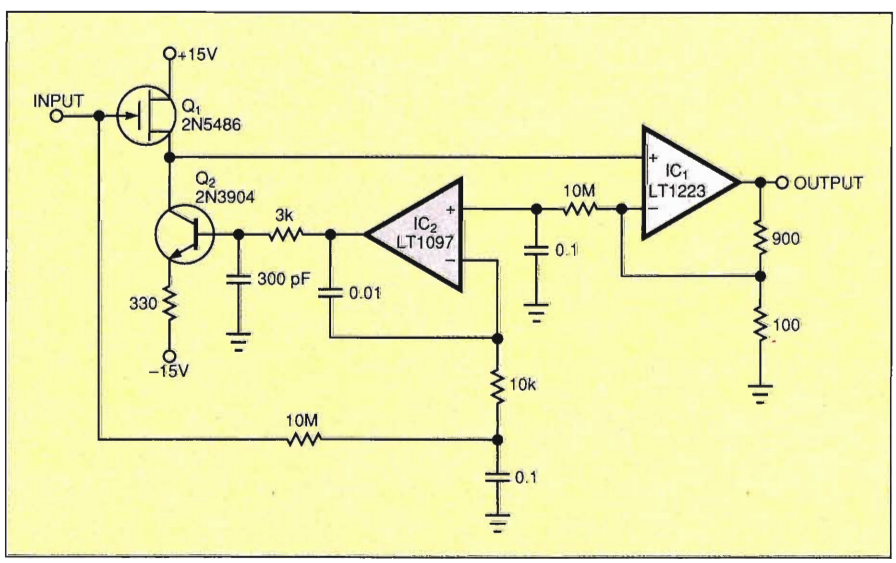


***Fig 14—This stabilized FET-input amplifier** is an example of the breadboarding techniques shown in **Fig 15a** through **d**.*

Despite the breadboard's seemingly haphazard construction, the circuit works well. Input capacitance measures a few pF (including the BNC connector), and bias current is about 100 pA. Slew rate is 1000 V/μsec, and the bandwidth approaches 100 MHz. Even with 50-mA loading, the output is clean, with no sign of oscillation or other instabilities.

Once the breadboard seems to work, it's useful to begin thinking about the pc-board layout and component choices for production. Experiment with the existing layout to determine just how sensitive nominally critical points are. Add controlled parasitic terms, such as resistors, capacitors, and physical layout changes, to test for sensitivity. Gentle touching of suspect points with a finger can yield preliminary indication of sensitivity, giving clues that can be quite valuable.

Finally, design the breadboard to be quick and easy to build, work with, and modify. Observe the circuit, and listen to what it is telling you before trying to get it the desired state. Don't hesitate to try just about anything; that's what the breadboard is for. Almost anything you do will cause some result—whether it's good or bad is almost irrelevant. Anything you do that enhances your ability to correlate events occurring on the breadboard can only be beneficial. EDN

## Author's biography

*For more information on this article's author, see pg 163 .*

Article Interest Quotient (Circle One)
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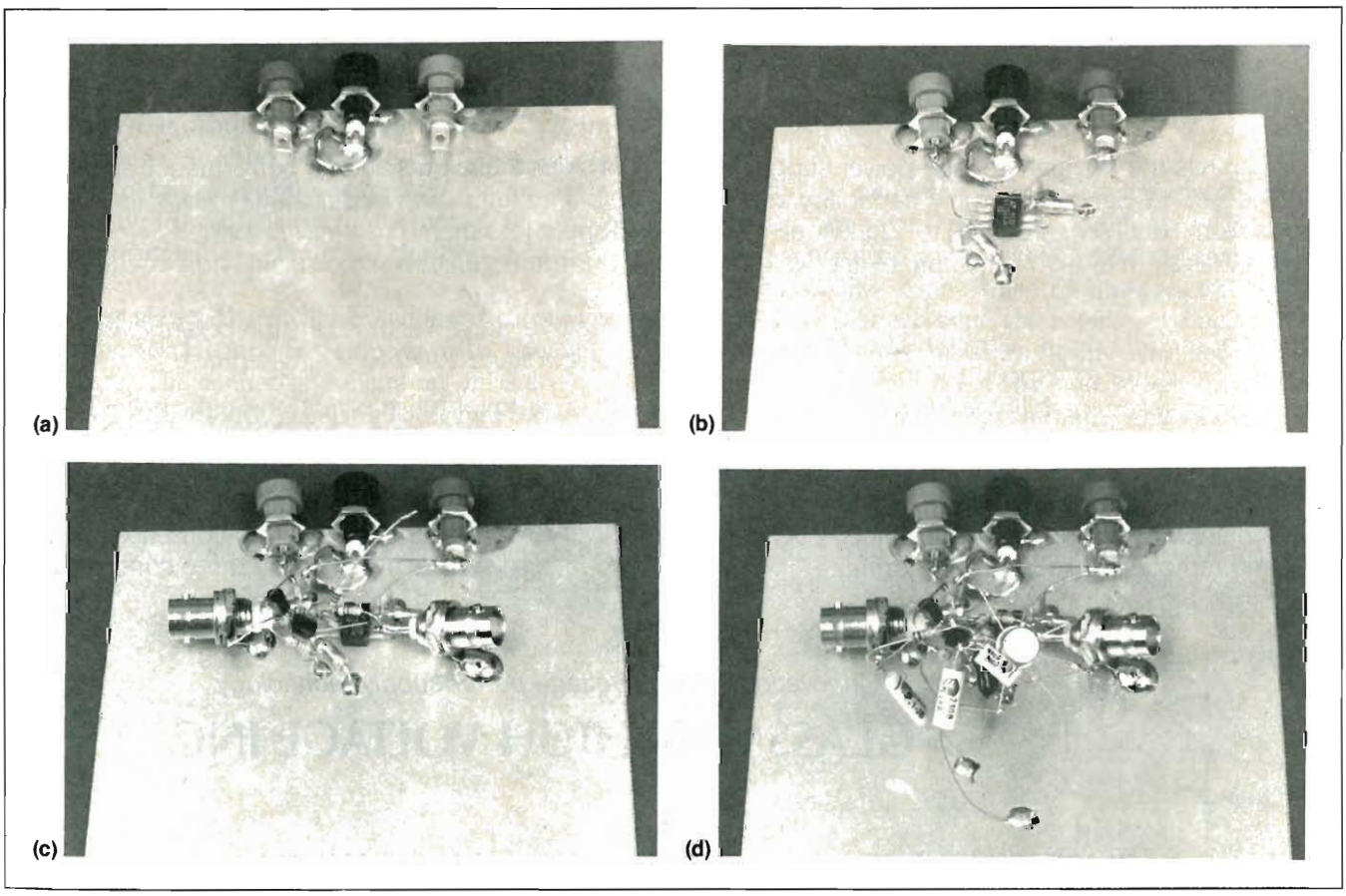



***Fig 15—In the initial breadboard construction (a),*** *banana jacks are soldered to a copper-clad board. With the addition of a high-speed amplifier, IC$_1$ (***b***), bypass capacitors provide support while the bent amplifier pins ease connections and minimize the distance to the ground plane. High-speed discrete components and BNC connectors are added to* **c**. *Note the short connections at the amplifier input pins (left side of package). The uncommitted ends of the 10-MΩ resistors are just visible. Finally, you wire the dc servo amplifier to complete the connections to the 10-MΩ resistors (***d***). This part of the circuit is not layout sensitive.*

# THE JIM WILLIAMS PAPERS

MOST ENGINEERS THINK designing analog circuits for high-frequency and high-speed applications is a black art known only to a few wizards. If you are among that majority, prepare to enter the sorcerers' inner circle. Jim Williams has pried loose the secrets of practical, high-speed analog design. By codifying his observations, he has moved high-speed analog design away from the art realm and toward the engineering domain.

Williams presents his discoveries in the articles that follow. Each article is self-contained, so you won't have to read the first article to understand the second. He delves into the mysteries of power-supply bypassing, parasitic coupling, and compensation. He discusses ways to prevent amplifiers from oscillating, how to keep oscillators stable, and how to couple high-speed analog circuits to the digital world. He even discusses the problems you'll face when your analog circuits outperform your test equipment. In short, he tells you how to obtain full performance from your high-speed analog silicon.

Regarding this undertaking, Williams writes

*Even the most veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high-speed circuits can work only if you negotiate compromises with nature. Ignorance of or contempt for physical law is a direct route to frustration. Mother Nature laughs at dilettantes and dabblers. She crushes arrogance unknowingly.*

Over the past 15 years, the name Jim Williams has become synonymous with analog design in EDN. He published his first article in EDN on May 5, 1975, while teaching and conducting research at the Massachusetts Institute of Technology. In 1979, he started a 3-year stint as a linear designer at National Semiconductor Corp. Williams joined Linear Technology Corp (Milpitas, CA) in 1982 and continued to write innumerable articles about his designs, which today cover almost every analog function you can name.

Williams' devotion to the art of analog design drives his successful and unconventional career. Although he has no formal degree in engineering—Williams describes his experience with formal education as an incredible impedance mismatch—Williams was designing circuits, or in his words, "bumbling around circuits," long before he'd heard of calculus. Williams now describes himself as a floater. He spends about half of his time as a staff scientist doing what he's done for the last 15 years: designing circuits and writing about them. The rest of the time he's either acting as a mentor for engineers at his company or designing circuits for specific customers.

Despite working in the competitive business of selling semiconductors, Williams manages to balance the commercial aspirations of his employer while designing and writing about circuits that often include a competitor's device. You are about to read his latest opus—the product of one year's effort. These secrets didn't pry loose easily, and Williams has a mountain of breadboards for proof. EDN is proud of its long-standing relationship with Jim Williams and is proud to present a work of this caliber.

Illustration by John Schreck

THE JIM WILLIAMS PAPERS

# The mysteries of probing

Unless you master the mysteries of probing and oscillography, you'll be doomed to measuring the errors in your setup and oscilloscope, not the errors in your circuit.

Jim Williams, *Linear Technology Corp*

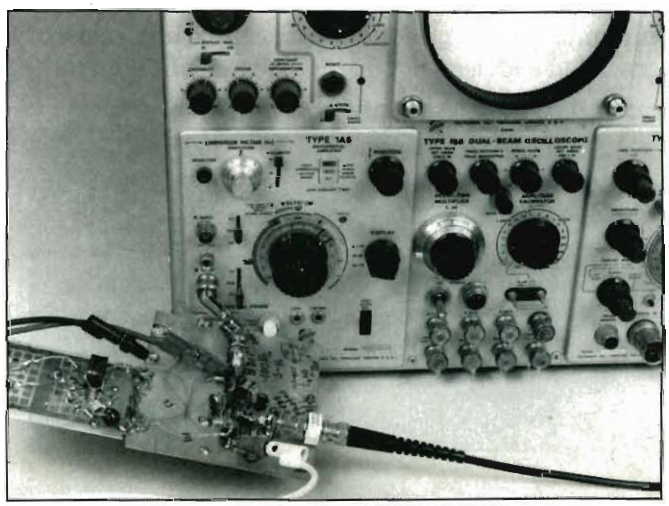
Measuring a high-speed linear circuit is a classic problem in observability. The problem is twofold: Stimulating and probing the circuit without disturbing its behavior and ensuring that the waveforms on your oscilloscope's screen are valid representations of your circuit's behavior. Problems can start before you apply power to your prototype.

Even something as simple as cabling requires thought. All coaxial cable is not the same. Always route high-speed signals to and from your circuit board with good-quality coaxial cable. Use cable appropriate to your system's characteristic impedance.

Poorly chosen cable materials or construction methods can introduce odd effects at very high speeds, resulting in distorted waveforms. A poor cable choice can adversely affect 0.01% settling in the 100- to 200-nsec region. Similarly, poor-quality cable can spoil even the cleanest pulse generator's 1-nsec rise time or purity. All too typically, inappropriate cable can introduce tailing, rise-time degradation, aberrations following transitions, nonlinear impedance, and other undesirable effects.

Other potential cabling problems begin at your circuit's input. The driven end of an input cable is usually an instrument (such as a pulse or signal generator), presumably endowed with proper characteristics by its manufacturer. The cable and its termination, selected by the experimenter, often cause problems.

**Fig 1a** shows severe ringing on the pulse edges at the output of an unterminated pulse-generator cable. Reflections cause this ringing and you can eliminate it by terminating the cable. Always terminate the source with its characteristic impedance when driving cable or long printed-circuit traces. In the high-speed



***One of the secrets of probing is that*** *sometimes the best probe is no probe. Oscilloscopes are so well designed that a 25-year-old scope suffices for 90% of today's applications.*

linear domain, any conductor longer than one inch is suspect.

In **Fig 1b** the cable is terminated, but ripple and aberration are still present following the high-speed edges. In this instance the terminating resistors' leads are lengthy (~¾ in.), sabotaging the wideband termination. The best terminating resistors for 50Ω cable are the BNC coaxial type. Their impedance vs frequency is flat into the GHz range. Although these terminators are practical on the test bench, they are rarely board-level components.

These coaxial terminators should not simply be resistors in an enclosure. Good grade, 50Ω terminators maintain true coaxial form. They use a carefully designed 50Ω resistor. The terminators' designers devoted significant effort to the connections to the actual resistive element. In particular, the terminators have the largest possible connection-surface area to minimize high-speed losses.

### Termination resistors

The best termination resistors for pc-boards are carbon or metal-film types having the shortest possible lead lengths. These resistors' "end-cap" connections provide better high-speed characteristics than the rod-connected composition types' connections. Wirewound resistors, because of their inherent, pronounced inductance, are completely unsuitable for high-speed work. This prohibition includes noninductive types of resistors.

Another termination consideration is disposing of the current flowing through the terminator. High-speed currents flowing from the terminating resistor's grounded end must not disrupt your circuit's operation. For example, returning terminator current to ground near the grounded positive input of an inverting op-amp would be unwise. The high-speed, high-density current flow could cause serious corruption of the op amp's reference. For example, 5V pulses through a 50Ω termination generate 100-mA current spikes.

This possible corruption is another reason why, for bench testing, the coaxial BNC terminators are preferable to discrete, breadboard-mounted resistors. In the coaxial types, the termination current returns directly to the source generator and never flows in the breadboard. Select terminations carefully, and evaluate the effects of their placement in your test setup.

**Figs 2a** and **2b** illustrate these terminators' performance nicely. In **Fig 2a**, a 1-GHz sampling scope (Tektronix 556 with 1S1 sampling plug-in and P6032 probe) monitors a 1-nsec pulse with 350-psec rise and fall times. The waveform is clean, with only a slight hint of ring after the falling edge. The setup used in **Fig 2a** is a high-grade BNC coaxial terminator. The setup in **Fig 2b** does not share these attributes. Rather, a 50Ω carbon-composition resistor with lead lengths of about ⅛ in. terminate the generator. The waveform rings and tails badly on turn-off before finally settling. Note that the sweep speed required a 2.5× reduction to capture these unwanted events.

Connectors, such as BNC barrel extensions and tee-type adapters, represent a discontinuity in the cable and can introduce small but undesirable effects. In general, you should use them as close as possible to a terminated point in the system. Using them in the middle of a cable run provides only minimal absorption of their mismatch and reflections.

The worst offenders among connectors are adapters.

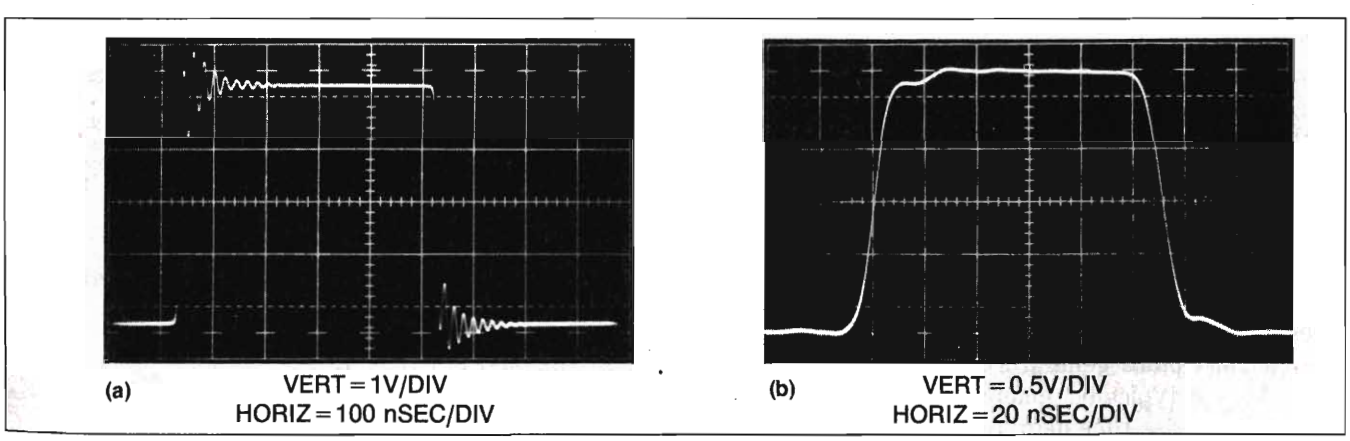



***Fig 1—In scope photo a,*** *an unterminated cable causes severe ringing. In* ***b,*** *improperly spec'ed termination resistors reduce, but do not eliminate, ringing.*

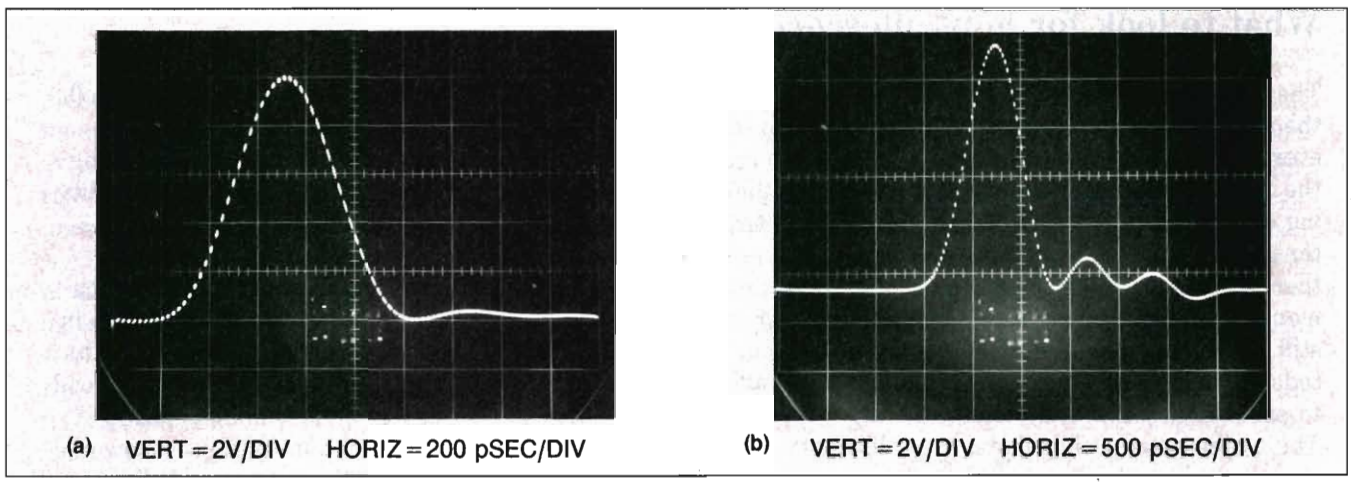



***Fig 2—Coaxial-termination resistors (a)*** *are superior in performance to carbon-composition resistors (**b**).*

The lack of standard connectors among wideband instrumentation makes this situation unfortunate. The mismatch caused by a BNC-to-GR874 adapter at the input of a wideband sampling scope is small, but clearly discernible on an oscilloscope. Similarly, you can readily measure mismatches in almost all adapters on a high-frequency network analyzer, such as the Hewlett-Packard 4195A—even in theoretically identical adapters of different manufacture. (For additional wisdom and terror along these lines, see **Ref 1**.)

BNC connections are easily the most common, but not necessarily the most desirable, wideband connectors. The ingenious GR874 connector has notably superior high-frequency characteristics, as does the type N. Unfortunately, it's a BNC world out there.

## Choosing the proper probe

After you find the type of connector that is best for your needs, you must choose a probe. Your oscilloscope's probe becomes an integral part of the circuit under test. Therefore, choosing which oscilloscope probe to use for a measurement is absolutely crucial.

Sometimes, however, the best probe is no probe at all. In some circumstances, connecting critical breadboard points directly to the oscilloscope is not only possible, but preferable. Connecting directly to critical breadboard points provides the highest possible grounding integrity, eliminates probe attenuation, and maintains bandwidth. In most cases, however, the direct connection is mechanically inconvenient, and often the oscilloscope's electrical characteristics (particularly input capacitance) will not permit it.

Of course, this mechanical inconvenience is why equipment makers developed oscilloscope probes in the first place, and why they have put so much effort into their probes' development. (**Ref 2** is an excellent reference for the designing of probes.)

Probes are the most overlooked source of oscillographic mismeasurement. The most obvious culprit is probes' input resistance, but input capacitance usually dominates in a high-speed measurement. You can lose much time chasing phantom circuit events that are actually caused by improperly selected or applied probes. Pay particular attention to the probe's input capacitance. Standard 10-MΩ, 10× probes typically have 8 to 10 pF of input capacitance, with 1× types having much higher input capacitance.

*Text continued on pg 170*

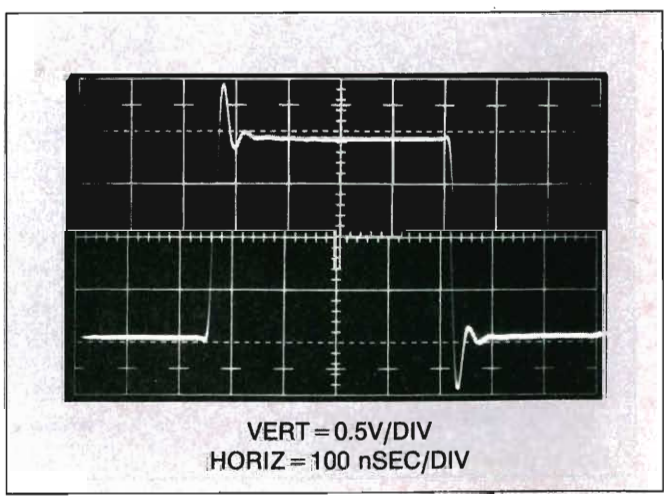



***Fig 3—The capacitance of a probe clipped*** *to another node in the circuit distorts this amplifier's response.*

## What to look for in oscilloscopes

The modern oscilloscope is one of the most remarkable instruments ever constructed. Perhaps only the zealotry devoted to timekeeping equals the protracted and intense development devoted to these machines. That instruments manufactured 25 years ago still suffice for more than 90% of today's measurements is a tribute to past oscilloscope designers. The oscilloscope-probe combination you select for your high-speed work is the most important equipment decision you can make.

Ideally, your oscilloscope should have at least 150-MHz bandwidth, but slower instruments are acceptable if you understand their limitations. Be certain of the characteristics of your probe-oscilloscope combination. You must keep rise time, bandwidth, resistive and capacitive loading, delay, noise, channel-to-channel feedthrough, overdrive recovery, sweep nonlinearity, triggering, accuracy, and other limitations in mind. High-speed linear circuitry demands a great deal from test equipment, and you can save yourself countless hours by knowing your instruments well.

Engineers have wasted obscene amounts of time pursuing "circuit problems" that in reality arose from misunderstood, misapplied, or out-of-spec equipment. Intimate familiarity with your oscilloscope is invaluable in getting the best possible results with it. In fact, you can get good results with seemingly inadequate equipment if you know and respect the equipment's limitations.

Familiarity with equipment and thoughtful measurement technique permit useful measure-

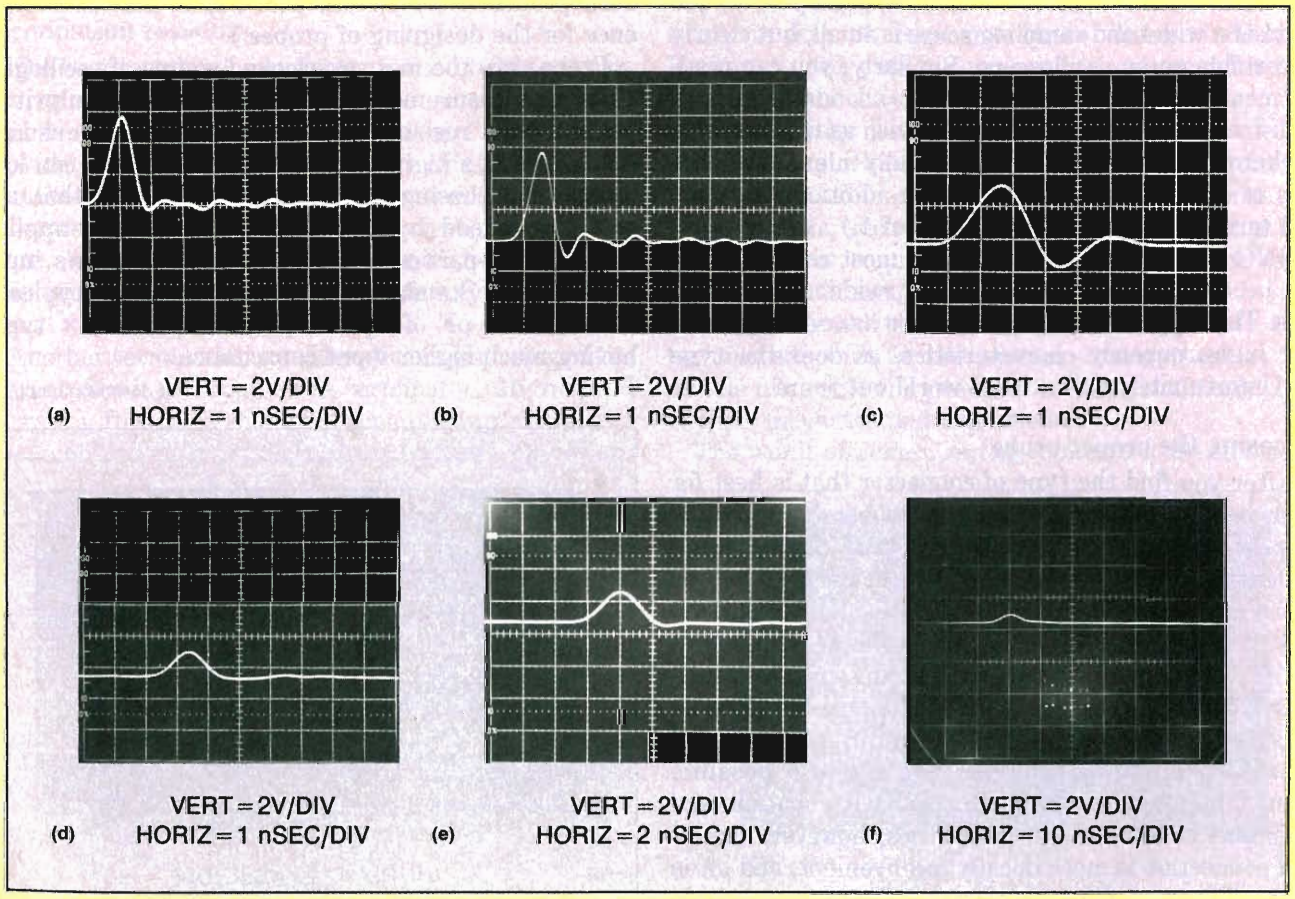



***Fig A—This series of photos shows*** *what the fast pulse in* ***Fig 2a*** *(pg 167) looks like on a variety of oscilloscopes.*

ments seemingly beyond instrument specifications. A 50-MHz oscilloscope cannot track a 5-nsec rise-time pulse, but it can measure a 2-nsec delay between two such events. Using such techniques, you can often deduce the desired information. In some situations no amount of cleverness will work and you must use the right equipment (for example, a faster oscilloscope).

Sometimes "reality checking" a limited-bandwidth instrument with a higher-bandwidth oscilloscope is all that you need to do. For high-speed work, brute-force bandwidth is indispensable when needed, and no amount of features or computational sophistication will substitute. Most high-speed circuitry does not require more than two traces to get where you are going. Versatility and many channels are desirable, but if your budget is limited, spend for bandwidth.

Probe-oscilloscope combinations of varying bandwidths produce dramatic differences in their displays. The series of scope photos in this box shows what a fast pulse looks like on various oscilloscopes. **Fig 2a** (pg 167) in the main text shows the output of a very fast pulse (**Ref 3**) monitored with a 1-GHz sampling scope (Tektronix 556 with 1S1 sampling plug-in). At this bandwidth the 10V amplitude appears clean, with just a hint of ringing after the falling edge. The rise and fall times of 350 psec are suspicious, as the sampling oscilloscope's rise time is also 350 psec.

**Fig Aa** shows the same pulse observed on a 350-MHz instrument with a direct connection to the input (Tektronix 485/50Ω input). Indicated rise time balloons to 1 nsec, while displayed amplitude shrinks to 6V, reflecting this instrument's lesser bandwidth. Poor grounding technique (1½ in. of ground lead to the ground plane) creates the prolonged rippling after the pulse fall.

**Fig Ab** shows results from the same 350-MHz oscilloscope with a 3-GHz, 10× probe (Tektronix P6056, 50Ω input). Displayed results are nearly identical, because the probe's high bandwidth contributes no degradation. Again, deliberate poor grounding causes overshoot and rippling on the pulse's falling edge.

**Fig Ac** equips the same oscilloscope with a 10× probe specified at a 290-MHz bandwidth (Tektronix P-6047). Additionally,

*Text continued on pg 170*

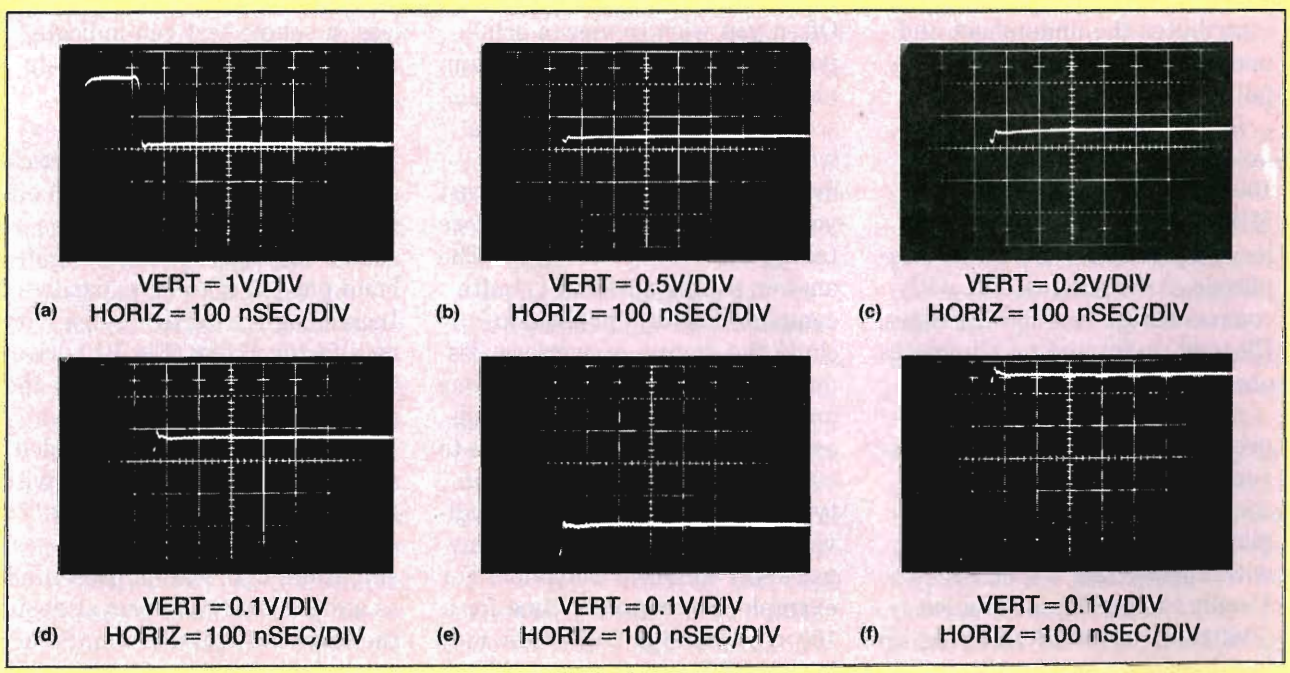



***Fig B—Your particular oscilloscope may** perform peculiarly when overloaded, as this series of scope photos demonstrates.*

The probe-caused problem in **Fig 3** shows up as output peaking and ringing. In other respects the display is acceptable. A second 10× probe connected to the amplifier's summing junction causes this output peaking. Because the summing point is so central to analyzing op-amp operation, it often has a probe attached. At high speeds, the probe's 10-pF input capacitance causes a significant lag in feedback action, forcing the amplifier to overshoot and hunt as it seeks the null point. Minimizing this effect calls for probes having the lowest possible input capacitance, mandating FET types or special passive probes. Account for the effects of probe capacitance, which often dominate the probe's impedance at high-speeds. A standard 10-pF 10× probe, combined with a 1-kΩ source resistance, forms a 10-nsec lag.

But, by far, improper grounding is the greatest source of error in probe use. Poor probe grounding can cause ripples and discontinuities in the observed waveform. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is the parasitic inductance in the probe's ground connection.

**Fig 4** shows an amplifier output that rings and distorts badly after rapid voltage excursions. Here, the circuit is not at fault; the probe's ground lead is too long. For general-purpose work, most probes come with ground leads about six inches long. At low frequencies this length is fine. At high-speed, the long ground lead looks inductive, causing the ringing shown.

Fast probes always come with a variety of spring clips and accessories designed to aid in making the

## What to look for in oscilloscopes *(continued)*

the oscilloscope was in its 1-MΩ input mode, reducing bandwidth to a specified 250 MHz. Amplitude degrades to less than 4V, and edge times similarly increase. The deliberate poor grounding contributes the undershoot and underdamped recovery on pulse fall.

In **Fig Ad** a 100-MHz, 10× probe (Hewlett-Packard Model 10040A) substitutes for the 290-MHz unit. The oscilloscope and its setup remains the same. Amplitude shrinks below 2V, with commensurate rise and fall times. Cleaned up grounding eliminates aberrations.

A Tektronix 454A (150 MHz) produced **Fig Ae**'s trace. A pulse generator connected directly to the oscilloscope's input. Displayed amplitude is about 2V, with appropriate 2-nsec edges. Finally, a 50-MHz instrument (Tektronix 556 with 1A4 plug-in) just barely grunts in response to the pulse (**Fig Af**). Indicated amplitude is 0.5V, with edges reading about 7 nsec. This last display is a long way from the 10V and 350 psec that's really there.

A final oscilloscope characteristic is overload performance. Often you wish to view a small portion of a large waveform's amplitude. In many cases the oscilloscope must supply an accurate waveform after the display is driven off screen. How long must you wait after an overload before taking the display seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude and other considerations. Oscilloscope response to overload varies widely between types. Among a given type, individual instruments often display markedly different behavior. For example, the recovery time for a 100× overload at 0.005V/div may be very different than at 0.1V/div. The recovery may also vary with waveform shape, dc content, and repetition rate.

With so many variables, clearly you must approach measurements involving oscilloscope overload with caution. Nevertheless, a simple test can indicate when overdrive is deleteriously affecting an oscilloscope.

Place the waveform to be expanded on the screen at a vertical sensitivity that eliminates all off-screen activity. **Fig Ba** shows such a display. The lower right-hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (**Fig Bb**) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, you can see small-amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of

lowest possible inductive connection to ground. Most of these attachments assume that your circuit has a ground plane—which it should have. Always try to make the shortest possible connection to ground; anything longer than one inch may cause trouble. The ideal probe-ground connection is purely coaxial. Probes mated directly to board-mounted coaxial connectors give the best results.

Sometimes determining if probe grounding is the cause of observed waveform aberrations is difficult. One good test is to disturb the grounding setup and see if changes occur. Touching the ground plane or jiggling probe-ground connectors or wires should have no effect. If you are using a ground-strap wire, try changing its orientation or simply squeezing it together to change and minimize its loop area. If any waveform change occurs, your probe grounding is unacceptable.

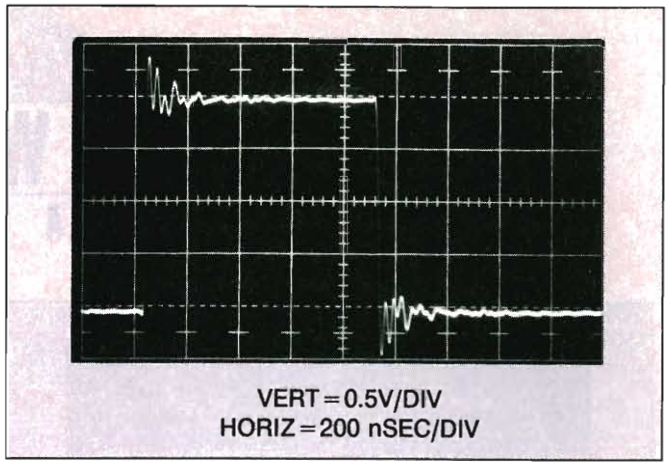



***Fig 4—Probe capacitance isn't the only fly in*** *the ointment; here, an overly long ground lead induces ringing.*

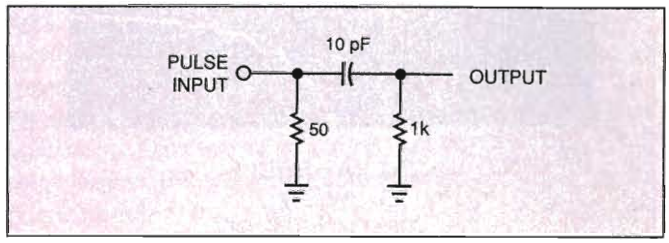



***Fig 5—Monitoring this simple circuit's*** *response to a pulse illustrates several potential probing problems.*

the original waveform is believable.

In **Fig Bc**'s display, gain is higher, and all the features of the **Fig Bb** example are amplified accordingly. The basic waveshape appears clearer, and the dip and small disturbances are also easier to see. No new waveform characteristics appear. The **Fig Bd** photo brings some unpleasant surprises. This increase in gain causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in **Fig Bc**. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble.

A further test can confirm that overloading is influencing this waveform. In **Fig Be**'s photo, the gain remains the same but the vertical position knob has repositioned the display at the screen's bottom. This shifts the oscilloscope's dc operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (**Fig Bf**). Obviously, for this particular waveform, you cannot obtain accurate results at this gain.

Differential plug-ins can address some of the issues associated with excessive overdrive, although they cannot solve all problems. Two differential plug-in types merit special mention. At low levels, a high-sensitivity differential plug-in is indispensable. The Tektronix 1A7 and 7A22 feature 10-μV sensitivity, although bandwidth is limited to 1 MHz. The units also have selectable highpass and lowpass filters and good high-frequency, common-mode rejection. Tektronix type 1A5, W, and 7A13 are differential comparators. They have calibrated dc nulling ("sideback") sources, letting you observe both small, slowly moving events on top of common mode dc or fast events riding on a waveform.

A special case is the sampling oscilloscope. Because of its nature of operation, a sampling scope in proper working order is inherently immune to input overload, providing essentially instantaneous recovery between samples (**Ref 4**).

The best approach to measuring small portions of large waveforms, however, is to eliminate the large signal swing seen by the oscilloscope. The **box,** "Measuring amplifier settling time," in the article "Subduing high-speed op-amp problems" (scheduled for the October 24 issue of EDN), shows ways to do this when measuring DAC/amplifier settling time to very high accuracy at high speed.

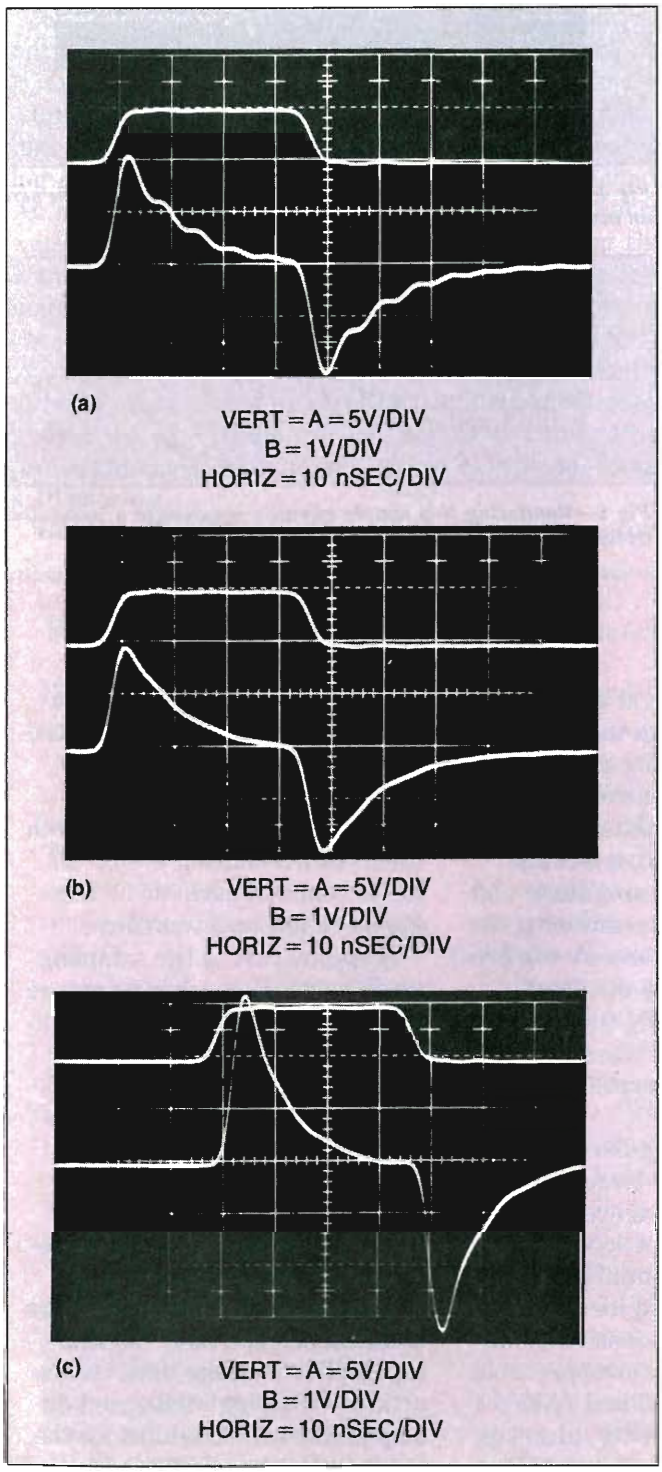



***Fig 6—A probe's capacitance and ground-lead*** *inductance add ringing and distortion to the output (**a**). Substituting a spring clip for the ground lead cleans up the output trace somewhat (**b**). Substituting an FET probe for the ground lead (**c**) reveals a 50% amplitude distortion in **b**.*

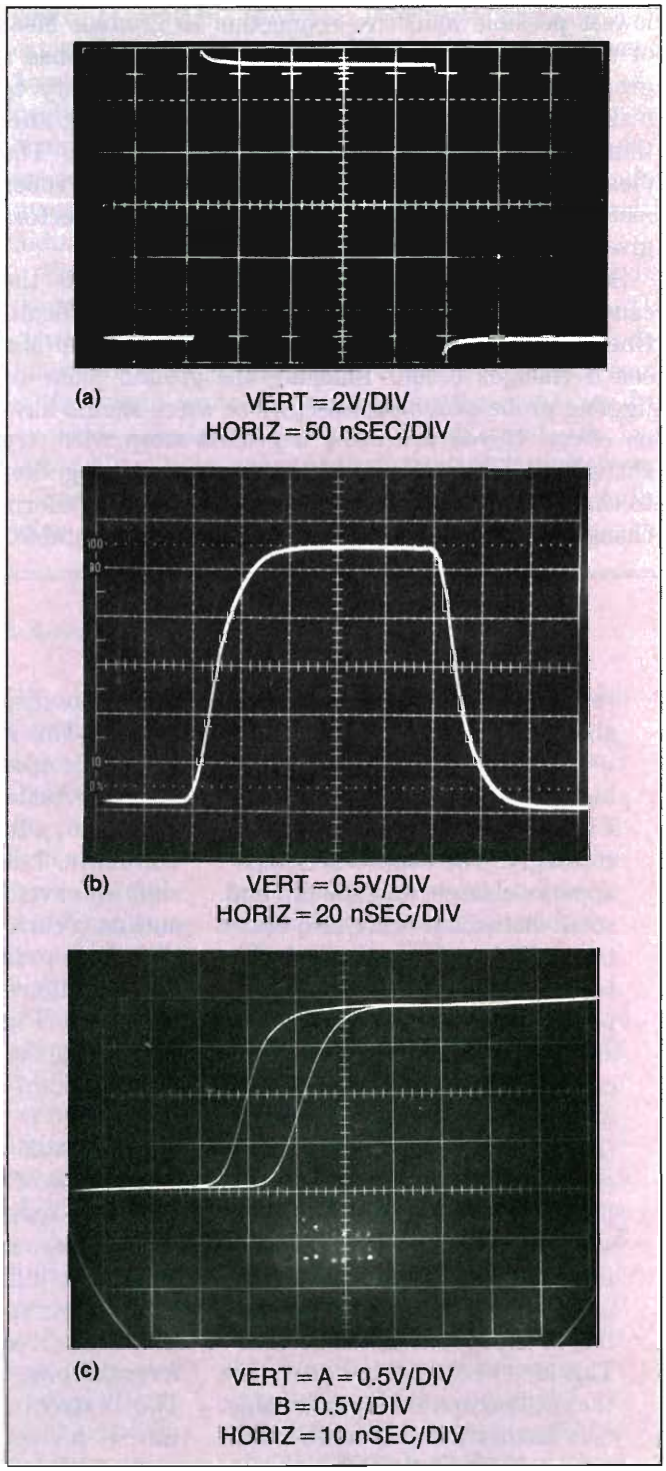



***Fig 7—In a, a grossly miscompensated or improperly*** *selected oscilloscope probe causes an op amp to appear to be delivering an 11V output from a 5V supply. In **b**, a probe having insufficient bandwidth rounds off the edges of this waveform. Probes can also add significant delay to observed waveforms (**c**).*

The simple network of the circuit in **Fig 5** shows just how easily poorly chosen or used probes cause bad results. A 9-pF input-capacitance probe with a 4-in. ground strap monitors the output (**Fig 6a**). Although the pulse input is clean, the output contains ringing. Using the same probe with a ¼-in. spring-tip ground-connection accessory seemingly cleans up everything (**Fig 6b**). However, substituting a 1-pF FET probe (**Fig 6c**) reveals a 50% output-amplitude error in **Fig 6b**'s measurement. The FET probe's low-input capacitance allows a more accurate version of the circuit's action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5 nsec because of delay in its active circuitry. Hence, you must make separate measurements with each probe to determine amplitude and timing characteristics of the output.

### Poorly compensated probe

In **Fig 7a**, the probe is properly grounded, but a new problem pops up. This photo shows an amplifier output excursion of 11V—quite a trick from an amplifier running from ±5V rails. Engineers commonly report this confusing problem when they work on high-speed circuits. The problem arises not because of a suspension of natural law, but from a grossly miscompensated or improperly selected oscilloscope probe. Use probes that match your oscilloscope's inputs and compensate them properly.

**Fig 7b** illustrates another probe-induced problem. Here the waveform's amplitude seems correct, but the amplifier appears slow, developing pronounced edge rounding. Here, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1× or "straight" probes. Their bandwidth is 20 MHz or less and their capacitive loading is high. Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope that has adequate bandwidth.

Mismatched probes account for the apparent excessive amplifier delay in **Fig 7c**'s amplifier. The display shows delay of almost 12 nsec for an amplifier that specs 6 nsec. Always keep in mind that various types of probes have different signal-transit delay times. At high-sweep speeds this effect shows up in multitrace displays as time skew between individual channels. Using similar probes will eliminate this problem, but measurement requirements often dictate dissimilar probes. In such cases you should measure the differential delays and then mentally factor them in to reduce error when interpreting the display. Note that active probes, such as FET and current probes, have signal transit times as long as 25 nsec. A fast 10×- or 50Ω-probe's delay can be inside 3 nsec. Account for probe delays in interpreting oscilloscope displays.

**Fig 8a** depicts a wildly distorted amplifier output. The output slews quickly, but the pulse's top and bottom recovery have lengthy, tailing responses. Additionally, the amplifier's output seems to clip well below its nominal-rated output swing. A common oversight is responsible for these conditions—An FET probe monitors the amplifier's output in this example. The probe's common-mode input range has been exceeded, causing the probe to overload, clip, and distort badly.

The rising pulse drives the probe deeply into saturation, forcing its internal circuitry away from normal

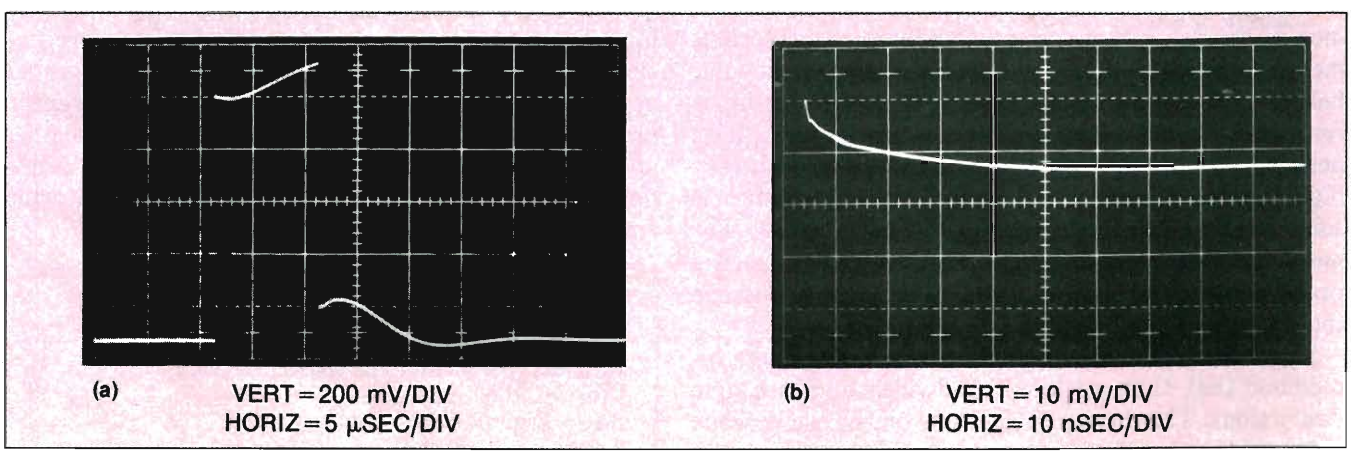



***Fig 8—Section a shows the result of overdriving an FET probe's internal circuitry,*** *and* ***b*** *illustrates the inadvisability of attaching bargain-basement probes to a high-speed circuit.*

operating points. Under these conditions the displayed pulse top is invalid. When the circuit's output falls, the probe's overload recovery is lengthy and uneven, causing the tailing. More subtle forms of FET probe overdrive may show up as extended delays, but there is no obvious signal distortion. Avoid saturation effects arising from an FET probe's common-mode input limitations (typically ±1V) by using 10× and 100× attenuator heads when required.

A peaked, tailing response is the characteristic depicted in **Fig 8b**. The photo shows the final 40 mV of a 2.5V amplifier excursion. Instead of a sharp corner that settles cleanly, peaking occurs, followed by a lengthy tailing decay. An inexpensive "off-brand" 10× probe picked off this waveform. Such probes are often poorly designed, and constructed from materials inappropriate for high-speed work. Selecting and integrating materials for wideband probes is a specialized and difficult art. Probe designers must expend substantial design effort to get good fidelity at high speeds. Never use probes unless their manufacturer specifies them for wideband operation. Obtain probes from a vendor you trust.

When choosing your probe, also keep in mind that you cannot use all 10× probes with all oscilloscopes indiscriminately; the probe's compensation range must match the oscilloscope's input capacitance. Low impedance probes, designed for 50Ω inputs, (with 500Ω to 1kΩ resistance) usually have input capacitance of 1 or 2 pF. They are a very good choice if you can stand the low resistance. FET probes maintain high-input resistance and keep capacitance at the 1-pF level, but have substantially more delay than passive probes.

FET probes also have limitations on the input common-mode range that you must adhere to or serious measurement errors will result. Contrary to popular belief, FET probes do not have extremely high input resistance—some types are as low as 100 kΩ. It is possible to construct a wideband FET probe with very high input impedance, although input capacitance is somewhat higher than standard FET probes. For measurements requiring these characteristics, such a probe is useful (see **box,** "Build your own oscilloscope tools").

Regardless of which type of probe you select, remember that they all have bandwidth and rise-time restrictions. The displayed rise time on the oscilloscope is the vector sum of source, probe, and scope rise times,

$$T_{RISE}=\sqrt{(T_{RISE}\ SOURCE)^2+(T_{RISE}\ PROBE)^2+(T_{RISE}\ OSCILLOSCOPE)^2}.$$

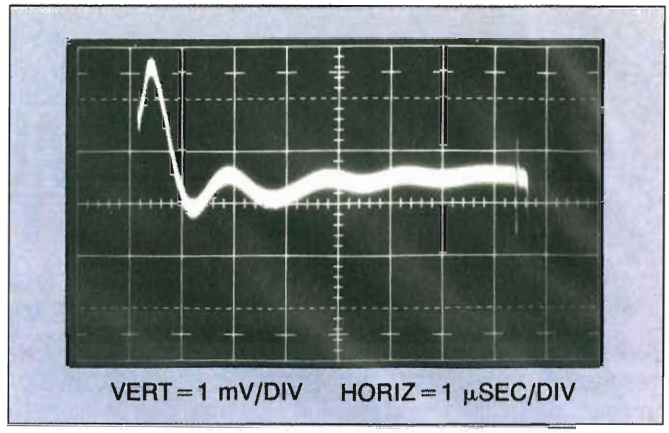



***Fig 9—What appears to be a circuit's ringing*** *is actually the oscilloscope recovering from overdrive arising from an off-screen excursion.*

This equation warns that some rise-time degradation must occur in a cascaded system. In particular, if the probe and oscilloscope have the same rise time, the system's response will be slower than either.

Current probes are useful and convenient. The passive transformer types are fast and have less delay than the Hall-effect versions. The Hall types, however, respond at dc and low frequency, while the transformer types typically roll off somewhere below 1 kHz to 100 Hz. Both types have saturation limitations which, when exceeded, cause odd results on the CRT that will confuse the unwary. The Tektronix CT-1 current probe, albeit not nearly as versatile as the clip-on probes, bears mention. Although the CT-1 is not a clip-on device, it may be the least electrically intrusive way of extracting wideband signal information. Rated at a 1-GHz bandwidth, the CT-1 produces 5-mV/mA output with only 0.6-pF loading. The decay time-constant of this ac-current probe is ~1%/50 nsec, resulting in a low-frequency limit of 35 kHz.

A very special probe is the differential probe. You may think of a differential probe as two matched FET probes contained within a common probe housing. This probe literally brings the advantage of a differential-input oscilloscope to the circuit board. The probes' matched, active circuitry provides greatly improved high-frequency, common-mode rejection compared to single-ended probing or even matched, passive probes used with a differential amplifier. The differential probe's resultant ability to reject common-mode signals and "ground noise" at high frequency lets this probe deliver exceptionally clean results when monitoring small, fast signals.

## Acronyms used in this article

**BNC**—BNC coax connector. A twist-lock connector for various types of RG-type coaxial cables.
**CRT**—Cathode-ray tube
**DAC**—Digital-to-analog converter
**dc**—Direct current
**FET**—Field-effect transistor
**IC**—Integrated circuit

A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can introduce stray capacitance to a suspected circuit node while you observe the results on the CRT. Two fingers, lightly moistened, can provide an experimental resistance path. Some engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

You can mount a miniature coaxial connector on your circuit board and mate whichever type of probe you choose to it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended. If you use a current probe, a ground connection is not usually required. However, at high speeds, a ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of current probes, a long strap is usually permissible.

Even an ideal probe connection does not guarantee an accurate scope display. **Fig 9** shows the final movements of an amplifier output excursion. Setting the scope at only 1-mV per division, the objective is to view the settling residue at high resolution. Multiple time constants, nonlinear recovery, and tailing characterize this response. Note also the high-speed event just before the waveform begins its negative going-transition. What you are actually seeing is the oscilloscope recovering from excessive overdrive. You should approach any observation that requires off-screen positioning of parts of the waveform with the greatest caution. Oscilloscopes vary widely in their response to overdrive, bringing displayed results into question. Approach all oscilloscope measurements that require off-screen activity with caution. Know your instrument's capabilities and limitations. EDN

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## Author's biography

*For more information on this article's author, see pg 163*

Article Interest Quotient (Circle One)
High 491 Medium 492 Low 493

## Build your own oscilloscope tools

Under most circumstances the 1- to 2-pF input capacitance and 10-MΩ resistance of FET probes is more than adequate for difficult probing situations. Occasionally, however, you may need very high input resistance along with high speed. At some sacrifice in speed and input capacitance, compared with commercial probes, you can construct such a probe.

**Fig A** shows schematic details. $IC_1$, a 350-MHz hybrid FET buffer, forms the electrical core

*Text continued on pg 176*

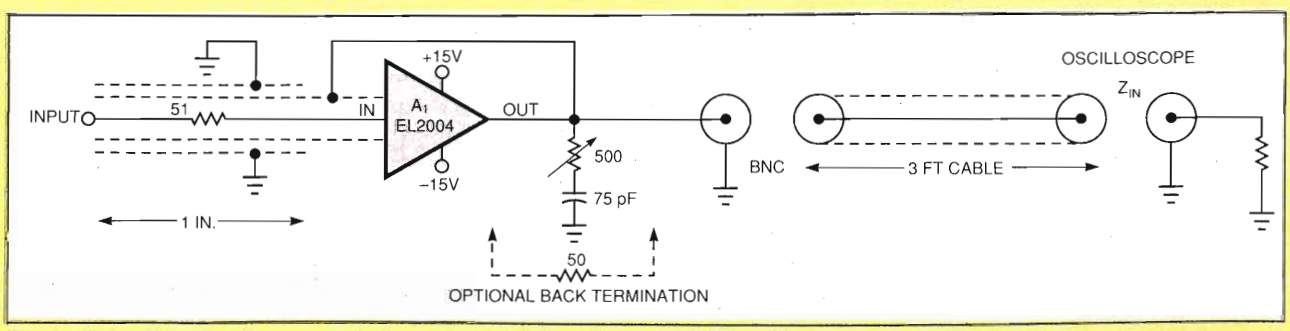



***Fig A—Using this circuit, you can** build your own high-performance FET oscilloscope probe.*

## Build your own oscilloscope tools *(continued)*

of the probe. This device is a low input-capacitance, wideband-FET source follower driving a fast bipolar output stage. The input of the probe goes to this device via a 51Ω resistor, reducing the possibility of oscillations in the follower's input stage when the probe sees low ac impedance. $IC_1$'s output drives a guard shield around the probe's input line, reducing effective input capacitance to about 4 pF. A ground-referred shield encircles the guard shield, reducing pickup and making high-quality ground connections to the circuit under test easy.

$IC_1$ drives the output BNC cable to feed the oscilloscope. Normally, back-terminating the cable at $IC_1$ is undesirable because the oscilloscope sees only half of $IC_1$'s output. Although a back termination provides the best signal dynamics, the resulting attenuation is a heavy penalty. You can trim the RC damper for best edge response while still maintaining an unattenuated output.

What you can't see in the schematic is the probe's physical construction. You must built the probe very carefully to maintain low input capacitance, low bias current, and wide bandwidth. The probe's head is particularly critical. Make every effort to minimize the length of wire between $IC_1$'s input and the probe's tip. In our lab, we have found that discarded pieces of broken 10× probes, particularly attenuator boxes and probe heads, provide excellent packaging for this probe.

**Fig B** shows the probe's head. Note the compact packaging. Additionally, $IC_1$'s package transfers its not-insubstantial heat to the probe's case when the snap-on cover (shown in photo) is in place. This reduces $IC_1$'s substrate temperature, keeping bias current down. $IC_1$'s input connects directly to the probe's head to minimize parasitic capacitance. The power supply for $IC_1$, located in a separate enclosure, feeds in through separate wires. $IC_1$'s output goes to the oscilloscope via conventional BNC hardware.

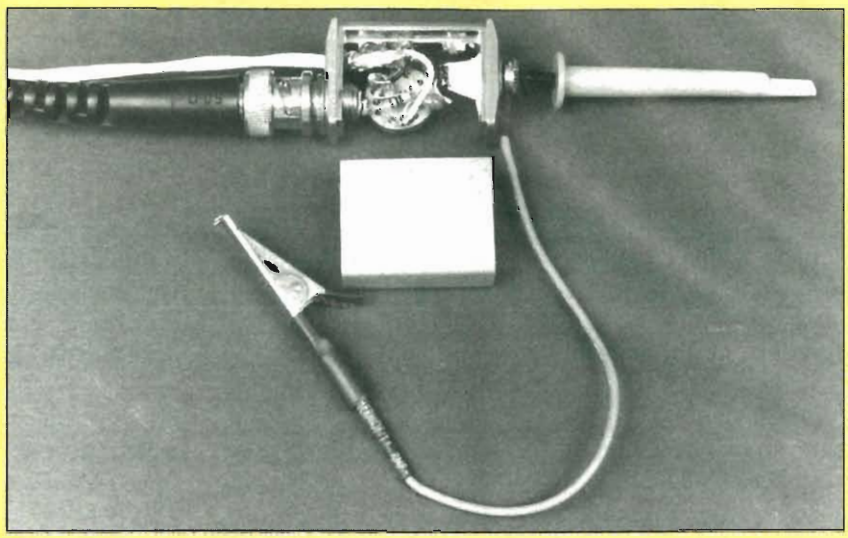


***Fig B—The components in Fig A fit** nicely into a salvaged commercial probe.*

**Fig C** shows the probe's output responding to an input as monitored on a 350-MHz oscilloscope (Tektronix 485). Measured specifications for Linear Technology's version of this probe include a rise time of 6 nsec, 6-nsec delay, and 350-MHz bandwidth. The delay time splits evenly between the amplifier and cable. Input capacitance is about 4 pF without the probe-hook tip and 7 pF with the hook tip. Input bias current measured 400 pA and gain error about 5% ($IC_1$ is an open-loop device).

Verifying the rise-time limit of wideband test equipment setups is a difficult task. In particular, you must often know the "end-to-end" rise time of oscilloscope-probe combinations to ensure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. The circuit described in **Ref 1** does this, providing a 1-nsec pulse having rise and fall times less than 350 psec. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time of almost any oscilloscope-probe combination.

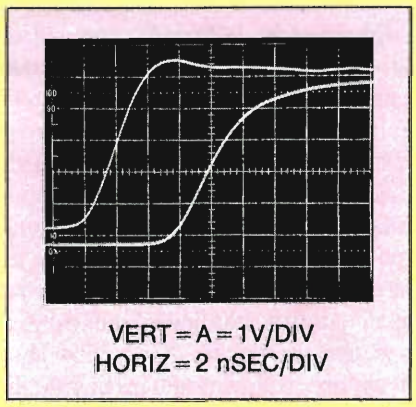



***Fig C—This scope photo shows the homemade probe's** output responding to an input.*

THE JIM WILLIAMS PAPERS

# High-speed amplifiers with low offset and drift

Amplifiers designed for wide bandwidth or fast settling often exhibit inferior characteristics at dc—that is, high voltage, current offset, and drift. Used with care, the techniques described here let you build circuits that exhibit exemplary performance from dc to MHz.

Jim Williams, *Linear Technology Corp*

Often, you must produce an amplifier circuit that has both the low offset of a dc amplifier and the wide bandwidth of a fast device. A number of techniques let you achieve such a result. Which method is best depends heavily on your application. Several circuits follow that you can study, build, and compare to determine what's best for you.

**Fig 1** shows a composite amplifier that consists of an LT1097 low-drift device ($IC_1$) and an LT1191 high-speed amplifier ($IC_2$). The overall circuit is a unity-gain inverter that has its summing node at the junction of the two 1-kΩ resistors. $IC_1$ monitors this summing node, compares it to ground, and drives $IC_2$'s positive input to complete a dc-stabilizing loop around $IC_2$. The 100-kΩ·0.01-μF time constant at $IC_1$ limits the amplifier's response to low-frequency signals. $IC_2$ handles high-frequency inputs, whereas $IC_1$ stabilizes the dc operating point. The 4.7-kΩ/220Ω divider at $IC_2$'s input prevents excessive overdrive during startup. This circuit combines $IC_1$'s 35-μV offset and 1.5-μV/°C drift with $IC_2$'s 450V/μsec slew rate and 90-MHz bandwidth. Bias current, dominated by $IC_2$, is about 500 nA.

**Fig 2** is similar, except that the sensing is differential, preserving access to both of the fast amplifier's inputs. $IC_1$ measures the dc error at $IC_2$'s input terminals and biases $IC_2$'s offset pin to force the offset to within 50 μV. $IC_2$'s offset-pin biasing arrangement always lets $IC_1$ find the servo point. The 0.01-μF capacitor rolls off $IC_1$'s gain at low frequencies, and $IC_2$ han-

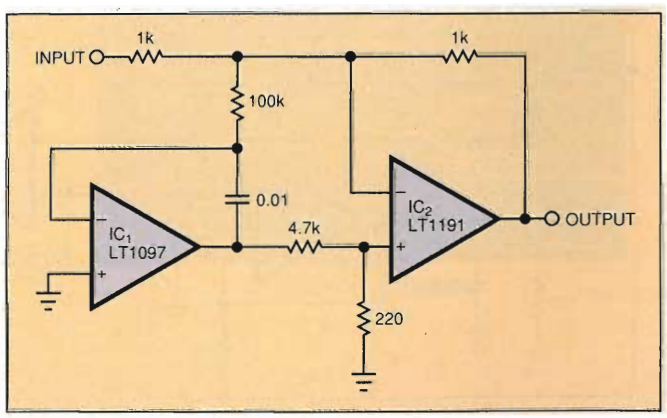



***Fig 1—An integrator ($IC_1$) reduces the drift of a wideband amplifier ($IC_2$) by applying a signal to the wideband amplifier's noninverting input. That signal holds the wideband amplifier's summing junction at ground.***

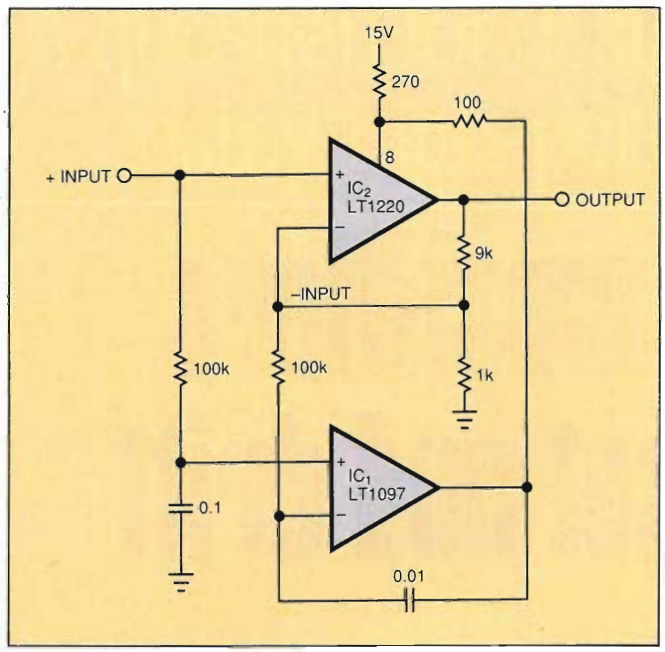



***Fig 2—You can also stabilize the offset*** *of a wideband amplifier ($IC_2$, in this case) by using a precision dc amplifier ($IC_1$) to apply correcting signals to the wideband amplifier's offset-trim adjustment pin.*

dles high-frequency signals. The combined characteristics of these amplifiers yield an offset voltage of 50 μV, an offset drift of 1 μV/°C, a slew rate of 250 V/μsec, and a gain bandwidth of 45 MHz.

**Fig 3** shows wideband, highly stable gain-of-10 amplifier with high input impedance. The input capacitance is about 3 pF. Because of its low input capacitance and low (100 pA) bias current, the circuit is well suited for use in probing IC wafers or as a pin amplifier in automatic-test systems.

$Q_1$ and $Q_2$ constitute a simple, high-speed FET-input buffer. $Q_1$ functions as a source follower, and the $Q_2$ current-source load sets the drain-to-source channel current. $IC_2$ provides a gain of 10 with 100-MHz bandwidth. Normally, this open-loop configuration would drift unacceptably because there is no dc feedback. $IC_1$, by comparing the filtered circuit output to a similarly filtered version of the input signal, provides the feedback to stabilize the circuit. The amplified difference between these signals sets $Q_2$'s bias—and hence $Q_1$'s channel current—thereby forcing $Q_1$'s $V_{GS}$ to match the circuit's input and output potentials. The capacitor around $IC_1$ provides stable loop compensation. The R-C network in $IC_1$'s output prevents that output from seeing high-speed edges coupled through $Q_2$'s collector-base junction.

**Fig 4a** shows a way to combine wide bandwidth with true differential inputs and dc stabilization. $IC_1$ and $IC_2$ sense the input differentially at gains of 10. Wideband amplifier $IC_1$ feeds high-frequency signals to output amplifier $IC_3$ via a highpass network. Low-frequency and dc information get to $IC_3$ via the slower $IC_2$. The 2-kΩ/200-pF lowpass networks remove the input signal's high-frequency components, so only lower frequencies reach $IC_2$. Because the gain and bandwidth of the high- and low-frequency paths complement each other, $IC_3$'s output is an undistorted, amplified version of the input (see **Fig 4b**, trace D.)

**Fig 4b**, trace A is one side of a differential input signal applied to the circuit. Trace B is $IC_1$'s output

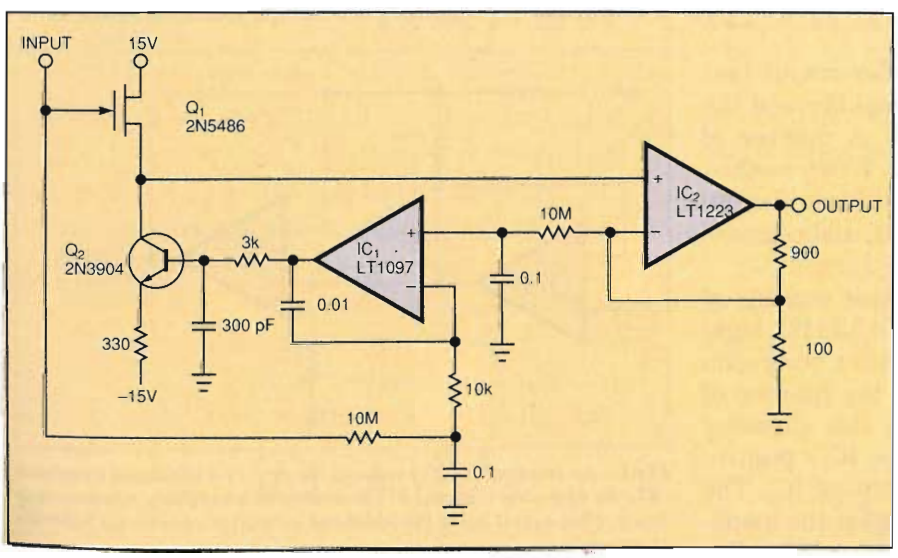



***Fig 3—An integrator ($IC_1$)*** *drives a current source ($Q_2$), which biases a FET ($Q_1$) that completes a dc feedback loop around $IC_2$ to stabilize the amplifier's operation at dc.*

taken at the junction of the 500Ω potentiometer and 0.001-μF capacitor. Trace C is $IC_2$'s output. With the "ac-gain" and "dc-gain-match" trims properly adjusted, the two paths' contributions match up and trace D is clean, with no residual artifacts. You can optimize the adjustments by trimming the ac gain for the squarest corners and the dc-gain match for a flat top. Bandwidth for this circuit exceeds 35 MHz; slew rate is 450V/μsec; and dc offset is about 200 μV.

### Parallel paths yield the best of two worlds

**Fig 5a** shows a very powerful extension of the previous circuit. The circuits operate similarly, but this one has a gain of 1000; its bandwidth is about 35 MHz; its rise time is 7 nsec; and its delay is less than 7.5 nsec. Full-power response is available to 10 MHz, and broadband input noise is about 15 μV. This kind of speed, coupled with true differential inputs, a gain of 1000, high dc stability, and low cost make the circuit broadly applicable in wideband instrumentation.

As before, two differential amplifiers, $IC_1$ and $IC_2$, simultaneously sense the inputs. In this case, $IC_1$ is a 592-733 type operating at a gain of 100. Its differential outputs feed output amplifier $IC_3$ via 1-μF/1-kΩ high-pass networks that strip out the dc content of $IC_1$'s output. $IC_2$, a precision dc differential amplifier, operates in similar fashion to its counterpart in the previous circuit, supplying dc and low-frequency information to $IC_3$ at a trimmed gain of 100.

In this case, the output amplifier, $IC_3$, is not a follower but a differential-input/single-ended-output gain block whose nominal gain is 10. This change is necessary because $IC_1$'s differential output must become a single-ended signal to provide the circuit's final output. Consequently, $IC_2$ does not directly apply its low-frequency information to $IC_3$ as it did before. Instead, $IC_4$ measures the difference between $IC_2$'s output and a fraction of $IC_3$'s output. $IC_4$'s output, biasing $IC_3$'s positive input via the 1-kΩ resistor, closes a loop around the circuit's dc and low-frequency path. To make the circuit's dc gain equal to its ac gain, you adjust the divider that feeds $IC_4$'s negative input.

**Fig 5b** shows the circuit's response to a 60-nsec, 2.5-mV pulse, trace A. The ×1000 output, trace B, responds cleanly, with both delay and rise time in the 5- to 7-nsec range. Some small amount of overshoot is evident, but you can trim the overshoot with the peaking adjustment at $IC_1$. **Fig 5c** plots the circuit's gain vs frequency. The gain is flat within 0.5 dB to 20 MHz, with the −3 dB point at 40 MHz. The overshoot of **Fig 5b** shows up here as a very slight gain increase starting around 1 MHz and continuing to about 15 MHz. The peaking adjustment eliminates this effect.

To use this circuit, apply a low-frequency or dc signal of known amplitude and adjust the low-frequency gain to ×1000 after the output has settled. Next, adjust the high-frequency gain so that the signal's leading and trailing corners have amplitudes identical to those

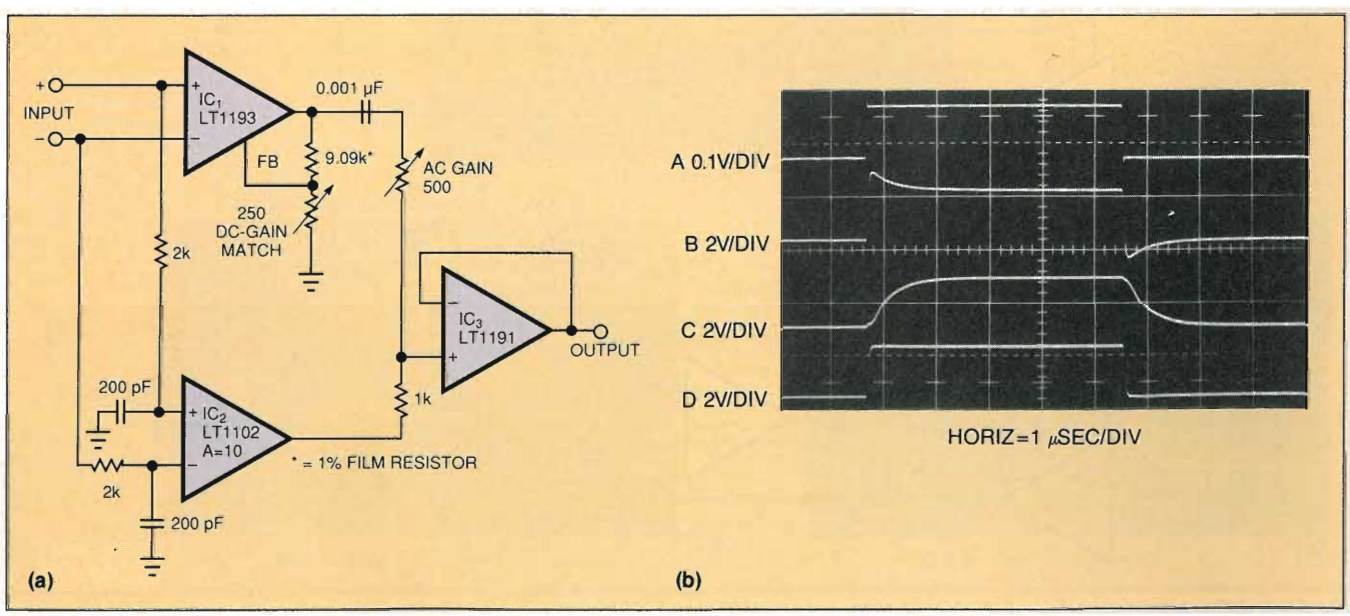



***Fig 4—Parallel paths** for ac and dc signals **(a)** provide low offset and good dynamic response—if you correctly adjust the trims (**b**, trace D).*

of the settled portion. Finally, trim the peaking adjustment for the best settling of the output pulse's corners.

**Fig 5d** shows the input (trace A) and output (trace B) waveforms with all adjustments properly set. The fidelity is excellent, with no aberrations or other artifacts of the parallel-path operation evident. **Fig 5e** shows the effects of too much ac gain; excessive peaking on the edges, with proper amplitude achieved only after the dc channel takes control of the output. Similarly, excessive dc gain produces **Fig 5f**'s traces. The ac-gain path provides proper initial response, but too much dc gain forces a long, tailing response that finally settles at an incorrect amplitude.

The use of parallel-path schemes to simultaneously achieve wide bandwidth and outstanding dc performance isn't new. In fact, it predates the use of low-drift bipolar differential gain stages. The first parallel-path amplifiers achieved dc stability by using electromechanical choppers to convert dc to ac. Gain stages consisting first of vacuum tubes and later of Germanium transistors amplified the chopped dc. Synchronous rectifiers converted the ac back to dc. AC-coupled amplifi-

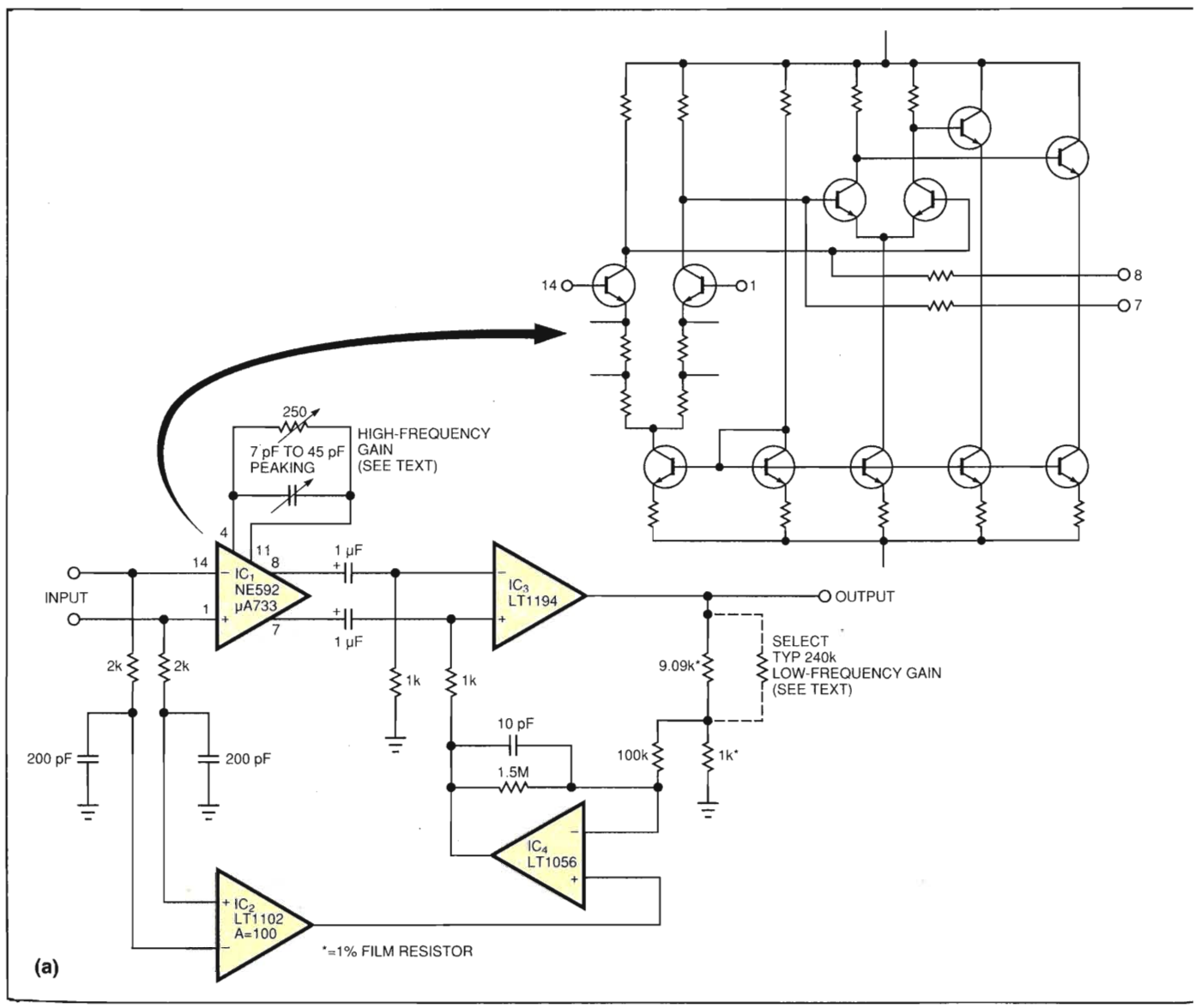


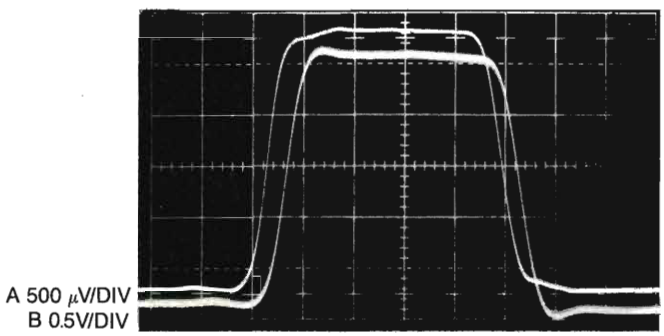

***Fig 5—A differential-to-single-ended gain of 1000** with 38-MHz bandwidth and excellent dc characteristics results from extending the parallel-path architecture, **(a)**. The pulse response (**b**, trace B) shows a minimum of overshoot, which is reflected in the frequency response*

ers in parallel with the chopper amplifiers provided good bandwidth. As **Figs 5e** and **5f** illustrate, these schemes have historically had a problem in many applications that demand the best at both dc and high frequencies: Unless you carefully match the dc and ac gains, the amplifiers' response to an input voltage step exhibits a long "tail." Keeping the response free of such tails over wide temperature ranges and long periods of time has always presented a challenge. Modern components make meeting that challenge easier, but the challenge still exists. EDN

## Author's biography

*For more information on this article's author, turn to page 163 in the October 10, 1991, issue.*

**Article Interest Quotient (Circle One)**
**High 473 Medium 474 Low 475**

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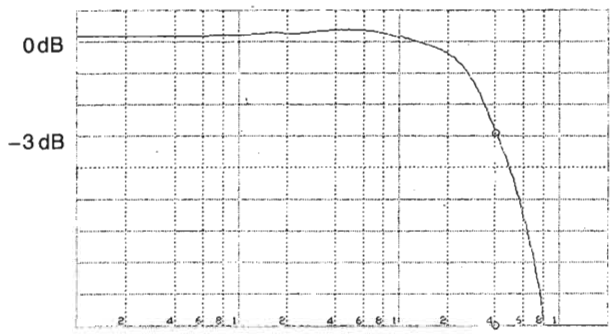


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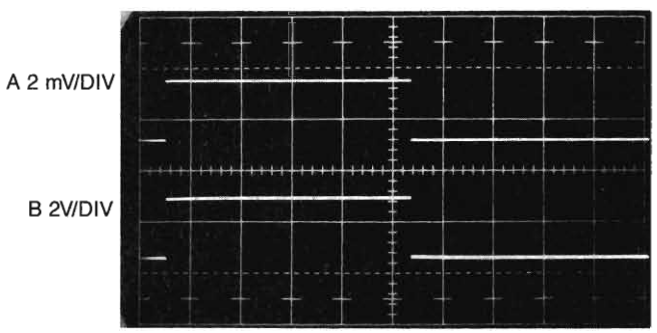


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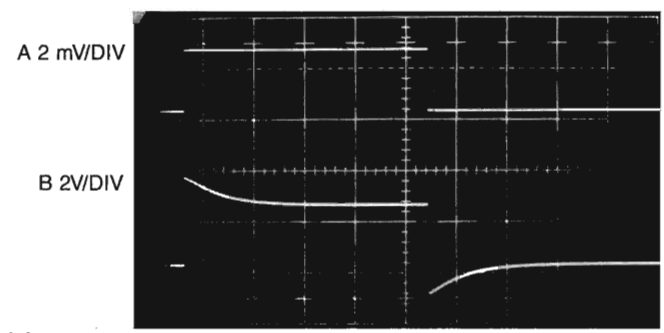
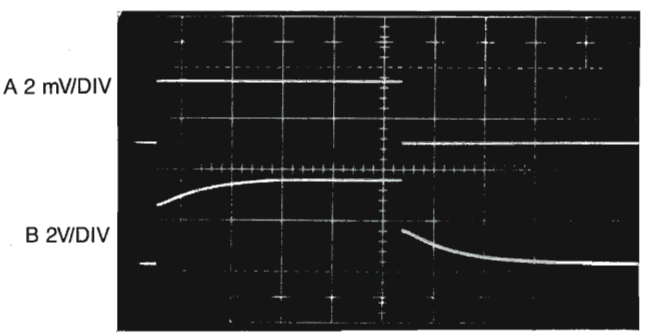



(e)




(f)

*(c) as a slight peak near 6 MHz. In the other three photos, (d, e, and f), you see, respectively, the effects of correctly matching the ac and dc gains, setting the ac gain too high, and setting the dc gain too high.*

THE JIM WILLIAMS PAPERS

# High-speed amplifiers in application circuits

Once you acquire some familiarity with high-speed amplifiers and a respect for their design requirements, you can use these devices' speed to design a variety of application circuits. These circuits include DAC current-to-voltage converters, video amplifiers, and power boosters.

Jim Williams, *Linear Technology Corp*

Recent processing and design advances have made inexpensive, precision wideband amplifiers practical. They are less prone to oscillation and other variations than some much slower amplifiers. High-speed amplifiers' raw speed capabilities, combined with their inherent flexibility as op amps, permit a range of applications. These amplifiers let you create fast linear circuits that are difficult or impractical to create using other approaches. You can use these application circuits to capitalize on the amplifier's speed to improve on a standard circuit. Or you can utilize speed to implement a traditional function in a nontraditional way, with attendant advantages. You can even design completely new, start-of-the-art circuit functions that were previously impractical to implement at the board level. Simply put, these amplifiers make implementing high-speed functions easier.

One of the most common applications for a high-speed amplifier, transforming a 12-bit DAC's current output into a voltage, is also one of the most difficult. Although an op amp can easily perform the required current-to-voltage conversion, obtaining good dynamic performance requires careful design. A fast DAC can settle to 0.01% in 200 nsec or less, but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's output directly drives an amplifier's summing junction, placing the parasitic capacitance between ground and the amplifier's input. This capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to ring about the final value before settling.

Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance—in the 100- to 150-pF range, which varies with the input code. Bipolar DACs typically have 20 to 30 pF of capacitance, which is constant over all codes. As such, bipolar DACs are almost always better to use where high speed is required. **Fig 1a** shows the AD565A 12-bit DAC with an LT1220 output op amp. **Fig 1b** shows clean 0.01% settling in 280 nsec (trace B) to a full-scale input step (trace A). The requirements for obtaining trace B's display are not trivial (**Ref 1**).

Another application area requiring good dynamic

stability is video amplifiers driving cables. **Fig 2** shows a simple way to multiplex two video amplifiers onto a single 7Ω cable. The level of the input-select line determines which of the two amplifiers is active in accordance with the truth table in the figure. Amplifier performance includes 0.02% differential gain error and 0.1° differential phase error. The cable's 75Ω back termination means that the amplifiers must swing $2V_{p-p}$ to produce $1V_{p-p}$ at the cable output, but most amplifiers can easily handle this output swing.

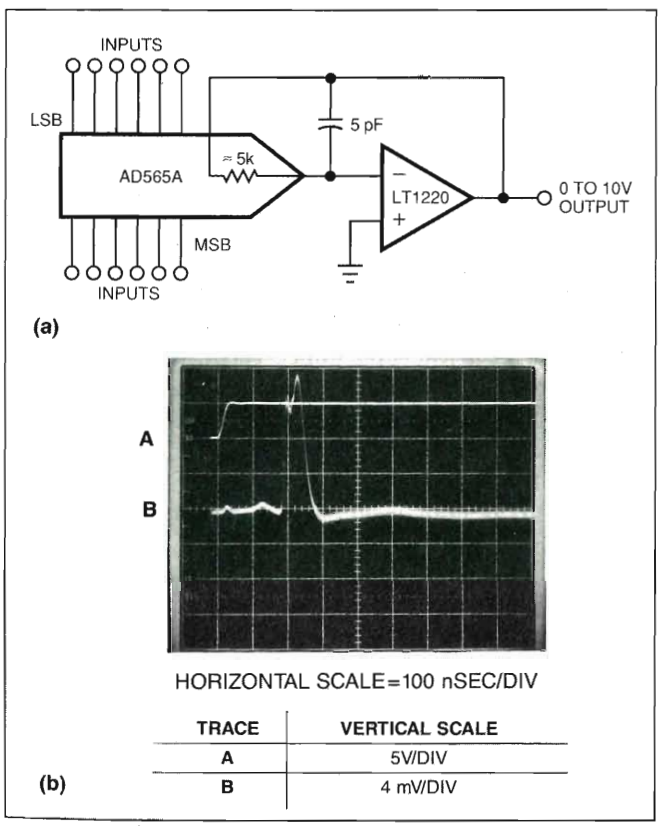
### Simple video amp

**Fig 3** is a simpler version of **Fig 2**. This circuit is a single-channel video amplifier, and it provides for a gain of 10. The circuit retains the double-cable termination of **Fig 2**, and the circuit has a 55-MHz bandwidth.

**Fig 4** is another cable-related circuit. Here, the differential amplifier simply hangs across a distribution cable, extracting the signal. The amplifier's true differential inputs reject common-mode signals. As in the previous circuit, differential-gain and phase errors measure 0.02% and 0.1°, respectively. A separate input permits for adjustment of the dc level.

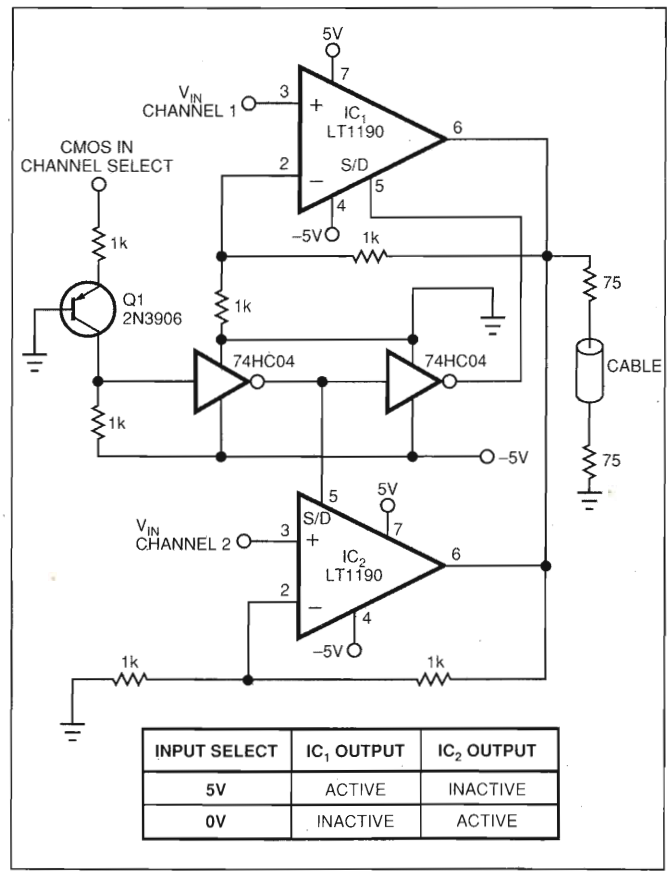
High-speed analog signals transmitted on a line often pick up substantial common-mode noise. **Fig 5a** shows a simple, fast, differential line receiver using the LT1194 gain-of-10 differential amplifier ($IC_1$). The differential line is fed to $IC_1$. The resistor-diode networks prevent overload and ensure sufficient input bias for $IC_1$ under all conditions. $IC_1$'s output represents the difference of the 2-line input, times a gain of 10. In theory, the circuit should reject all common-mode noise.

The test-circuit (**Fig 5b**) waveforms (**Fig 5c**) confirm this noise rejection. The sine-wave oscillator drives $T_1$ (**Fig 5c**, trace A), producing a differential line output at its secondary. $T_1$'s secondary returns to ground through a broadband noise generator, flooding the line inputs with common-mode noise (traces B and C are




| TRACE | VERTICAL SCALE |
|---|---|
| A | 5V/DIV |
| B | 4 mV/DIV |

*Fig 1—**Achieving good dynamic performance while** converting a DAC's output current to voltage is a difficult job for many op amps. The output of the circuit in **a** responds to a full-scale step (**b**, trace A) by fully settling in 280 nsec (**b**, trace B).*




| INPUT SELECT | $IC_1$ OUTPUT | $IC_2$ OUTPUT |
|---|---|---|
| 5V | ACTIVE | INACTIVE |
| 0V | INACTIVE | ACTIVE |

*Fig 2—**This 2-channel video amplifier features** 0.02% differential-gain error and 0.1° differential-phase error.*

$IC_1$'s inputs). Trace D, $IC_1$'s multiplied-by-10 version of the differential signal at its inputs, shows no visible noise or disturbances. This circuit provides a clean output, even in the presence of noise that dominates the signal by a 100:1 ratio from dc to 5 MHz.

**Fig 6a** shows another way to achieve high common-mode rejection. Additionally, this circuit has the advantage of true 3-port isolation. That is, the input, gain stage, and output are all galvanically isolated from each other. This configuration is useful where large common-mode differences exist or where ground integrity is uncertain. The circuit configures $IC_1$ for a simple gain of 11. $T_1$ feeds $IC_1$'s positive input, and the output passes through $T_2$. **Fig 6b** shows the circuit's response to a 4-MHz input, with all transformer leads designated "•" referred to ground. The input (**Fig 6b**, trace A) drives $T_1$, whose output (trace B) feeds $IC_1$. $IC_1$ amplifies the signal, and its output (trace C) feeds $T_2$. $T_2$'s output (trace D) is the circuit's output. Phase shift is evident, although tolerable. $T_1$ and $T_2$ are very wideband devices, with low phase shift. Note the negligible phase difference between the A-B and C-D trace pairs. $IC_1$ contributes the entire phase error. Using the transformers specified, the circuit's low frequency cut-off is about 10 kHz.

It is often desirable to examine or amplify one particular portion of a signal while rejecting all others.

*Text continued on pg 162*

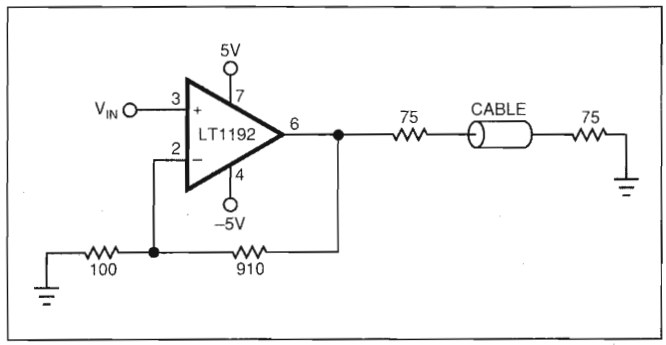



***Fig 3—This double-terminated cable driver*** *features a bandwidth of 55 MHz.*

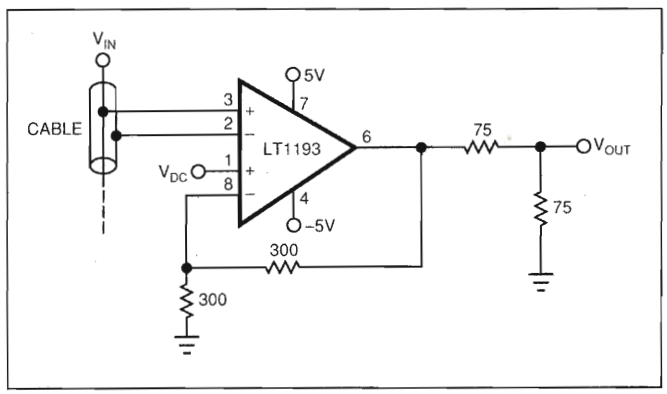
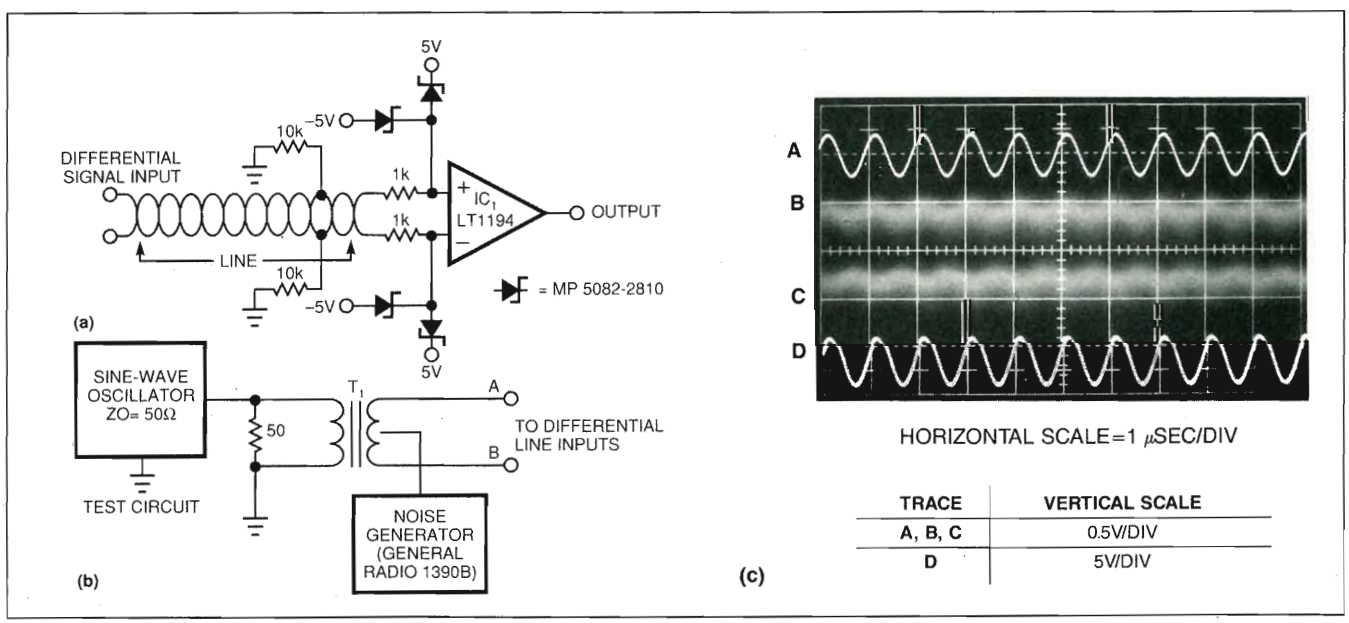



***Fig 4—To extract video signals,*** *this cable-sense amplifier features a loop-through connection.*




| TRACE | VERTICAL SCALE |
|---|---|
| A, B, C | 0.5V/DIV |
| D | 5V/DIV |

***Fig 5—By extracting signals buried*** *in common-mode noise, the output* ***(c****, trace D) of this differential line receiver* ***(a)*** *is clean despite the 100-to-1 noise-to-signal ratio. The test circuit in* ***b*** *provides both the input signal* ***(c****, trace A), and input noise* ***(c****, trace B) and C).*

# About "current-mode" feedback

Contrary to some enthusiastic marketing claims, so-called current-mode feedback isn't new. In fact, it is much older than the normal voltage-mode feedback that has been so popularized by op amps. The current-feedback connection is at least 50 years old, and probably much older. William R Hewlett used it in 1939 to construct his now-famous sine-wave oscillator. The term "cathode feedback" was widely applied in RF- and wideband-instrument design throughout the thirties, forties, and fifties. It was a favorite form of feedback, if for no other reason than there wasn't anyplace else left to feed back to.

In the early 1950s, G A Philbrick Researches introduced the K2-W, the first commercially available, packaged operational amplifier. This device, with its high-impedance differential inputs, permitted voltage-type feedback. Although low-frequency instrumentation engineers were quick to utilize the increased utility afforded by high-impedance feedback nodes, RF and wideband designers hardly noticed. They continued to use "cathode feedback," called (what else?) "emitter feedback" in the new transistor form.

Numerous examples of the continued use of "current-mode" feedback in RF and wideband instruments are found in designs dating from the 1950s to the present. Ostensibly easier-to-use voltage-type feedback was readily usable during this period, particularly as monolithic devices became cheap. Why did designers continue to use discrete current feedback? The reason for the continued popularity of current-feedback techniques was—and is—bandwidth. Current feedback is simply much faster.

Within certain limits, a current-feedback-based amplifier's bandwidth does not degrade as the closed-loop gain increases. This feature is a significant advantage over voltage-mode feedback amplifiers, whose bandwidth does degrade.

Recently, current-feedback-based designs have become available in general-purpose, easy-to-use monolithic and hybrid devices. These devices bring high-speed capability to a much wider audience, hopefully opening up new applications. So, while the technique is not new, marketing claims notwithstanding, the opportunity is. Although current-mode-based designs have poorer dc performance than voltage mode amplifiers, their bandwidth advantage is undeniable. What's the magic?

## Current feedback basics

William H Gross, Design Manager at Linear Technology Corp, offers the following insight into current feedback.

The distinctions between current-feedback and voltage-feedback amplifiers are not obvious at first because, viewed from the outside, the differences can be subtle. Both amplifier types use a similar symbol and can be applied on a first-order basis using the same equations. However, their behavior in terms of the gain-bandwidth tradeoff and large-signal response is another story.

Unlike in voltage-feedback amplifiers, small-signal bandwidth in a current-feedback amplifier isn't a straight inverse function of closed-loop gain, and large-signal response is closer to ideal. Both benefits stem from the fact that the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor, $R_F$, from output to inverting input, works with internal junction capacitances to set the closed-loop bandwidth. Even though the gain-set resistor, $R_G$, from inverting input to ground, works with $R_F$ to set the voltage gain, just as in a voltage feedback op amp, the closed-loop bandwidth does not change.

The explanation of these effects is fairly straightforward. The equivalent gain-bandwidth product of the current-feedback amplifier is set by the Thevenin equivalent resistance at the inverting input and the internal

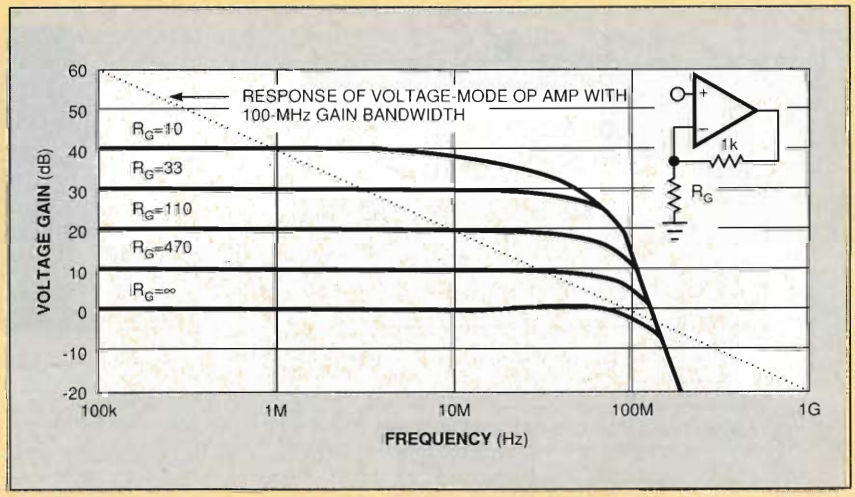



***Fig A—Unlike in traditional op amps,*** *which exhibit a gain-vs-frequency similar to that of the dashed line, current-feedback amplifiers have a constant bandwidth, even at different gain settings.*

compensation capacitor. If $R_F$ is held constant and gain changed with $R_G$, the Thevenin resistance changes by the same amount as the gain. From an overall loop standpoint, this change in feedback attenuation will produce a change in noise gain and a proportionate reduction of open-loop bandwidth, as in a conventional op amp.

With current feedback, however, the key point is that changes in Thevenin resistance also produce a compensatory change in open-loop bandwidth, unlike in a conventional fixed-gain bandwidth amplifier. As a result, the net closed-loop bandwidth of a current-feedback amplifier remains the same for various closed-loop gains.

## Bandwidth is the key advantage

**Fig A** shows a plot of voltage gain vs frequency for a representative current-feedback amplifier, the LT1223, for five gain settings, driving 100Ω. For comparison, the figure also shows a plot of the fixed 100-MHz gain-bandwidth limitation that a voltage-feedback amplifier would have. It is obvious that for gains greater than one, the current-feedback amplifier provides 3 to 20× more bandwidth. The general shape of this bandwidth profile is common to all current-feedback amplifiers.

Because the feedback resistor determines the compensation of the amplifier, you can optimize bandwidth and transient response for almost every application. When operating from ±15V supplies, $R_F$ should be 1 kΩ or more for stability. When operating from ±5V supplies, the minimum value is 680Ω because the junction capacitors increase with lower voltage. For either case, larger feedback resistors can also be used but will slow down the amplifier—which may be desirable in some applications.

The difference in operating characteristics between voltage- and current-feedback op amps results in slight differences in common circuit configurations. **Fig B** summarizes some popular circuit types, showing differences between each op-amp type. Gain can be set with either $R_{IN}$ or $R_F$ in a voltage-feedback op amp, but the $R_F$ used with a current-feedback op amp is fixed.

You can control a voltage-mode op amp's bandwidth using a feedback capacitor. However, when using current-feedback op amps, bandwidth must be limited at the input. A feedback capacitor is never used. In an integrator, the 1-kΩ resistor must be included in the current-feedback amplifier's feedback path so its negative input sees the optimal impedance.

There is no correlation between bias currents of a current-feedback amplifier's inputs. Thus, source impedance matching will not improve dc accuracy. Matching input source impedances aids offset performance only in op amps that do not have internal bias-current cancellation.

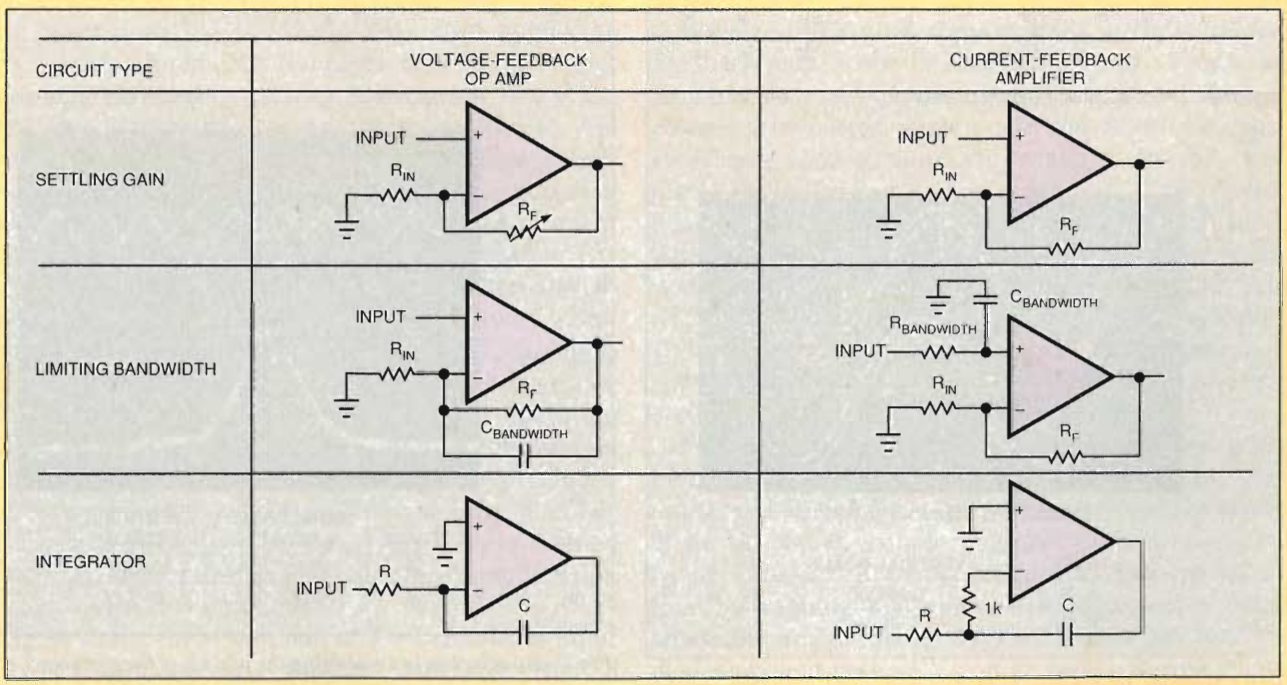



***Fig B—Although voltage-mode and current-feedback op amps look alike*** *when viewed from the outside, their internal architectural differences require that you use slightly different circuit topologies when applying them.*

At high speed, this can be difficult because the amplifier may see fast, large common-mode voltage swings. Recovery from such activity usually is dominated by saturation effects, making the quality of the amplifier's output questionable. Differential amplifiers with fast overload recovery can perform this function while maintaining output fidelity to the input signal. The circuit in **Fig 7a** allows you to set the input level at which amplifying begins, allowing any amplitude-defined point to be selected. In **Fig 7a**, $IC_1$, the LT1019 reference, and associated components form an adjustable, bipolar voltage source that is coupled to differential amplifier $IC_2$'s negative input. The input signal biases $IC_2$'s positive input; $R_1$ and $R_2$ set $IC_2$'s gain.

Input signals below $IC_2$'s negative input levels keep $IC_2$'s output in saturation, and no signal appears at the output. When the positive input rises above the negative input's bias point, $IC_2$ becomes active, providing an amplified version of the instantaneous difference between its inputs. **Fig 7b** shows what happens when you apply the output of a triangle wave generator (trace A) to the circuit. Setting the bias level just below the triangle peak permits high gain and detailed operation of the turnaround at the peak. Trace B clearly shows the switching residue in the generator's output. Appropriate variations in the voltage-source setting would permit more of the triangle slopes to be observed, with attendant loss of resolution due to oscilloscope overload limitations. Similarly, increasing $IC_2$'s gain allows more amplitude detail while placing restrictions on how much of the waveform you can display.

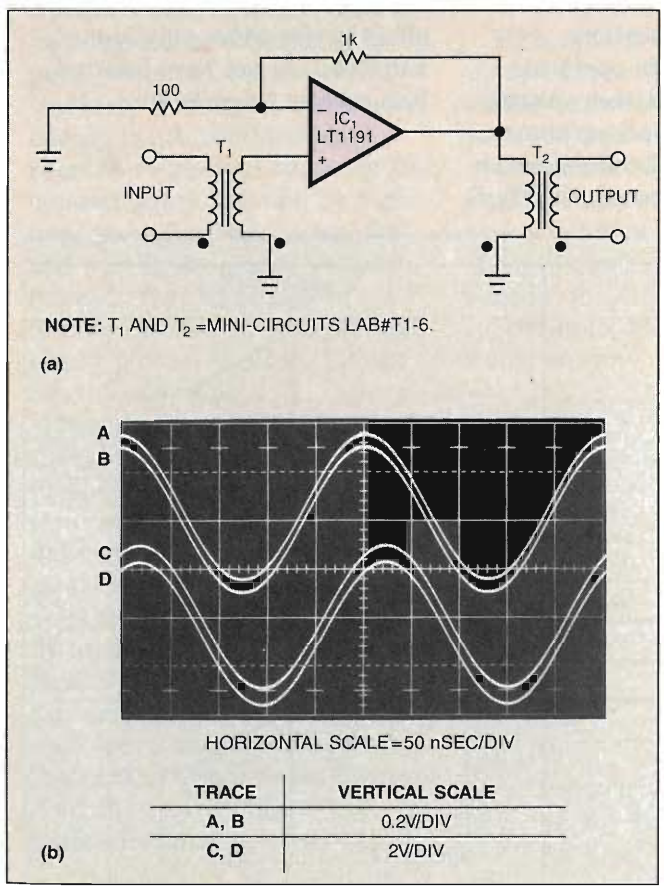



***Fig 6—Methods to achieve high common-mode rejection include*** *transformer coupling. The amplifier in* ***a*** *responds to an input (****b****, trace A) with a slightly phase-shifted output (trace D). Traces B and C are $T_1$'s secondary and $T_2$'s primary, respectively.*

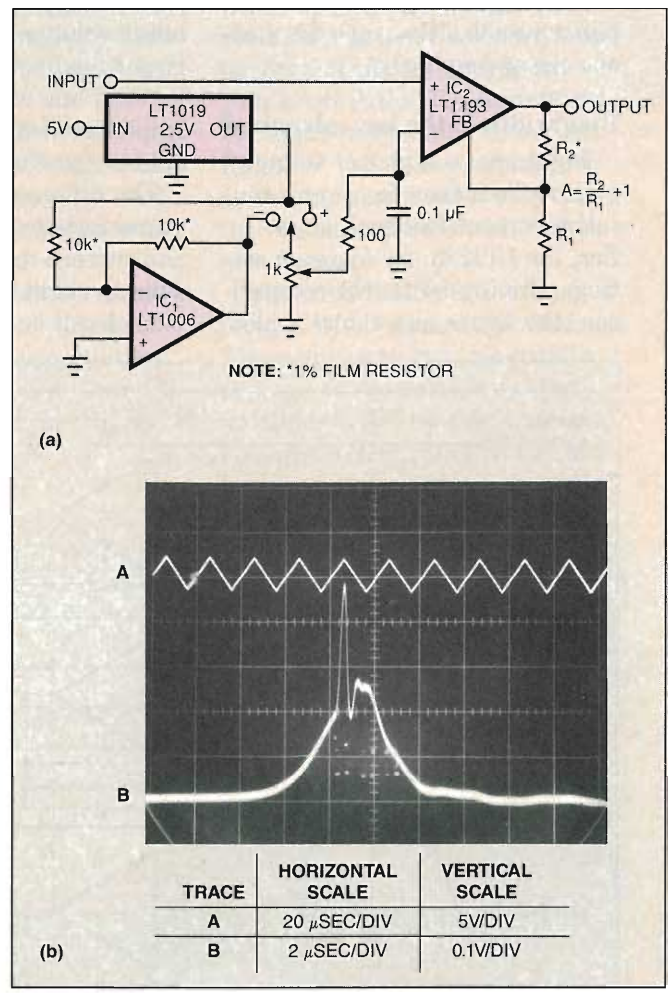
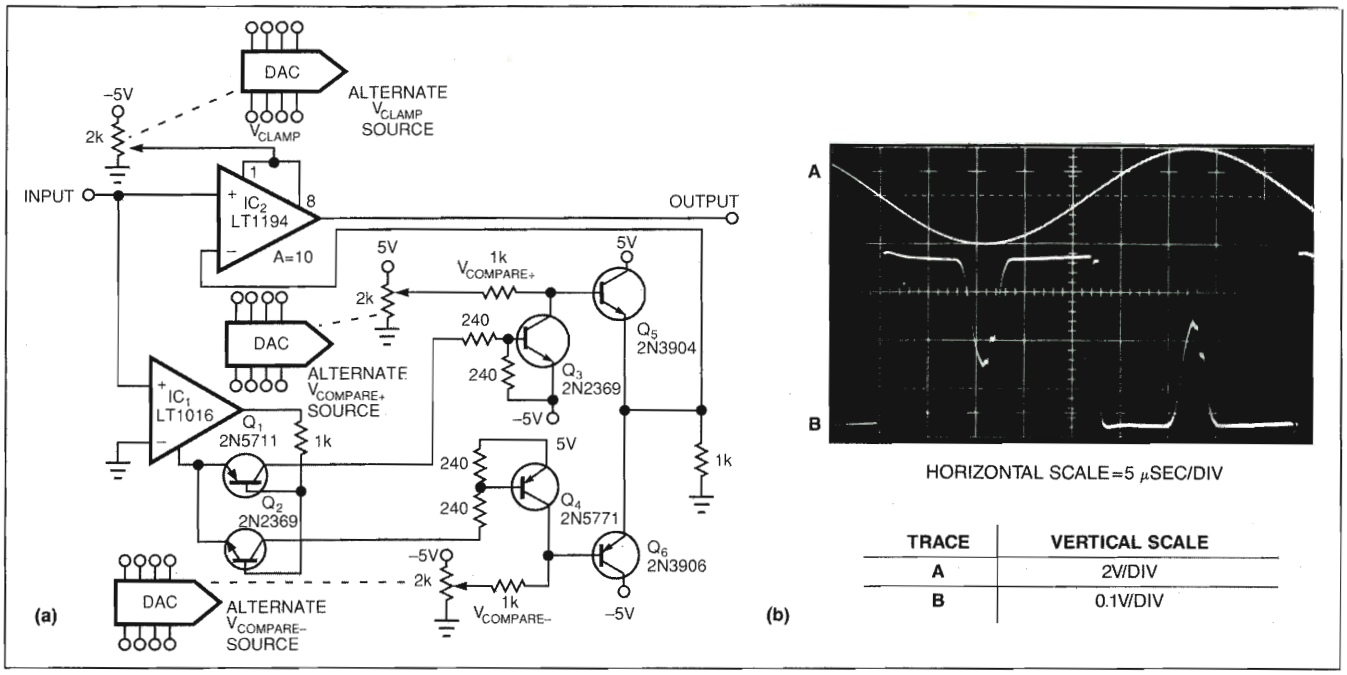



***Fig 7—By selectively amplifying*** *the portion of the signal you select, this differential-comparator amplifier* ***(a)*** *enables you to extract signal detail from a triangle waveform (****b****, trace A). At the triangle wave's peak (****b****, trace B), the triangle-wave generator's switching artifacts are clearly evident.*




| TRACE | VERTICAL SCALE |
|---|---|
| A | 2V/DIV |
| B | 0.1V/DIV |

***Fig 8—A differential-comparator amplifier (a) allows*** *you to observe signals between two amplitude-defined points that you can set. The amplifier detects switching residuals (**b**, trace B) in the sine-wave generator's input (**b**, trace A).*

It is worth noting that this circuit performs the same function as differential plug-in units for oscilloscopes. This circuit's output is accurate and settles to 0.1% within 100 nsec after entering its linear region.

## Window a waveform

**Fig 8a** extends the previous circuit's operation, allowing amplified observation of information between two amplitude-defined points that you can set. You can choose both the magnitude and sign of the amplitude setpoints. In this circuit, comparator $IC_1$'s output state determines the polarity of the offset applied to $IC_2$'s negative input. $IC_1$ compares the circuit's input to ground, generating polarity information at its outputs. Two level shifters, consisting of $Q_1$ and $Q_3$ and $Q_2$ and $Q_4$, bias followers $Q_5$ and $Q_6$. Positive circuit inputs result in $Q_5$ supplying the $V_{COMPARE+}$ potential to $IC_2$, whereas negative inputs route $V_{COMPARE-}$ to $IC_2$.

This additional circuitry eliminates the previous circuit's manual polarity switch, permitting automatic selection of the difference polarity and amplitude. Additionally, this circuit takes advantage of $IC_2$'s input-clamp feature. This feature limits the dynamic range of the input, clamping the amplifier's input operating range. Signals inside the clamp limit are processed normally, while signals outside the limit are precluded from influencing the amplifier. This combination of circuit controls allows you to select very tightly defined "windows" on a waveform for accurate amplification without overload restrictions.

**Fig 8b** shows the circuit output for a sine-wave input (trace A) from the same function generator used to test the previous circuit. The $V_+$ and $V_-$ compare voltages are set just below the sine-wave peaks, with $V_{CLAMP}$ programmed to restrict amplification to the peaks' excursion. Trace B, the circuit's output, simultaneously shows amplitude detail of both peaks of the sine wave. The observed distortion is directly traceable to this generator's imperfect internal triangle waveform (**Fig 7b**), as well as its sine-wave shaper characteristics.

Occasionally, it is necessary to supply larger output currents than an amplifier is capable of delivering. The power gain stage, sometimes called a booster, is usually placed within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics.

Because the output stage resides in the amplifier's feedback path, loop stability is a concern. This is particularly the case with high-speed amplifiers. You must consider the output stage's gain and ac characteristics to achieve good dynamic performance. Overall circuit phase-shift, frequency-response, and dynamic-load-handling capabilities are issues that you can't ignore when designing a power gain stage for a monolithic amplifier. The output stage's added gain and phase shift can cause poor ac response or outright oscillation. Judicious application of frequency-compensation methods is needed for good results. (See **Ref 1** for discussion and details on compensation methods.)

**Fig 9a** shows a 200-mA power booster used with a high-speed amplifier. Complementary emitter followers $Q_1$ and $Q_5$ provide current gain for positive signals, while $Q_2$ and $Q_6$ handle negative excursions. $Q_3$ and $Q_4$ are $V_{BE}$-based current limiters, turning on and thereby robbing drive from the appropriate output transistor when current exceeds about 300 mA. The diodes prevent reverse $V_{BE}$ at $Q_1$ and $Q_2$ during current limiting. The 100Ω resistor and ferrite beads prevent the low-impedance amplifier output from causing $Q_1$ and $Q_2$ to oscillate (**Ref 1**).

To be effective, the booster must be exceptionally fast. A slow design will obviate the ac performance of the amplifier by controlling it, or in the worst case, by causing oscillation (again, see Ref 1). **Fig 9b** shows booster performance with the amplifier removed from the circuit. The input pulse (trace A) is applied to the booster input, with the output (trace B) taken at the indicated spot. Evaluation of the photograph shows that booster rise and fall times are limited by the input pulse generator. Additionally, delay is in the 1-nsec range. This kind of speed makes the circuit a good candidate for acceptable ac performance within a fast amplifier's loop.

**Fig 9c** shows the pulse response with the LT1220 installed in the circuit driving a 50Ω load. The booster's high speed contributes negligible delay, and overall response is clean and predictable. The local 3-pF compensation across the amplifier optimizes response but is not absolutely necessary in this circuit. The input (trace A) produces a nicely shaped slew-limited output (trace B).

In theory, achieving higher power-booster stages than that of the circuit in **Fig 9** should be possible by utilizing bigger devices. This is partly the case, but wideband pnp power transistors aren't readily available. **Fig 10a** shows a way around this problem. The circuit is a 1A-output version of **Fig 9a**, with several differences. In the positive signal path, output transistor $Q_4$ is an RF power type, driven by Darlington-connected $Q_3$. The diode in $Q_1$'s emitter compensates for the additional $V_{BE}$ introduced by $Q_3$, thereby preventing crossover distortion.

The negative signal path substitutes the $Q_5$-$Q_6$ connection to simulate a fast pnp power transistor. Although this configuration acts like a fast pnp follower, it has voltage gain and tends to oscillate. The 2-pF feedback capacitor across $Q_5$'s collector and base suppresses these parasitic oscillations and stabilizes the composite transistor. This circuit also includes a feedback-capacitor trim to optimize ac response. This trim capacitor, which is not included in the previous circuit, is necessary because of this circuit's slightly slower characteristics and much heavier loading. Current-limit

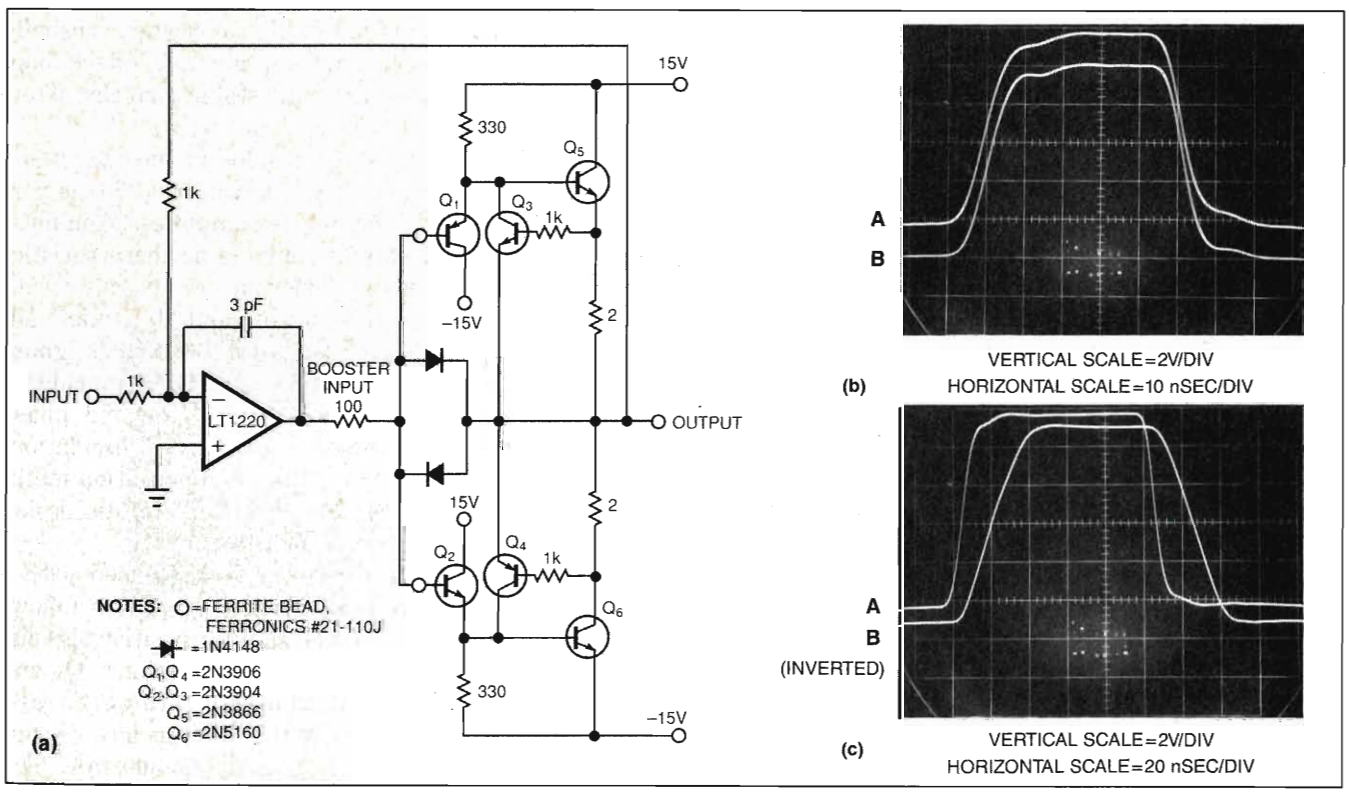



***Fig 9—An additional booster stage increases*** *the output of this circuit's wideband amplifier to 200 mA* ***(a)****. The response of the booster* ***(b****, trace B) alone to a pulse input* ***(b****, trace A) must be sufficiently fast not to limit the high-speed amplifier. The delay between trace A and B of* ***b*** *is approximately 1 nsec, and the pulse generator's rise and fall times limit those of the boost circuit. When included in the amplifier's feedback loop, the booster's high speed contributes negligible delay, and overall circuit response* ***(c****, trace B) is clean and predictable.*

operation and other characteristics are similar to the lower power circuit.

**Fig 10b** shows waveforms for a 10V negative input step (trace A) and a 10Ω load. The amplifier responds to the input (trace B), and drives the booster to whatever voltage is required to close the loop. The amplifier provides about 1.5V of overdrive to overcome the $V_{BE}$ drops of $Q_3$ and $Q_4$. The booster output, lagging by a few nsec (trace C), drives the load cleanly, with only minor peaking. Adjusting the 5- to 30-pF feedback capacitance trimmer minimizes the peaking. EDN

## Reference

1. Williams, Jim, "Subduing high-speed op-amp problems," *EDN*, October 24, 1991, pg 135.

## Author's biography

*For more information on this article's author, turn to pg 163 in the October 10, 1991, issue.*



## High-frequency-amplifier layout guidelines

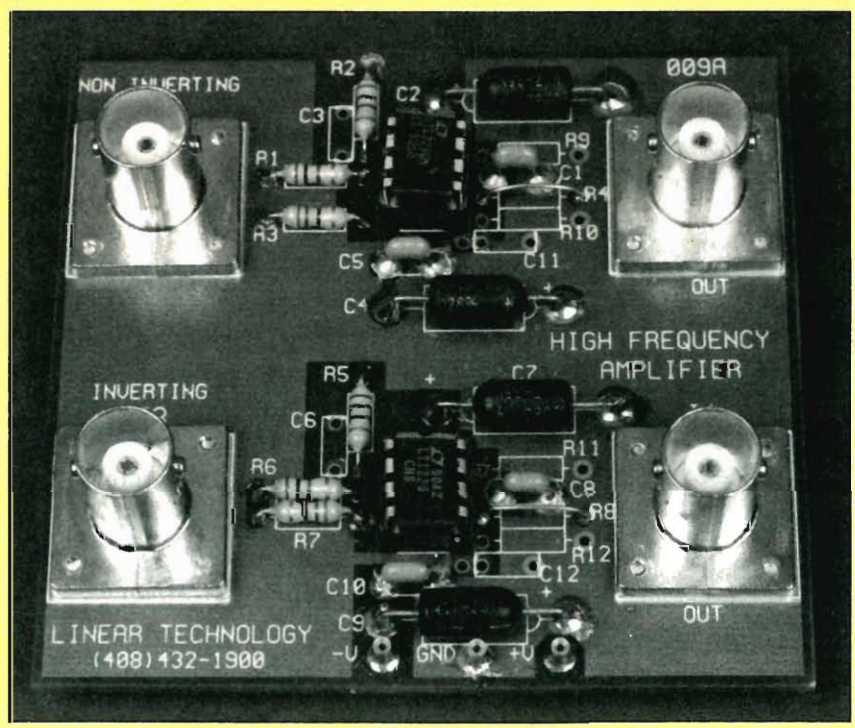
Layout is a primary contributor to the performance of any high-speed amplifier. Poor layout techniques adversely affect the behavior of a finished circuit. Several important layout techniques were applied in the construction of Linear Technology Corp's demo board 009 (**Fig A**), which simplifies the evaluation of voltage-mode and current-feedback high-speed op amps.

As should any high-frequency layout, the evaluation board pays attention to the following considerations:

1. Top-side ground plane: The primary task of a ground plane is to lower the impedance of ground connections. The inductance between any two points on a uniform sheet of copper is less than the inductance of a thin, straight trace of copper connecting the same two points. The ground plane approximates the characteristics of a copper sheet and lowers the impedance at key points in the circuit, such as the grounds of connectors and supply bypass capacitors.

2. Ground-plane voids: Certain components and circuit nodes are very sensitive to stray capacitance. Two good examples are the summing node of the op amp and the feedback resistor. Voids are put in the ground plane in these areas to reduce stray ground capacitance.

3. I/O matching: The width of the input and output traces is adjusted to a stripline impedance of 50Ω. Note that the terminating resistors, $R_3$ and $R_7$, are connected to the end of the input lines, not at the connector. While




***This demo board embodies** a number of layout techniques crucial to the performance of high-speed amplifiers: top-side ground plane, ground-plane voids around critical nodes, and proper bypassing.*

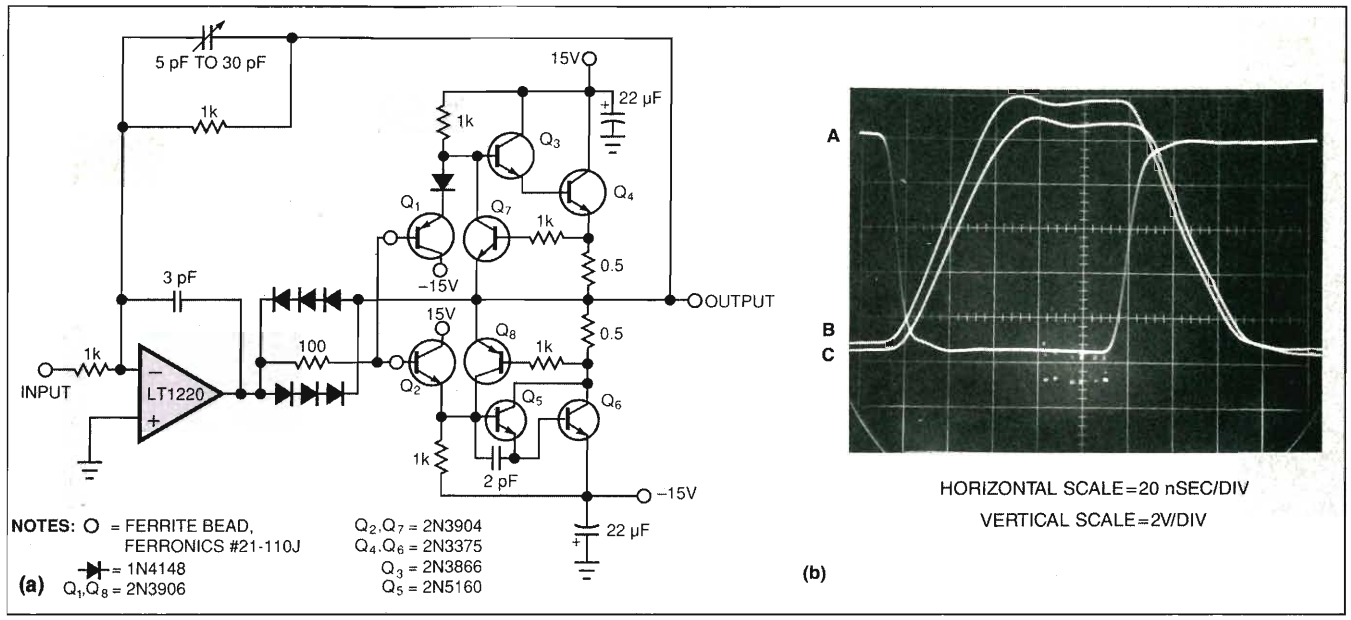



***Fig 10—$Q_5$ and $Q_6$ simulate*** *a fast pnp power transistor for this power booster* ***(a)****. The boosted op amp can drive a 1A load to 10V in 50 nsec. Trace A* ***(b)*** *is the 10V input, B is the op amp's output, C is the final circuit output.*

stripline techniques aren't absolutely necessary for the demo board, they are important on larger layouts where line lengths are longer. The short lines on the demo board can be terminated with 50, 75, or 93Ω without adversely affecting performance.

4. Separation of input and output grounds: Even though the ground plane exhibits a low impedance, input and output grounds are still separated. For example, the termination resistors, $R_3$ and $R_7$, and the gain-setting resistor, $R_1$, are grounded in the vicinity of the input connector. Supply bypass capacitors $C_1$, $C_2$, $C_4$, $C_5$, $C_7$, $C_8$, $C_9$, and $C_{10}$ are returned to ground in the vicinity of the output connectors.

5. Proper bypassing: High-speed op amps work best when you bypass their supply pins with RF-quality capacitors. For example, $C_1$, $C_5$, $C_8$, and $C_{10}$ should be 10-nF disc ceramic or other capacitors with self-resonant frequencies greater than 10 MHz. The polarized capacitors, $C_2$, $C_4$, $C_7$, and $C_9$, should be 1- to 10-µF tantalums. Most 10-nF ceramics are self-resonant well above 10 MHz, and 4.7-µF solid tantalums with axial leads are self-resonant at 1 MHz or below. Lead lengths are critical: The self-resonant frequency of a 4.7-µF tantalum drops by a factor of 2 when measured through 2-in. leads. Although a capacitor may become inductive at high frequencies, it is still an effective bypass component above resonance because the impedance is low.

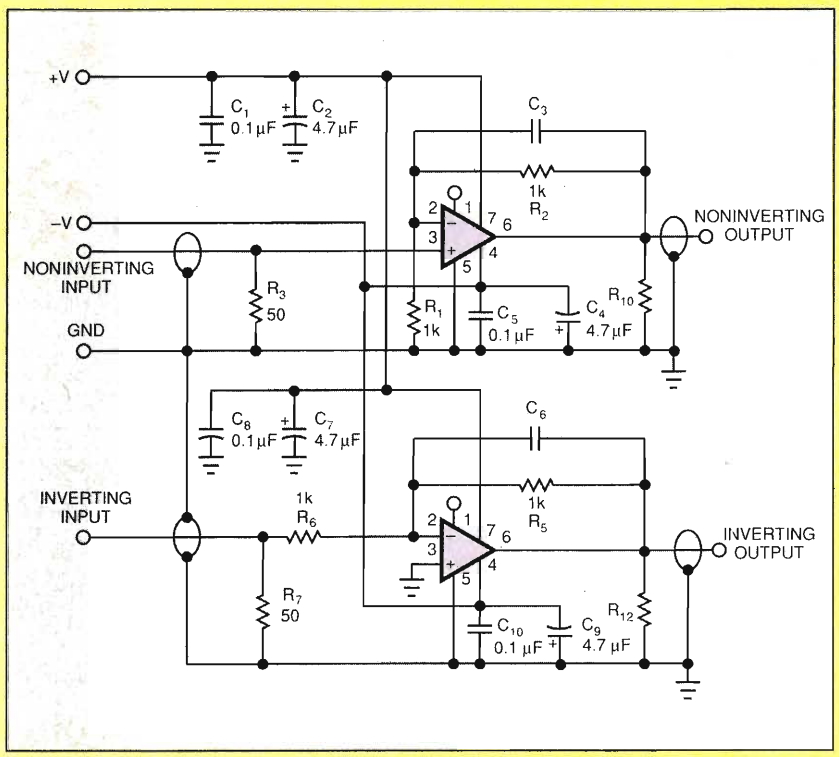



***Fig A—Mating the components of this schematic*** *to their placement on the demo board helps you visualize some high-frequency layout techniques and will help you transfer these techniques to your own high-speed boards.*

THE JIM WILLIAMS PAPERS

# High-speed amplifiers with low offset and drift

Amplifiers designed for wide bandwidth or fast settling often exhibit inferior characteristics at dc—that is, high voltage, current offset, and drift. Used with care, the techniques described here let you build circuits that exhibit exemplary performance from dc to MHz.

Jim Williams, *Linear Technology Corp*

Often, you must produce an amplifier circuit that has both the low offset of a dc amplifier and the wide bandwidth of a fast device. A number of techniques let you achieve such a result. Which method is best depends heavily on your application. Several circuits follow that you can study, build, and compare to determine what's best for you.

**Fig 1** shows a composite amplifier that consists of an LT1097 low-drift device ($IC_1$) and an LT1191 high-speed amplifier ($IC_2$). The overall circuit is a unity-gain inverter that has its summing node at the junction of the two 1-kΩ resistors. $IC_1$ monitors this summing node, compares it to ground, and drives $IC_2$'s positive input to complete a dc-stabilizing loop around $IC_2$. The 100-kΩ·0.01-μF time constant at $IC_1$ limits the amplifier's response to low-frequency signals. $IC_2$ handles high-frequency inputs, whereas $IC_1$ stabilizes the dc operating point. The 4.7-kΩ/220Ω divider at $IC_2$'s input prevents excessive overdrive during startup. This circuit combines $IC_1$'s 35-μV offset and 1.5-μV/°C drift with $IC_2$'s 450V/μsec slew rate and 90-MHz bandwidth. Bias current, dominated by $IC_2$, is about 500 nA.

**Fig 2** is similar, except that the sensing is differential, preserving access to both of the fast amplifier's inputs. $IC_1$ measures the dc error at $IC_2$'s input terminals and biases $IC_2$'s offset pin to force the offset to within 50 μV. $IC_2$'s offset-pin biasing arrangement always lets $IC_1$ find the servo point. The 0.01-μF capacitor rolls off $IC_1$'s gain at low frequencies, and $IC_2$ han-

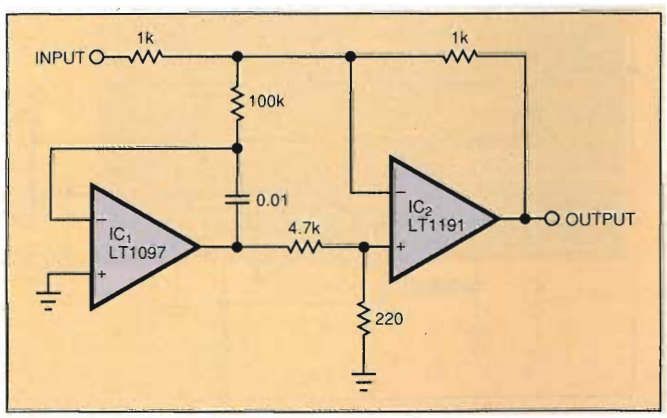



***Fig 1—An integrator ($IC_1$) reduces the drift of a wideband amplifier ($IC_2$) by applying a signal to the wideband amplifier's noninverting input. That signal holds the wideband amplifier's summing junction at ground.***

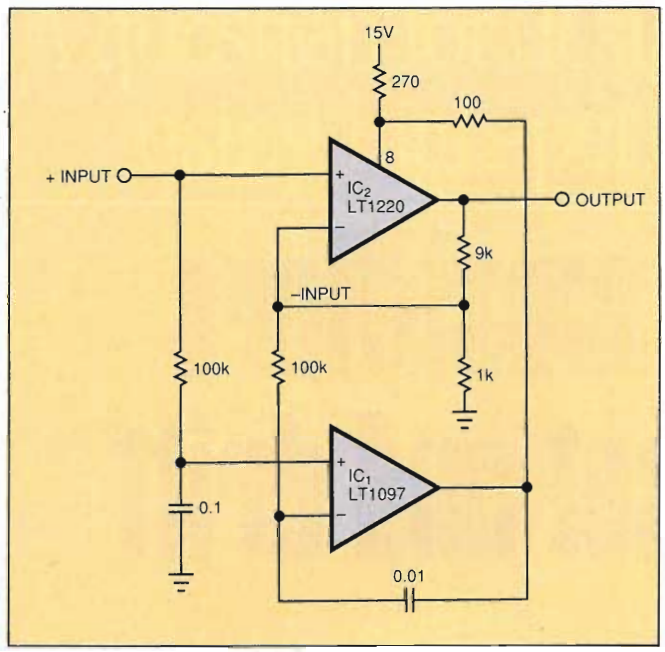



***Fig 2—You can also stabilize the offset*** *of a wideband amplifier ($IC_2$, in this case) by using a precision dc amplifier ($IC_1$) to apply correcting signals to the wideband amplifier's offset-trim adjustment pin.*

dles high-frequency signals. The combined characteristics of these amplifiers yield an offset voltage of 50 μV, an offset drift of 1 μV/°C, a slew rate of 250 V/μsec, and a gain bandwidth of 45 MHz.

**Fig 3** shows wideband, highly stable gain-of-10 amplifier with high input impedance. The input capacitance is about 3 pF. Because of its low input capacitance and low (100 pA) bias current, the circuit is well suited for use in probing IC wafers or as a pin amplifier in automatic-test systems.

$Q_1$ and $Q_2$ constitute a simple, high-speed FET-input buffer. $Q_1$ functions as a source follower, and the $Q_2$ current-source load sets the drain-to-source channel current. $IC_2$ provides a gain of 10 with 100-MHz bandwidth. Normally, this open-loop configuration would drift unacceptably because there is no dc feedback. $IC_1$, by comparing the filtered circuit output to a similarly filtered version of the input signal, provides the feedback to stabilize the circuit. The amplified difference between these signals sets $Q_2$'s bias—and hence $Q_1$'s channel current—thereby forcing $Q_1$'s $V_{GS}$ to match the circuit's input and output potentials. The capacitor around $IC_1$ provides stable loop compensation. The R-C network in $IC_1$'s output prevents that output from seeing high-speed edges coupled through $Q_2$'s collector-base junction.

**Fig 4a** shows a way to combine wide bandwidth with true differential inputs and dc stabilization. $IC_1$ and $IC_2$ sense the input differentially at gains of 10. Wideband amplifier $IC_1$ feeds high-frequency signals to output amplifier $IC_3$ via a highpass network. Low-frequency and dc information get to $IC_3$ via the slower $IC_2$. The 2-kΩ/200-pF lowpass networks remove the input signal's high-frequency components, so only lower frequencies reach $IC_2$. Because the gain and bandwidth of the high- and low-frequency paths complement each other, $IC_3$'s output is an undistorted, amplified version of the input (see **Fig 4b**, trace D.)

**Fig 4b**, trace A is one side of a differential input signal applied to the circuit. Trace B is $IC_1$'s output

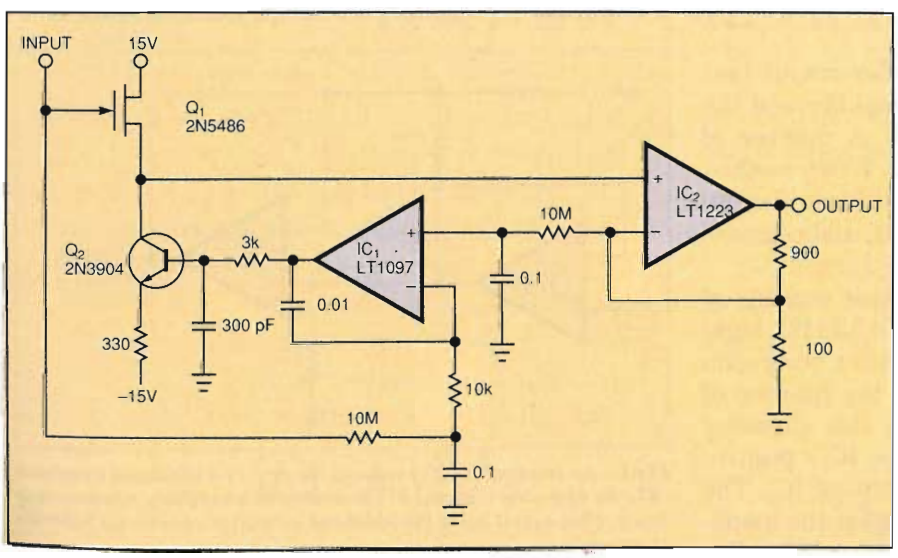



***Fig 3—An integrator ($IC_1$)*** *drives a current source ($Q_2$), which biases a FET ($Q_1$) that completes a dc feedback loop around $IC_2$ to stabilize the amplifier's operation at dc.*

taken at the junction of the 500Ω potentiometer and 0.001-μF capacitor. Trace C is $IC_2$'s output. With the "ac-gain" and "dc-gain-match" trims properly adjusted, the two paths' contributions match up and trace D is clean, with no residual artifacts. You can optimize the adjustments by trimming the ac gain for the squarest corners and the dc-gain match for a flat top. Bandwidth for this circuit exceeds 35 MHz; slew rate is 450V/μsec; and dc offset is about 200 μV.

### Parallel paths yield the best of two worlds

**Fig 5a** shows a very powerful extension of the previous circuit. The circuits operate similarly, but this one has a gain of 1000; its bandwidth is about 35 MHz; its rise time is 7 nsec; and its delay is less than 7.5 nsec. Full-power response is available to 10 MHz, and broadband input noise is about 15 μV. This kind of speed, coupled with true differential inputs, a gain of 1000, high dc stability, and low cost make the circuit broadly applicable in wideband instrumentation.

As before, two differential amplifiers, $IC_1$ and $IC_2$, simultaneously sense the inputs. In this case, $IC_1$ is a 592-733 type operating at a gain of 100. Its differential outputs feed output amplifier $IC_3$ via 1-μF/1-kΩ high-pass networks that strip out the dc content of $IC_1$'s output. $IC_2$, a precision dc differential amplifier, operates in similar fashion to its counterpart in the previous circuit, supplying dc and low-frequency information to $IC_3$ at a trimmed gain of 100.

In this case, the output amplifier, $IC_3$, is not a follower but a differential-input/single-ended-output gain block whose nominal gain is 10. This change is necessary because $IC_1$'s differential output must become a single-ended signal to provide the circuit's final output. Consequently, $IC_2$ does not directly apply its low-frequency information to $IC_3$ as it did before. Instead, $IC_4$ measures the difference between $IC_2$'s output and a fraction of $IC_3$'s output. $IC_4$'s output, biasing $IC_3$'s positive input via the 1-kΩ resistor, closes a loop around the circuit's dc and low-frequency path. To make the circuit's dc gain equal to its ac gain, you adjust the divider that feeds $IC_4$'s negative input.

**Fig 5b** shows the circuit's response to a 60-nsec, 2.5-mV pulse, trace A. The ×1000 output, trace B, responds cleanly, with both delay and rise time in the 5- to 7-nsec range. Some small amount of overshoot is evident, but you can trim the overshoot with the peaking adjustment at $IC_1$. **Fig 5c** plots the circuit's gain vs frequency. The gain is flat within 0.5 dB to 20 MHz, with the −3 dB point at 40 MHz. The overshoot of **Fig 5b** shows up here as a very slight gain increase starting around 1 MHz and continuing to about 15 MHz. The peaking adjustment eliminates this effect.

To use this circuit, apply a low-frequency or dc signal of known amplitude and adjust the low-frequency gain to ×1000 after the output has settled. Next, adjust the high-frequency gain so that the signal's leading and trailing corners have amplitudes identical to those

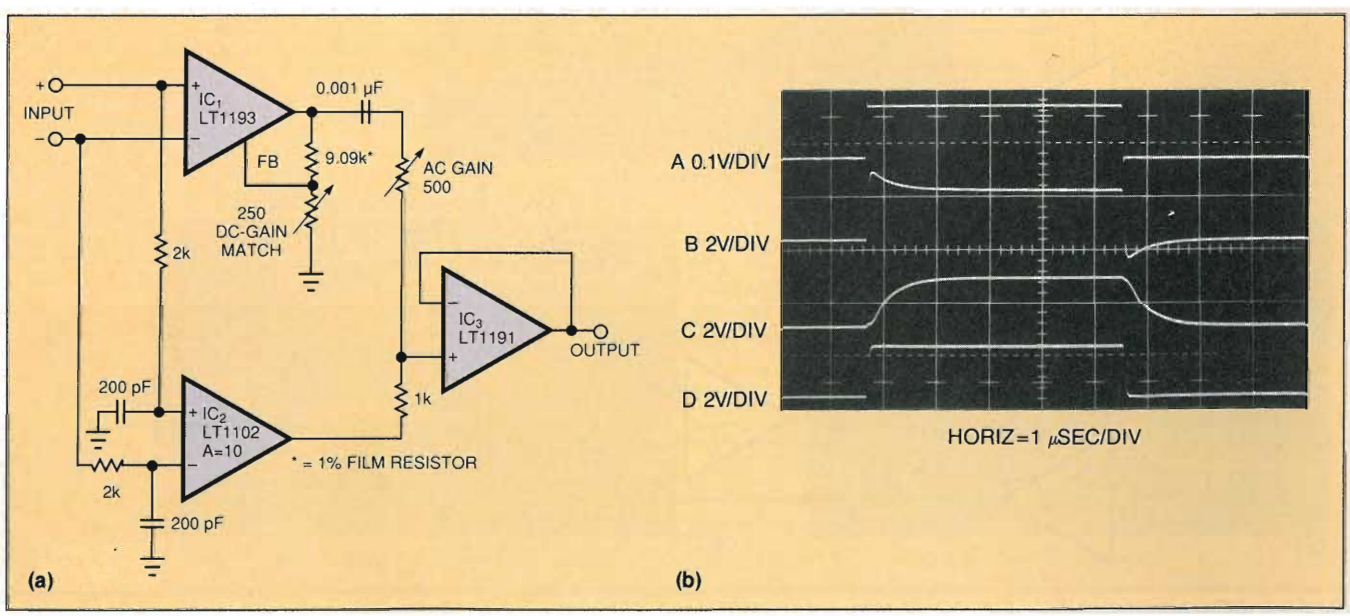



***Fig 4—Parallel paths** for ac and dc signals **(a)** provide low offset and good dynamic response—if you correctly adjust the trims (**b**, trace D).*

of the settled portion. Finally, trim the peaking adjustment for the best settling of the output pulse's corners.

**Fig 5d** shows the input (trace A) and output (trace B) waveforms with all adjustments properly set. The fidelity is excellent, with no aberrations or other artifacts of the parallel-path operation evident. **Fig 5e** shows the effects of too much ac gain; excessive peaking on the edges, with proper amplitude achieved only after the dc channel takes control of the output. Similarly, excessive dc gain produces **Fig 5f**'s traces. The ac-gain path provides proper initial response, but too much dc gain forces a long, tailing response that finally settles at an incorrect amplitude.

The use of parallel-path schemes to simultaneously achieve wide bandwidth and outstanding dc performance isn't new. In fact, it predates the use of low-drift bipolar differential gain stages. The first parallel-path amplifiers achieved dc stability by using electromechanical choppers to convert dc to ac. Gain stages consisting first of vacuum tubes and later of Germanium transistors amplified the chopped dc. Synchronous rectifiers converted the ac back to dc. AC-coupled amplifi-

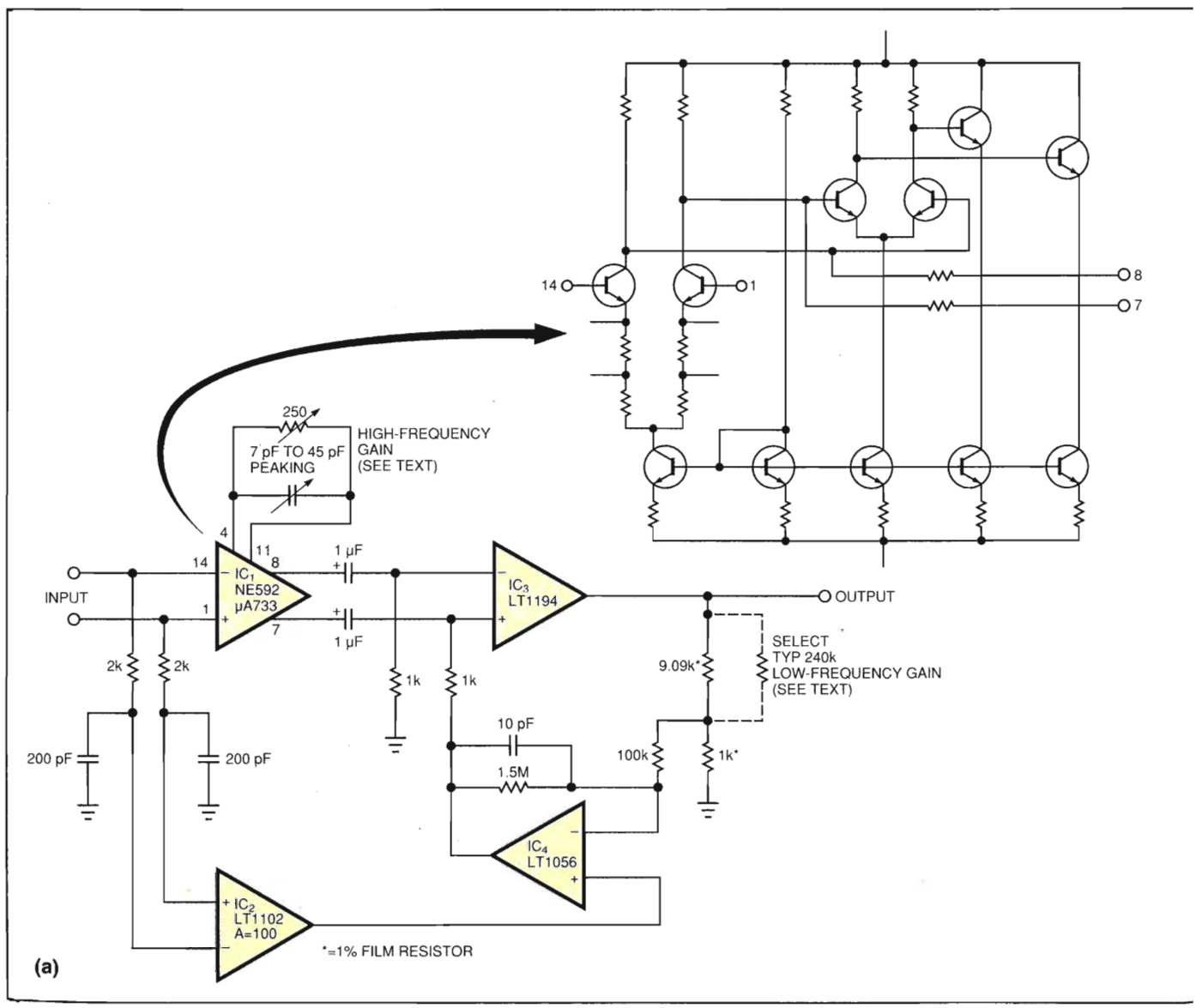



***Fig 5—A differential-to-single-ended gain of 1000** with 38-MHz bandwidth and excellent dc characteristics results from extending the parallel-path architecture, **(a)**. The pulse response (**b**, trace B) shows a minimum of overshoot, which is reflected in the frequency response*

ers in parallel with the chopper amplifiers provided good bandwidth. As **Figs 5e** and **5f** illustrate, these schemes have historically had a problem in many applications that demand the best at both dc and high frequencies: Unless you carefully match the dc and ac gains, the amplifiers' response to an input voltage step exhibits a long "tail." Keeping the response free of such tails over wide temperature ranges and long periods of time has always presented a challenge. Modern components make meeting that challenge easier, but the challenge still exists. EDN

## Author's biography

*For more information on this article's author, turn to page 163 in the October 10, 1991, issue.*

**Article Interest Quotient (Circle One)**
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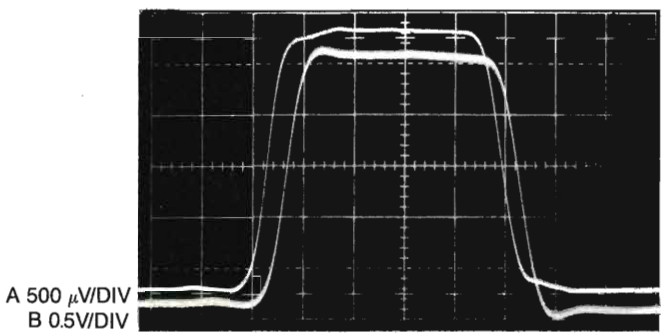


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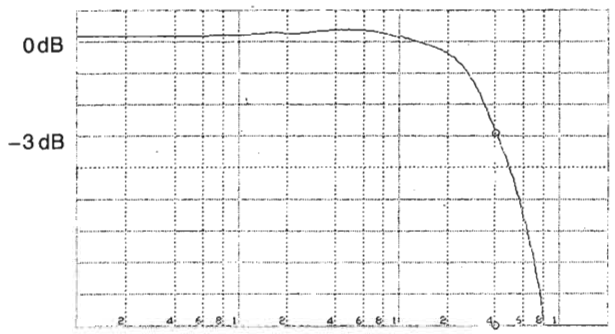


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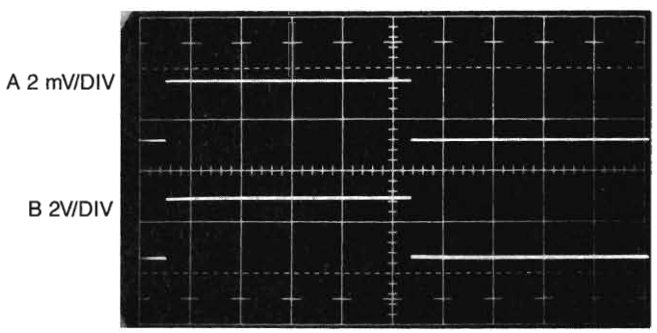


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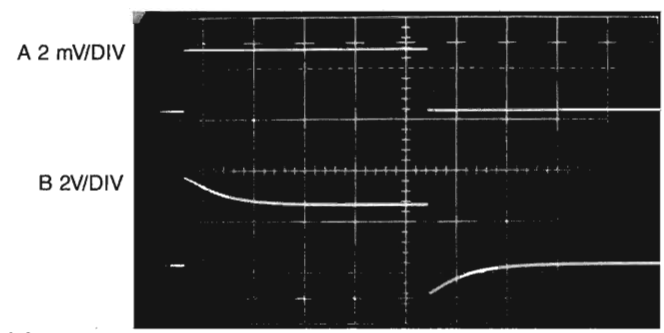


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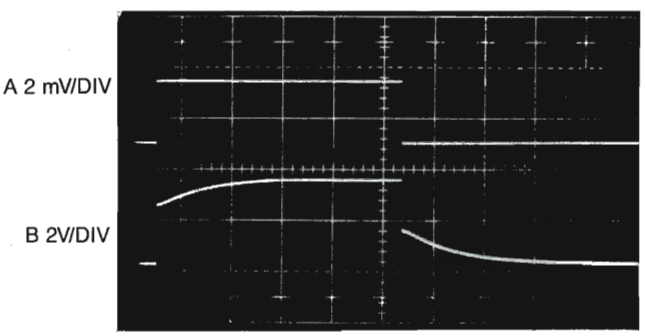


(f)

*(c) as a slight peak near 6 MHz. In the other three photos, (d, e, and f), you see, respectively, the effects of correctly matching the ac and dc gains, setting the ac gain too high, and setting the dc gain too high.*

THE JIM WILLIAMS PAPERS

# Subduing high-speed op-amp problems

The application of high-speed op amps requires special attention to a multitude of potential problems. You need to guard against noise intrusion, capacitance-loading effects, and parasitic conductive paths—without neglecting the compromises you may have to make between compensation and gain.

Jim Williams, *Linear Technology Corp*

Compared with their low-speed siblings, high-speed op amps are subject to many problems, many of which can result in oscillation. The forte of the operational amplifier is negative feedback, which stabilizes the operating point and fixes the gain. However, positive feedback or delayed negative feedback can cause oscillation. Thus, even a properly functioning amplifier constantly lives in the shadow of oscillation.

When oscillation occurs, several major candidates for blame are present. If the power supply is unbypassed, the impedance the amplifier sees at its power terminals is high, particularly at high frequency. This impedance forms a voltage divider with the amplifier, letting the supply vary as internal conditions in the amplifier change. This variation can cause local feedback, resulting in oscillation. The obvious cure is to bypass the amplifier. Power-supply impedance must be low to ensure stable operation.

A second common cause of oscillation is positive feedback. In most amplifier circuits feedback is negative, although the circuit may also use controlled amounts of positive feedback. In a circuit that normally has only negative feedback, unintended positive feedback may occur with poor layout. Check for possible parasitic feedback paths and unwanted or overlooked feedback action. To the extent possible, minimize the impedances seen by the amplifier inputs. A low impedance helps to attenuate the effects of parasitic feedback paths to the inputs. Similarly, minimize exposed input-trace area. Route the amplifier outputs and other signals well away from sensitive nodes. Sometimes no amount of layout finesse will work, and shielding is required. Use shielding only when required—extensive shielding is a sloppy substitute for good layout practice.

### Watch out for time delays

A third cause of oscillation is negative feedback that arrives significantly delayed in time. Under these conditions, the amplifier hopelessly tries to servo-control a feedback signal that consistently arrives "too late." The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point. The most common causes of this problem are reactive loading of the amplifier (most notably capacitive loads such as cable) and circuitry (such as power amplifiers) within the amplifier's feedback path. In many cases, isolating the reactive load from the amplifier's output (and feedback path) with a resistor will solve the problem. Sometimes rolling off the amplifier's frequency response will fix the problem, but in high-speed circuits this may not be an option.

Placing power-gain or other types of stages within

the amplifier's feedback path adds time delay to the stabilizing feedback. If the delay is significant, oscillation commences. Stages operating within the amplifier's loop should have a minimum time lag compared with the amplifier's speed capability. At lower speeds, this is not too difficult, but a stage within a 100-MHz amplifier's loop must be fast. As mentioned before, rolling off the amplifier's frequency response eases the job, but is usually undesirable in a wideband circuit. You should make every effort to maximize the bandwidth of the added stages before resorting to amplifier roll-off. In this way, you can achieve the fastest overall bandwidth while maintaining stability. (See the **box,** "The oscillation problem and frequency compensation," which discusses power-gain stages and other types of stages operating within amplifier loops.)

In certain cases, it may appear that there is an oscillation problem when there really isn't. For example, the low-level, square-wave output in **Fig 1** appears to suffer from parasitic oscillation. In actuality, the disturbance is typical of that caused by fast digital clocking or switching-regulator noise getting into critical circuit nodes. Plan for parasitic radiative or conductive paths and eliminate them with appropriate layout and shielding.

The **Fig 2** display underscores the previous statement. The scope trace shows the output from a gain-often inverter with a 1-kΩ input resistance. The output exhibits severe peaking induced by only 1-pF of parasitic capacitance across the 1-kΩ resistor. The 50Ω-terminated input source provides only 20 mV of drive, but that's more than enough to cause problems, even with only 1 pF of stray coupling. In this case the solution was a ground-referred shield at a right angle to, and encircling, the 1-kΩ resistor. Plan for parasitic radiative paths and eliminate them with appropriate shielding.

### Too low a gain can cause problems

A decompensated amplifier running at too low a gain produced the oscillation shown in **Fig 3.** The penalty for a decompensated amplifier's increased speed is a restriction on the minimum allowable gain. Decompensated amplifiers are simply not stable below some (specified) minimum gain, and no amount of wishful thinking will change this. Such oversight is common with these devices, although the amplifier never fails to remind the user. Observe gain restrictions when using decompensated amplifiers.

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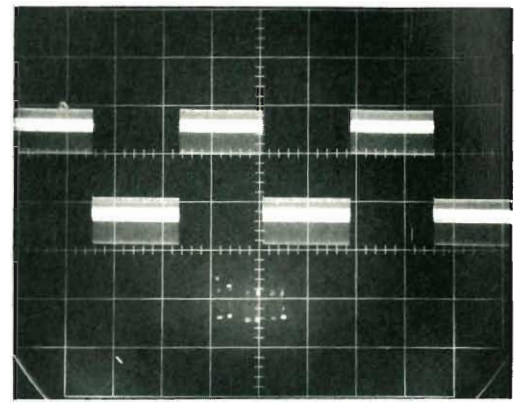


***Fig 1—This square-wave output disturbance*** *is typical of switching-regulator noise at critical circuit nodes. Poor layout is the culprit.*

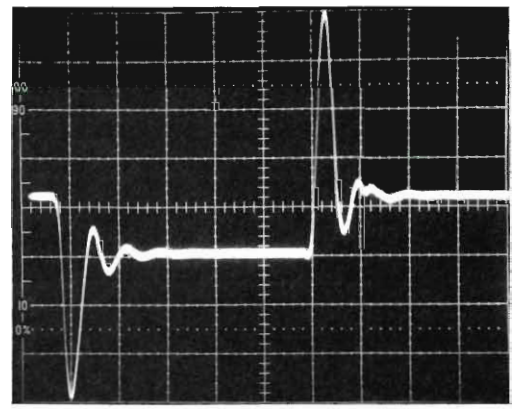


***Fig 2—The peaking and ringing at the output of a 10× amplifier*** *is the result of only 1 pF of stray capacitance across a 1-kΩ input resistor.*

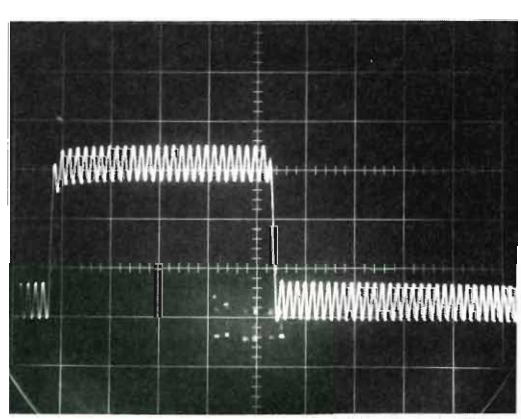


***Fig 3—A decompensated amplifier running at low gain*** *produced this oscillation. Such amplifiers are not stable below a specified minimum gain.*

# The oscillation problem and frequency compensation

All feedback systems have the propensity to oscillate. Basic theory tells us that an oscillator requires both gain and phase shift. Unfortunately, feedback systems, such as operational amplifiers, also have gain and phase shift. The close relationship between oscillators and operational amplifiers requires careful attention when designing op-amp circuits. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when you apply feedback. Furthermore, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This phase shift is why feedback-loop-enclosed stages can cause oscillation.

A large body of complex mathematics describing stability criteria is available, and is useful in predicting the stability characteristics of feedback amplifiers. For sophisticated applications, this complex approach is essential for optimum performance. However, comparatively little information is available that discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. The following is a practical approach to stabilizing various combinations of amplifier and power-gain stages, although the considerations are also useful to other feedback systems.

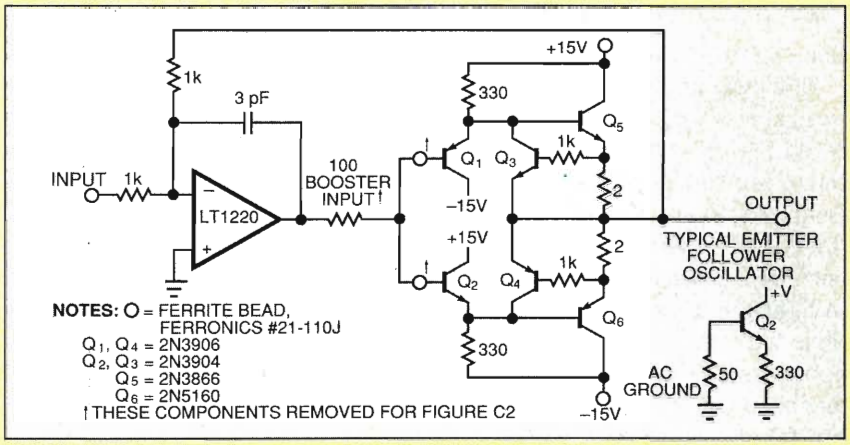


***Fig A—In this booster circuit**, the 100Ω resistor and the ferrite beads at the inputs of $Q_1$ and $Q_2$ play a critical role in maintaining stability.*

## Two categories exist

Oscillation problems in amplifier/power-booster combinations fall into two broad categories: local and loop oscillations. *Local* oscillations can occur in the booster stage, but should not appear in the IC op amp, which presumably was debugged prior to sale. These oscillations are the result of transistor parasitics, layout problems, or circuit-configuration instabilities. The oscillations are usually relatively high in frequency, typically in the 0.5- to 100-MHz range. Usually, local booster-stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation.

**Fig A** furnishes an instructive example. The $Q_1$ and $Q_2$ emitter-follower pair has a reasonably high $f_T$. These devices will oscillate if driven from a low-impedance source (**Refs 1** and **2**). To prevent problems, the 100Ω resistor and the ferrite beads are included to make the op amp's output look like a higher impedance. $Q_5$ and $Q_6$, also emitter followers, have an even higher $f_T$, but 330Ω sources drive them, eliminating the oscillation problem. The **Fig B** photo shows the action of the **Fig A** circuit without the 100Ω resistor and the ferrite beads. Trace A is the input, and Trace B is the output. The resultant high-frequency oscillation is typical of locally caused disturbances. Note that the major loop

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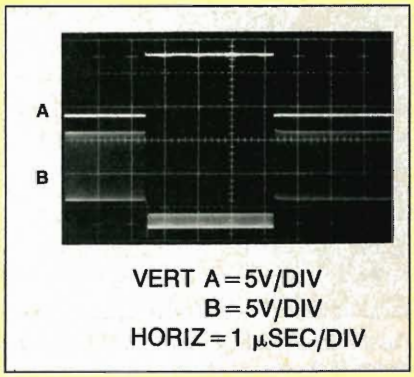


***Fig B—Removing the 100Ω resistor and the ferrite beads** from the **Fig A** circuit results in local oscillations, such as those shown here.*

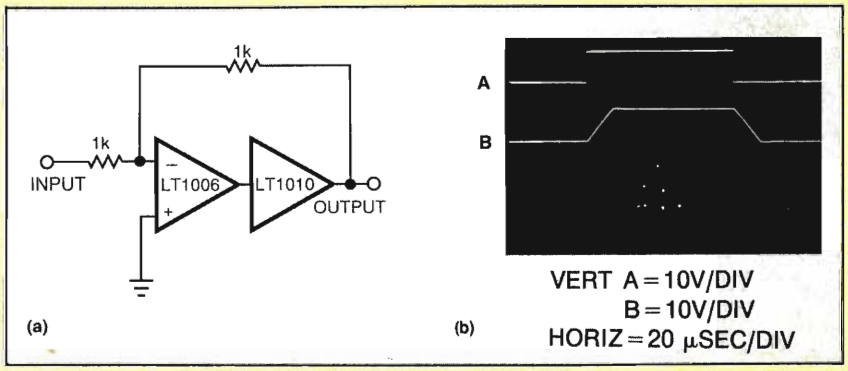


***Fig C—This slow op amp and medium-speed booster (a)** produced the stable output shown in **b**.*

## The oscillation problem and frequency compensation *(continued)*

is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high $f_T$ transistors unless they are needed. When high-frequency devices are in use, plan the layout carefully. In very stubborn cases, it may be necessary to lightly bypass transistor junctions with small capacitors or RC networks. Circuits that use local feedback can sometimes require careful transistor selection. For example, transistors operating in a local loop may require different $f_T$s to achieve stability. Emitter followers are notorious sources of oscillation, and should never be directly driven from low-impedance sources.

*Loop* oscillations are caused when the added gain stage supplies enough delay to cause substantial phase shift. This shift causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain, combined with the added delay, causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10 Hz to 1 MHz. A good way to eliminate loop-caused oscillations is to limit the gain-bandwidth of the control amplifier. If the booster stage has a higher gain-bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When the control amplifier's gain-bandwidth dominates, oscillation is ensured. Under these conditions, the control amplifier hopelessly tries to servo-control a feedback signal that consistently arrives too late, and the oscillation centers around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations, it is preferable to brutally force the compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling-off the control amplifier's gain-bandwidth. The feedback capacitor serves to trim only the step response; do not rely on it to stop outright oscillation.

**Fig C** illustrates these issues. The LT1006 amplifier used with the LT1010 current buffer produces the output shown in **Fig Cb**. As before, trace A is the input, and trace B is the output. The LT1006 has less than 1-MHz gain-bandwidth. The LT1010's 20-MHz gain-bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1006's internal roll-off is well below that of the output stage, and stability is achieved with no external compensation components. **Fig Da** uses the LT1223, which has a 100-MHz bandwidth, as the control amplifier. **Fig Db** shows the results. Here, the control amplifier's roll-off is well beyond the output stages, causing problems. The phase shift through the LT1010

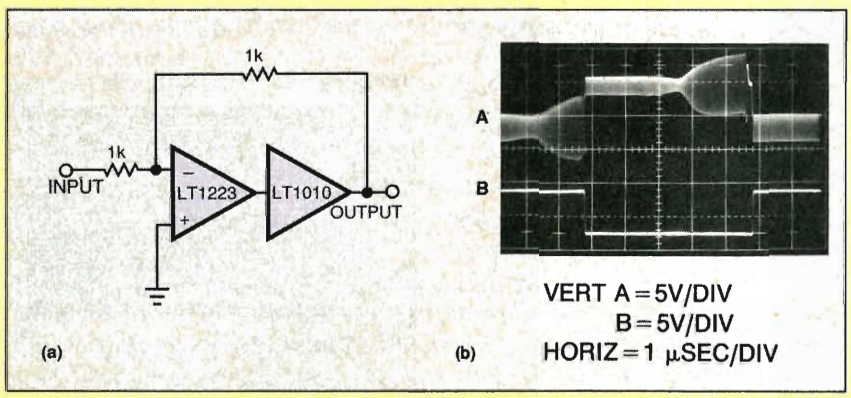


***Fig D—This fast op amp and medium-speed booster (a)*** *produced the oscillations shown in* ***b****.*

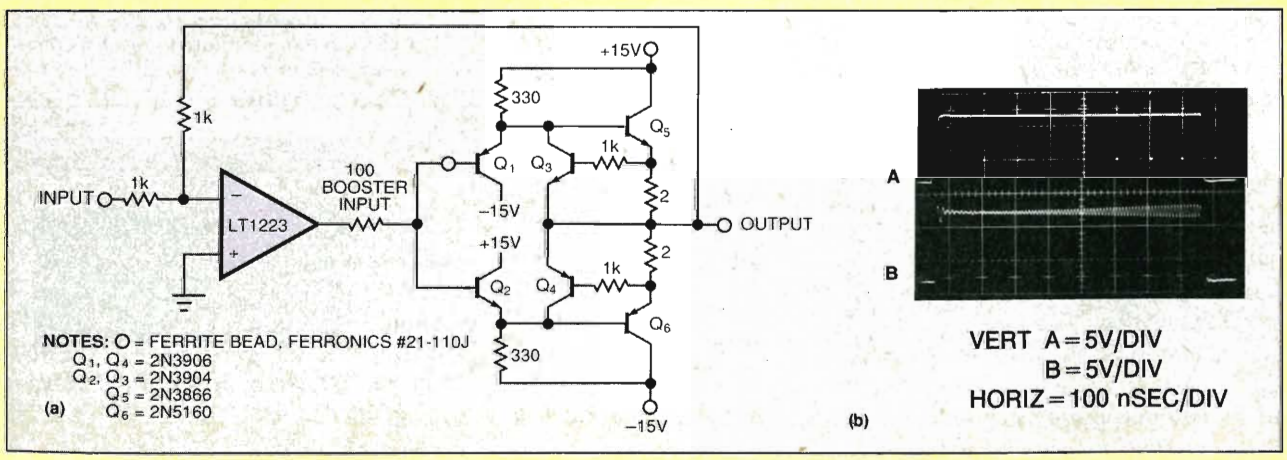


***Fig E—The fast amplifier and fast booster combination in a*** *attempts to correct the problems in the* ***Fig Da*** *circuit. Although the result is an improvement, the 100-MHz oscillation indicates that the booster stage is still too slow for the op amp* ***b****.*

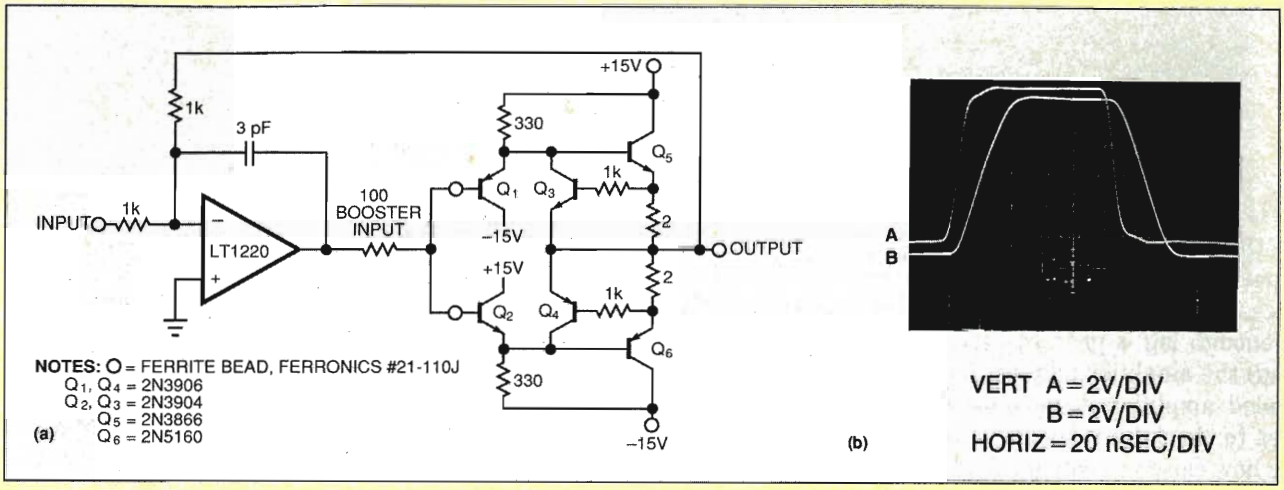


***Fig F—This circuit (a) produces more pleasing results than Fig Ea's circuit.*** *The 45-MHz LT1220 replaces the 100-MHz LT1223. The slower amplifier now works well with the booster stage in its loop. The circuit is well controlled, with no sign of oscillation (**b**).*

is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the control amplifier's gain-bandwidth.

The fact that the slower op-amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is free. The faster amplifier requires roll-off components for stability. Practically, the LT1223's speed is simply too fast for the LT1010. A somewhat slower amplifier is the way to go. Alternatively, you could use a faster booster. The circuit of **Fig Ea** attempts using this faster booster, but doesn't quite make it. Although the result (**Fig Eb**) is less corrupted than before, the 100-MHz oscillation indicates that the booster stage is still too slow for the LT1223.

Nearly identical to **Fig Ea**, the **Fig Fa** circuit produces more pleasant results. Here, the 45-MHz LT1220 replaces the 100-MHz LT1223. The slower amplifier, combined with minimum (3 pF) local compensation, works well with the booster stage in its loop. The result (**Fig Fb**) is a high-speed output that is well controlled, with no sign of oscillations.

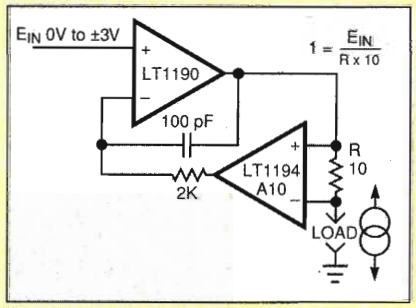


***Fig G—This current source** uses a 40-MHz LT1194 with a gain of 10 and a 50-MHz LT1190. The 100-pF feedback capacitor ensures a fast, stable loop.*

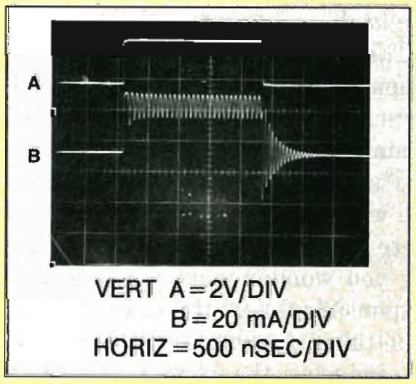


***Fig H—Removing the 100-pF feedback capacitor** from the **Fig G** circuit subjects the op amp to phase-shifted feedback, causing the oscillation shown here. Put that capacitor back in.*

Power boosters are not the only things you can place within an amplifier's feedback loop. The **Fig G** current source is an interesting variation. There is no power booster in the loop, but rather a 40-MHz differential amplifier with a gain of 10. For stability, the circuit uses the 50-MHz LT1190. The local 100-pF feedback slows it down a bit more, and the loop is fast and stable. What happens if you remove the 100-pF feedback path? **Fig H** shows that the loop is no longer stable, because the LT1190 control amplifier cannot servo-control the phase-shifted feedback at the higher frequency. So, put that 100-pF capacitor back in.

Even if you broke the output-input connection between the LT1190 and the LT1194 and inserted a booster stage, the circuit would still be stable—if you retained the 100-pF feedback capacitor. This tells us that the control amplifier doesn't care what generates the causal feedback between its input and output, as long as there isn't excessive delay.

When compensating loops like these, remember to investigate the effects of various loads and operating conditions. Sometimes a compensation scheme that appears to be proper gives bad results for some conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

Oscillation is also the problem illustrated in **Fig 4**. In this case, the oscillation is a result of excessive capacitive loading. Capacitive loading to ground introduces a lag in the feedback signal's return to the input. If enough lag is present (because of a large capacitive load) the amplifier may oscillate. Even if a capacitively loaded amplifier doesn't oscillate, it's always a good idea to check its response with step testing. It's amazing how close you can get to the edge of the cliff without falling off, except when you build 10,000 production units. Avoid capacitive loading. If such loading is necessary, check performance margins, and isolate or buffer the load.

The **Fig 5** waveform appears to be one cycle of oscillation. The output initially responds, but abruptly reverses direction, overshoots, and then heads positive again. Some overshoot again occurs, with a long tail and a small dip well before a nonlinear slew returns the waveform to zero. Ugly overshoot and tailing complete the cycle. This is certainly strange behavior, making you wonder what is going on. The input pulse is responsible for all these anomalies. The pulse's amplitude takes the amplifier outside its common-mode limits, inducing the bizarre effects shown. Keep inputs within the specified common-mode limits at all times.

**Fig 6** shows an oscillation-laden output (trace B) trying to unity-gain invert the input (trace A). The input's form is distinguishable in the output, but corrupted with very high-frequency oscillation and overshoot. In this case, the amplifier includes a booster within its loop to provide increased output current. The disturbances noted are traceable to local instabilities within the booster circuit. When using output booster stages, make sure they are inherently stable before placing them inside an amplifier's feedback loop. Wideband booster stages are particularly prone to device-level parasitic, high-frequency oscillation.

The booster-augmented, unity-gain inverting op amp in **Fig 7** also oscillates, but at a much lower frequency. Overshoot and nonlinear recovery dominate the waveform's envelope. Unlike the previous example, this behavior is not caused by local oscillations within the booster stage. Instead, the booster is simply too slow for the op-amp's feedback loop. The booster introduces enough lag to force oscillation, even as it hopelessly tries to maintain loop closure. Make sure that booster

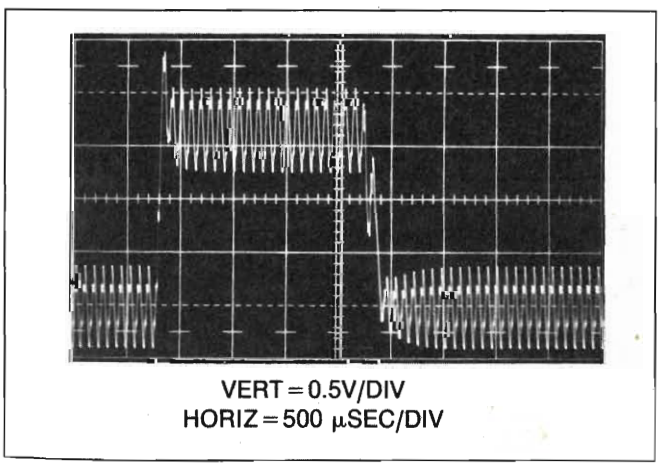


***Fig 4—The oscillation shown here** is the result of excessive capacitive loading, which causes a lag in the feedback to the input of the amplifier.*

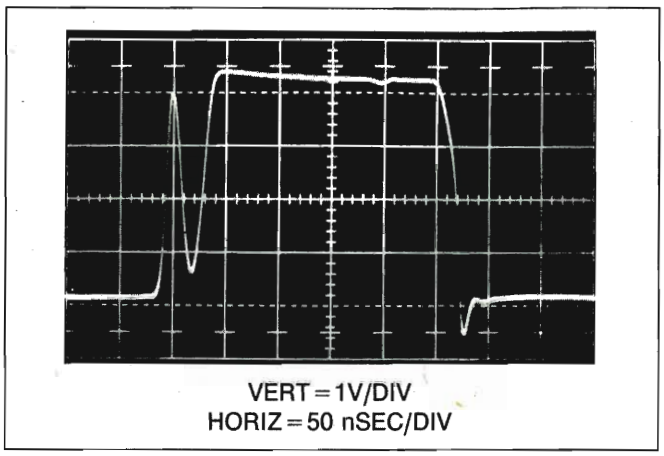


***Fig 5—What appears to be one cycle of oscillation** is actually the result of a high-amplitude pulse that exceeds the common-mode range of the amplifier.*

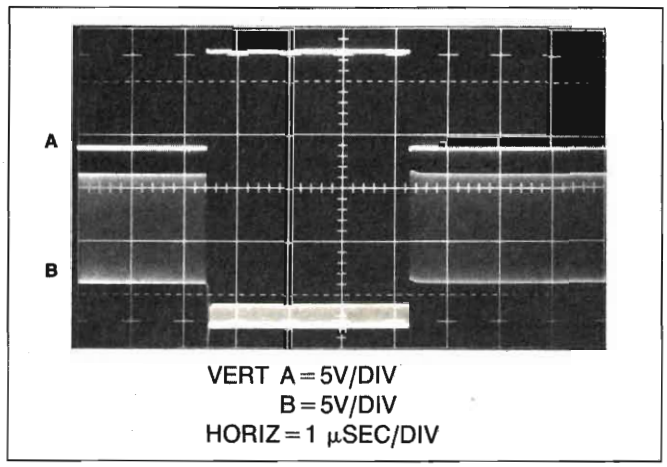


***Fig 6—Local oscillation in a booster stage** produced this result. Wideband booster stages are prone to high-frequency parasitic oscillation.*

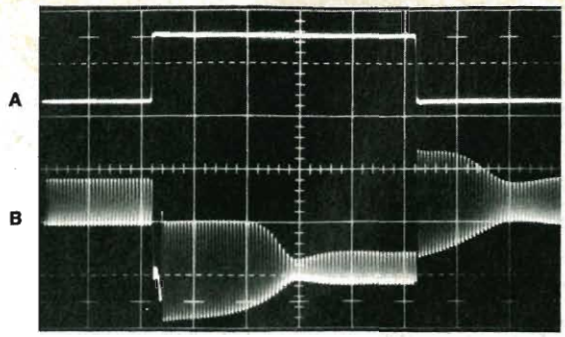


***Fig 7—Loop oscillation in a booster stage*** *produced this result. Note the lower frequency of oscillation compared with the local oscillation shown in* ***Fig 6****.*

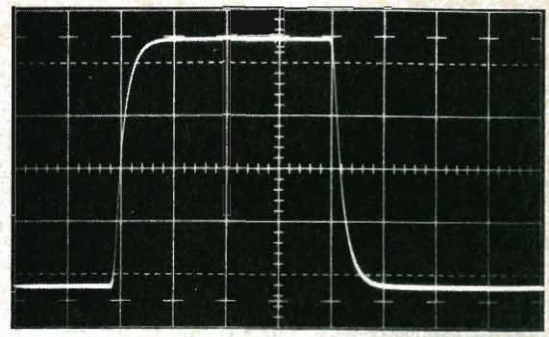


***Fig 8—Excessive source impedance*** *produced this serene—but undesired—result.*

stages are fast enough to maintain stability when placed in the amplifier's feedback loop.

The serene rise and fall of the **Fig 8** trace's pulse is a welcome relief from the oscillatory screaming of the previous examples. Unfortunately, such tranquilized behavior is simply too slow. This waveform is the result of excessive source impedance. The high impedance combines with the amplifier's input capacitance to band-limit the input, and the output reflects this action. Reduce the source impedance to a level that maintains the desired bandwidth, and minimize stray input capacitance. EDN

## Acronyms used in this article

**ac**—Alternating current
**DAC**—Digital-to-analog converter
**FET**—Field-effect transistor
**UHF**—Ultrahigh frequency

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## Author's biography

*For more information on this article's author, turn to page 163 in the October 10, 1991, issue.*

Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

## Measuring amplifier settling time

High-resolution measurement of an amplifier's settling time is often necessary. Frequently, a DAC drives the amplifier. Of particular importance is the time required for the DAC-amplifier combination to settle to its final value after an input step. This specification lets you set a circuit's timing margins with confidence that the data produced is accurate. The settling time is the total length of time from the input-step application until the amplifier's output remains within a specified error-band around the final value.

**Fig A** shows one way to measure DAC-amplifier settling time. The circuit uses the false-sum-node technique. The resistors and amplifier form a summing network. The amplifier output will step positive when the DAC moves. During amplifier slewing, the diodes limit the voltage excursion at the oscilloscope probe. The summing node is arranged so that, when settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half the actual settled voltage.

In theory, the **Fig A** circuit lets

*Text continued on pg 142*

you observe settling to small amplitudes. In practice, you can't rely on this circuit to produce useful measurements. Several flaws exist, including the oscilloscope connection. As probe capacitance rises, ac loading of the resistor junction will influence observed settling waveforms. The 20-pF probe alleviates this problem, but its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An active 1× FET probe might work, but another issue remains.

The clamp diodes at the probe point are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive-recovery characteristics vary among different types and are not usually specified. The 600-mV drop across the diodes means the oscilloscope may see an unacceptable overload, bringing displayed results into question. With the oscilloscope set at 1-mV per division, the diode voltage allows a 600:1 overdrive. Schottky diodes can cut this in half, but this is still much more than any real-time vertical amplifier can accommodate (**Ref 3**). The oscilloscope's

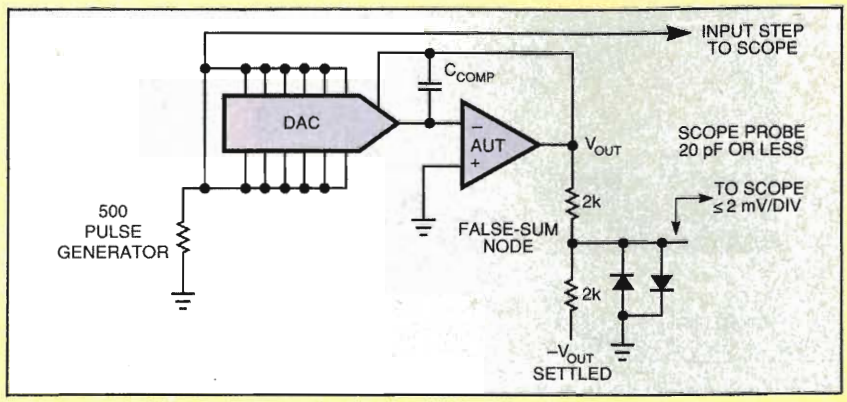



***Fig A—Using the false-sum-node technique**, this circuit has limitations in its ability to measure DAC-amplifier settling time.*

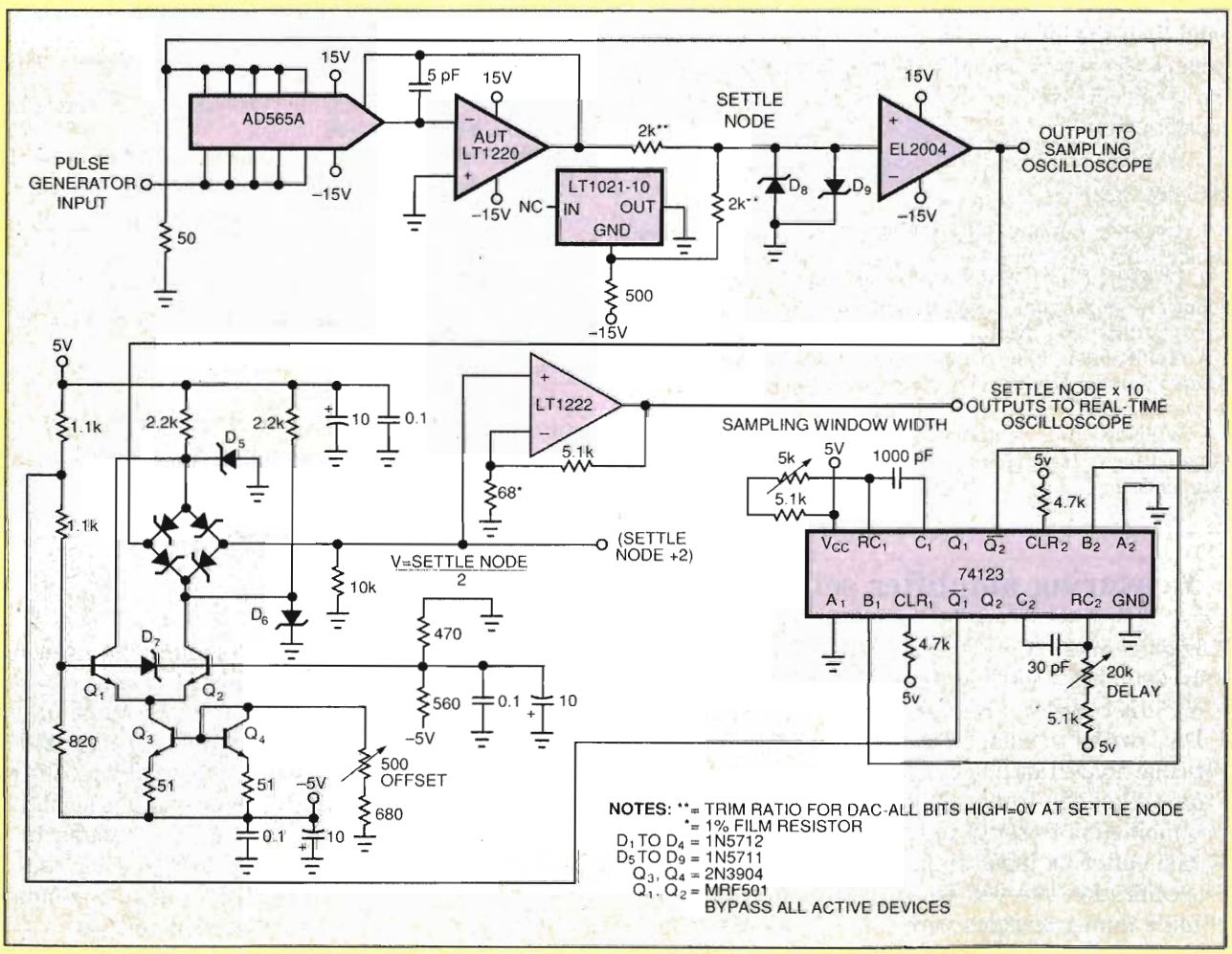



***Fig B—This settling-time test circuit** uses a sampling bridge to eliminate the oscilloscope overdrive problem of the previous circuit.*

overload recovery will completely dominate the observed waveform, and all measurements will be meaningless.

One way to achieve reliable settling-time measurements is to clip the incoming waveform in *time*, as well as amplitude. If you prevent the oscilloscope from seeing the waveform until settling is nearly complete, you can avoid overload problems. Doing this requires placing a switch at the settle circuit's output and controlling it with an input-triggered, variable delay. FET switches are not suitable because of their gate-source capacitance. This capacitance lets gate-drive artifacts corrupt the oscilloscope display, producing confusing readings. In the worst case, gate-drive transients will be large enough to induce overload, defeating the switch's purpose.

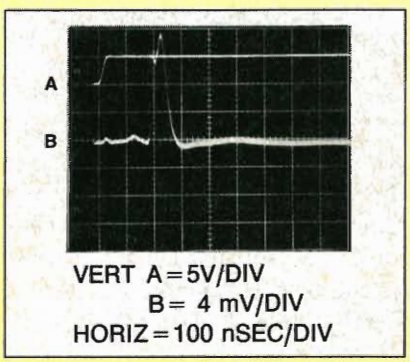



***Fig C—The 280-nsec settling time shown here** was measured using the **Fig B** circuit. The sampling switch closes just before the third vertical division, which lets you observe the settling detail without overdriving the oscilloscope.*

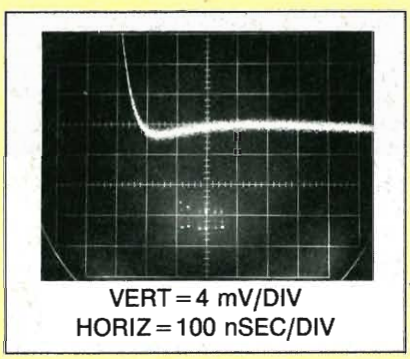



***Fig D—This 280-nsec settling-time measurement** was obtained using a sampling scope at **Fig B**'s sampling-scope output. The settling time and waveform is identical to that of **Fig C**.*

**Fig B** shows a way to implement a switch that largely eliminates these problems. This circuit lets you observe settling within 1 mV. The Schottky sampling bridge is the actual switch. The bridge's inherent balance, combined with matched diodes and very high-speed complementary bridge switching, yields a clean, switched output. An output-buffer stage unloads the settle node and drives the diode bridge.

The operation of the DAC-amplifier is as before. The additional circuitry provides the delayed switching function, eliminating oscilloscope overdrive. Buffering the settle node and driving the Schottky bridge is the EL2004, a unity-gain broadband FET-input buffer that has a 3-pF input capacitance and a 350-MHz bandwidth. The pulse generator's output fires the 74123 1-shot circuit. The arrangement of the 74123 produces a delayed pulse whose width sets the on-time of the diode bridge. The 20-kΩ potentiometer controls the pulse delay; the 5-kΩ potentiometer controls the pulse width. If you set the delay appropriately, the scope will not see any input until settling is nearly complete, eliminating overdrive. You adjust the width of the sample window so that all remaining settling activity is observable. In this way, the oscilloscope's output is reliable, and you can take meaningful data. $Q_1$ through $Q_4$ shift the level of the 1-shot's output, providing complementary switching drive to the bridge. The actual switching transistors, $Q_1$ and $Q_2$, are UHF types, permitting true differential bridge-switching with less than 1 nsec of time skew (**Ref 4**).

Using an oscilloscope having adequate sensitivity, you can observe the output of the bridge directly or you can look at the output of the LT1222, which provides a 10× amplified version. A third output, taken directly from the EL2004, is also available. This output, which bypasses the entire switching circuitry, provides a monitoring point for a sampling oscilloscope. Because of their operating nature, sampling oscilloscopes are inherently immune to overload (**Refs 5**, **6**, and **7**). A good test of this settling-time test fixture (and the above statement) is to compare the signals displayed by the sampling scope and the Schottky-bridge-aided real-time scope.

As an additional test, you can employ a completely different (albeit considerably more complex) method of measuring settling time, described by Barry Harvey (**Ref 8**). All three approaches represent good measurement techniques, and if you use proper construction, the results should be identical. That is, the data produced by the three methods has a high probability of being valid.

**Figs C**, **D**, and **E** illustrate settling time details of an AD565A DAC and an LT1220 op amp. The photos represent the sampling bridge, sampling scope, and "Harvey" methods, respectively. Photos **Figs C** and **E** display the input step for convenience in ascertaining the elapsed time. Photo **Fig D**, taken with a single-trace sampling oscilloscope (Tektronix 1S1 with a P6032 cathode-follower probe in a 556 mainframe), uses the left-most vertical graticule line as its zero-time reference. All methods agree on a 280-nsec settling time to 0.01% (1 mV on a 10V step). Note that Harvey's method inherently adds 30 nsec, which you must subtract from the displayed 310-nsec to get the real number. Note also that the shape of the settling waveform—in every detail—is

*Text continued on pg 144*

## Measuring amplifier settling time *(continued)*

identical in all three photographs. This kind of agreement provides a high degree of credibility for the measured results.

Some poorly designed amplifiers exhibit a substantial "thermal tail" after responding to an input step. This phenomenon, caused by die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking the settling at high speed, it is always a good idea to slow down the oscilloscope sweep and look for thermal tails. Often, you can accentuate the thermal tail's effect by loading the amplifier's output. Such a tail can make an amplifier appear to have settled in a much shorter time than it actually has.

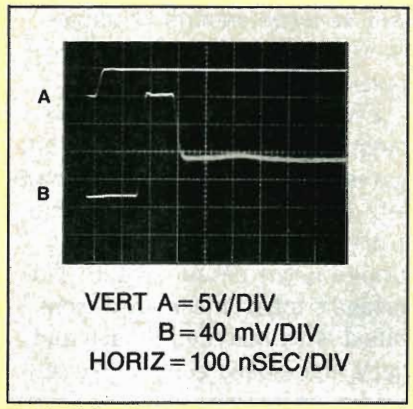



***Fig E—Harvey's method was used to obtain** this 280-nsec settling-time measurement. After subtracting this method's inherent 30-nsec delay, the settling time and waveform are identical to that of **Figs C** and **D**.*

### Select the feedback capacitor

To get the best possible settling time from any amplifier, you should choose the feedback capacitor, $C_F$, carefully. The purpose of $C_F$ is to roll off the amplifier gain at the frequency that permits the best dynamic response. The optimum value for $C_F$ will depend on the feedback resistor's value and the characteristics of the source. DACs are one of the most common sources and also one of the most difficult. Usually, you must convert a DAC's current output to a voltage. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200 nsec or less, but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the circuit unloads the DAC's current output directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase-shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling.

Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, which varies with code. Bipolar DACs typically have 20- to 30-pF of capacitance, which is stable over all codes. Because of their output capacitance, DACs furnish an instructive example in amplifier compensation.

**Fig Fa** shows the response of an industry-standard DAC-80 type and a relatively slow op amp. Trace A is the input, and traces B and C are the amplifier and settle outputs, respectively. In this example, there is no feedback capacitor ($C_F$), and the amplifier rings badly before settling. In **Fig Fb**, an 82-pF unit stops the ringing and settling time goes down to 4 μsec. The overdamped response means that $C_F$ dominates the capacitance at the AUT's input, assuring stability. For the fastest response, you must reduce the value of $C_F$. **Fig Fc** shows the critically damped behavior obtained with a 22-pF unit. The settling time of 2 μsec is the best obtainable for this DAC-amplifier combination. Higher speed is possible with faster amplifiers and DACs, but the compensation issues remain the same.

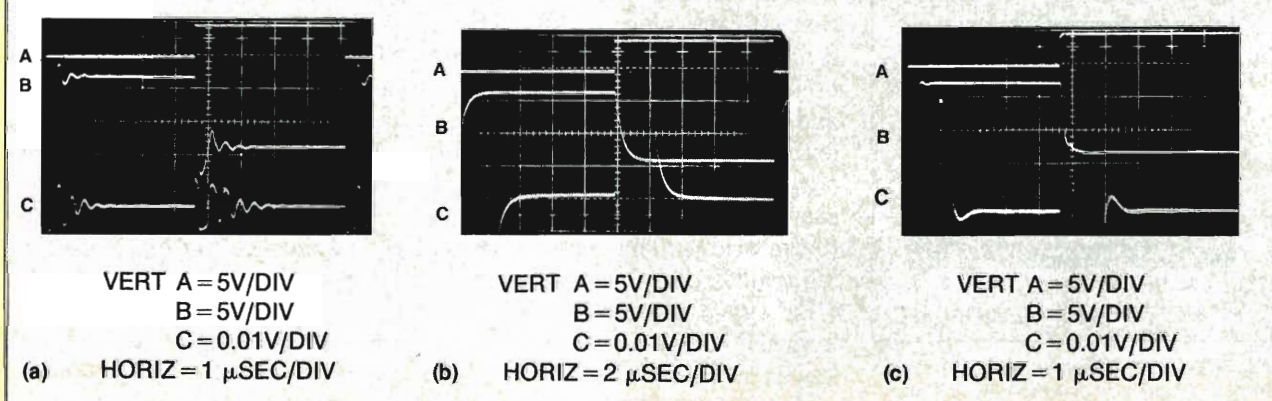



***Fig F—These three scope traces show the effects of different values of feedback capacitors** on DAC-amplifier combinations. The values for the three photos are no capacitance (**a**), 82 pF (**b**), and 22 pF (**c**).*

THE JIM WILLIAMS PAPERS

# Filters and oscillators

Filters get rid of a signal's unwanted frequency components. Oscillators create signals at predictable frequencies. As you might imagine, the two types of circuits have more than a little in common.

Jim Williams, *Linear Technology Corp*

Filters and oscillators share a common point of view—they deal with signals in the frequency domain. You can define a filter's function as rejecting frequencies you don't want (the job of a band-reject filter, for example) or including only the frequencies you want (what a bandpass filter does). If you reorient your thinking slightly, though, you realize that all filters reject unwanted frequencies. (The bandpass filter rejects frequencies outside the band of interest.) When you view filters in this way, you see that any filter's function is the inverse of an oscillator's; oscillators synthesize individual frequencies or ranges of frequencies. Although there are more kinds of filters and oscillators than any magazine article of reasonable length can hope to touch on, herein are a few types of circuits that can meet a range of needs.

**Fig 1a** shows a highly selective bandpass filter using a resonant ceramic element and a single amplifier. Except at its resonant frequency, (in this case, 400 kHz) the ceramic element looks like a high impedance. For off-resonance inputs, $IC_1$ produces no output; it acts as a follower whose input is grounded. At resonance,

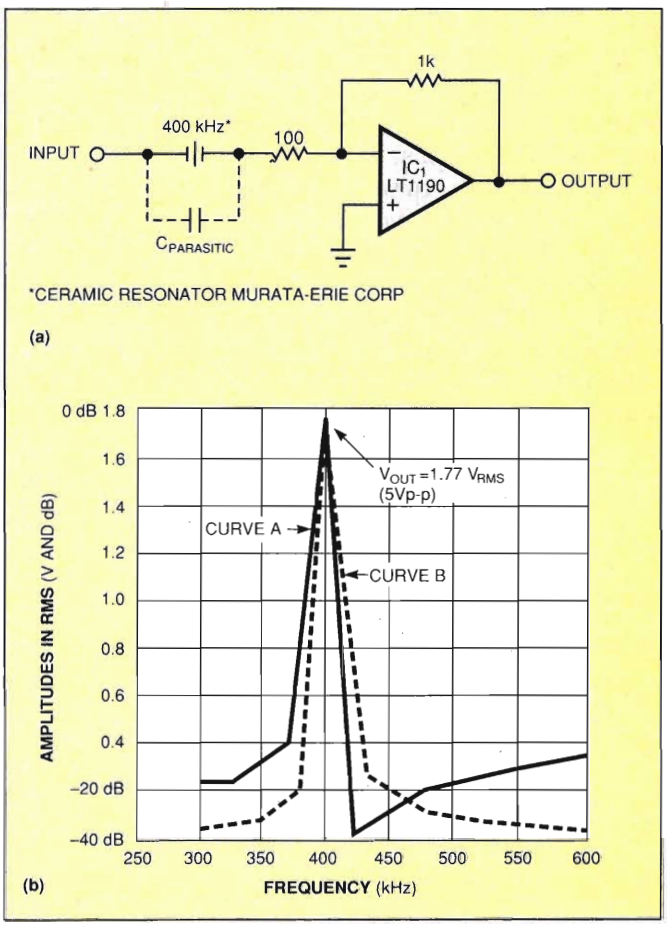



***Fig 1—One amplifier and a ceramic resonator*** *create a bandpass filter* ***(a)****. The solid curve of* ***b*** *shows the filter's frequency response. Note the dip to −40 dB on the high side of resonance. The dip is the result of the resonator's parasitic capacitance.*

the ceramic element has a low impedance, and $IC_1$ behaves as an inverter with gain. The 100Ω resistor isolates $IC_1$'s summing point from the ceramic element's capacitance. This capacitance is quite substantial and limits the circuit's out-of-band rejection. **Fig 1b**, curve A shows this effect. This plot shows very steep rejection, with $IC_1$'s output down almost 20 dB at 300 kHz and 40 dB at 425 kHz. The device's stray parasitic capacitance causes the gentle rise in the output at higher frequencies and also sets the −20-dB floor at 300 kHz.

**Fig 2** shows how to use a nulling technique to partially correct problems caused by the ceramic element's parasitic capacitance. This circuit is similar to the previous one, except that a portion of the input goes to $IC_1$'s positive input. The R-C network at that input has an impedance close to the ceramic resonator's off-null impedance. Therefore, out-of-band components produce similar signals at $IC_1$'s inputs, and, because of $IC_1$'s common-mode rejection, produce little output. At resonance, the added R-C network appears as a much higher impedance than does the ceramic element, and the filter response is similar to that of the circuit in **Fig 1a**. **Fig 1b**, curve B shows that this circuit has much better out-of-band rejection than does the earlier circuit. The high-frequency rolloff is smooth, and, at 475 kHz, over 20 dB deeper than that of the circuit in **Fig 1a**. At 375 kHz and below, on the low-frequency side of resonance, the circuits behave similarly.

By using quartz crystals, you can make filters whose high-frequency selectivity is even higher than that of filters based on ceramic resonators. **Fig 3a** replaces **Fig 1a**'s ceramic element with a 3.57-MHz quartz crystal. **Fig 3b** shows almost 30 dB of attenuation only a few kHz on either side of resonance! The differential nulling technique used with the ceramic elements is less effective with quartz crystals. Crystals have significantly lower parasitic capacitance, making the cancellation less effective.

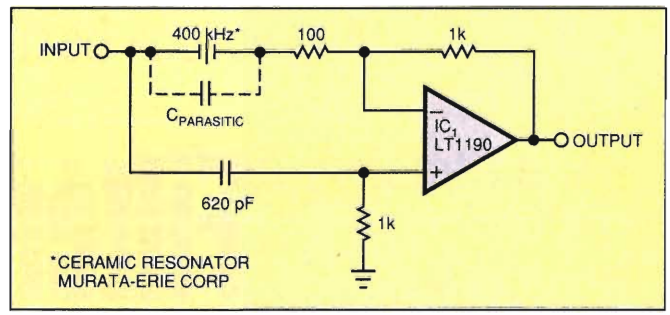



***Fig 2—A slight modification** of the circuit in **Fig 1a** allows you to cancel out the effects of the resonator's parasitic capacitance. The dashed curve of **Fig 1b** shows the effects on the filter response. Below resonance, the modified circuit attenuates by an extra 20 dB. Above approximately 525 kHz, the improvement is even more dramatic.*

## Oscillators use crystals and resonators

The circuit in **Fig 4** places a crystal within the amplifier's feedback path, creating an oscillator. With the crystal removed, the circuit is a familiar noninverting amplifier with a grounded input. The impedance ratio of the elements associated with $IC_1$'s negative input sets the gain. Inserting the crystal closes a positive

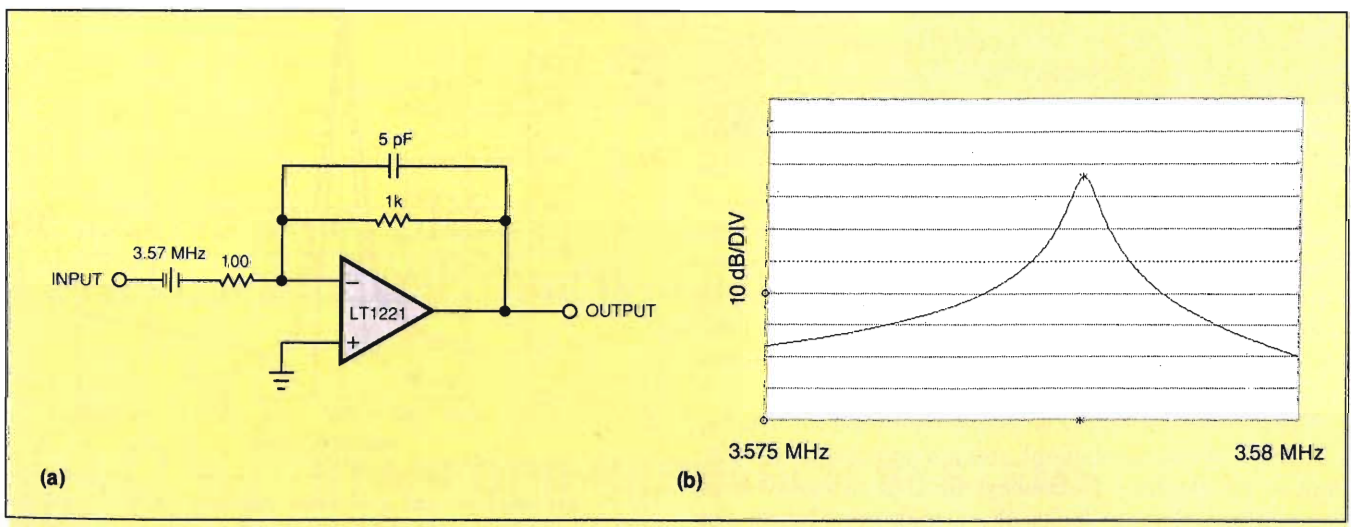



***Fig 3—Replacing the ceramic resonator** of **Fig 1a** with a 3.57-MHz crystal is the most significant change that leads to this crystal filter (**a**). You can see the crystal filter's response in **b**.*

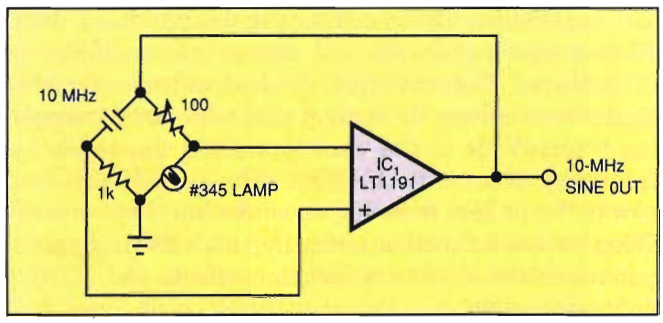



***Fig 4—An incandescent lamp's** current-dependent resistance stabilizes the oscillation amplitude of this 10-MHz crystal oscillator.*

feedback path at the crystal's resonant frequency, and oscillations commence.

In any oscillator, you must control the gain as well as the phase shift at the frequency of interest. If the gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting. In this circuit, gain control comes from the positive temperature coefficient of the lamp at $IC_1$'s negative input. When you first apply power, the lamp's resistance is low, the gain is high, and the oscillation amplitude increases. As the amplitude builds, the lamp current increases and causes heating, which raises the lamp resistance. The increased resistance reduces the amplifier gain and the circuit finds a stable operating point. This circuit's sine-wave output has all of the stability advantages associated with quartz crystals. Although shown with a 10-MHz crystal, the circuit works well with a variety of crystal types from 100 kHz to 20 MHz. Using a lamp to control the amplifier gain is a classic technique, first described by Meacham in 1938. Electronic gain control, though more complex, offers more precise control of amplitude.

**Fig 5a**'s quartz stabilized oscillator replaces the lamp with an electronic amplitude-stabilization loop. $IC_2$ compares the $IC_1$ oscillator's positive output peaks with a dc reference. The diode in the dc-reference path compensates for the rectifier diode's temperature dependence. $IC_2$ biases $Q_1$, controlling the FET's channel resistance and influencing the loop gain. The amplitude of the oscillator's output is a reflection of the loop gain. Loop closure around $IC_1$ stabilizes the amplitude of the oscillator's output; the 1-μF capacitor compensates the gain-control loop.

The dc-reference network provides optimum temperature compensation for the rectifier diode, which sees $IC_1$'s 2V p-p, 20-MHz output waveform. $IC_1$'s small output swing minimizes the distortion attributable to channel-resistance modulation in $Q_1$. To use this circuit, adjust the 50Ω trimmer until 2V p-p oscillations appear at $IC_1$'s output.

**Fig 5b** is a spectrum analysis of the oscillator's output. The fundamental is at 20 MHz; the second harmonic, at 40 MHz, is 47 dB down. The third harmonic,

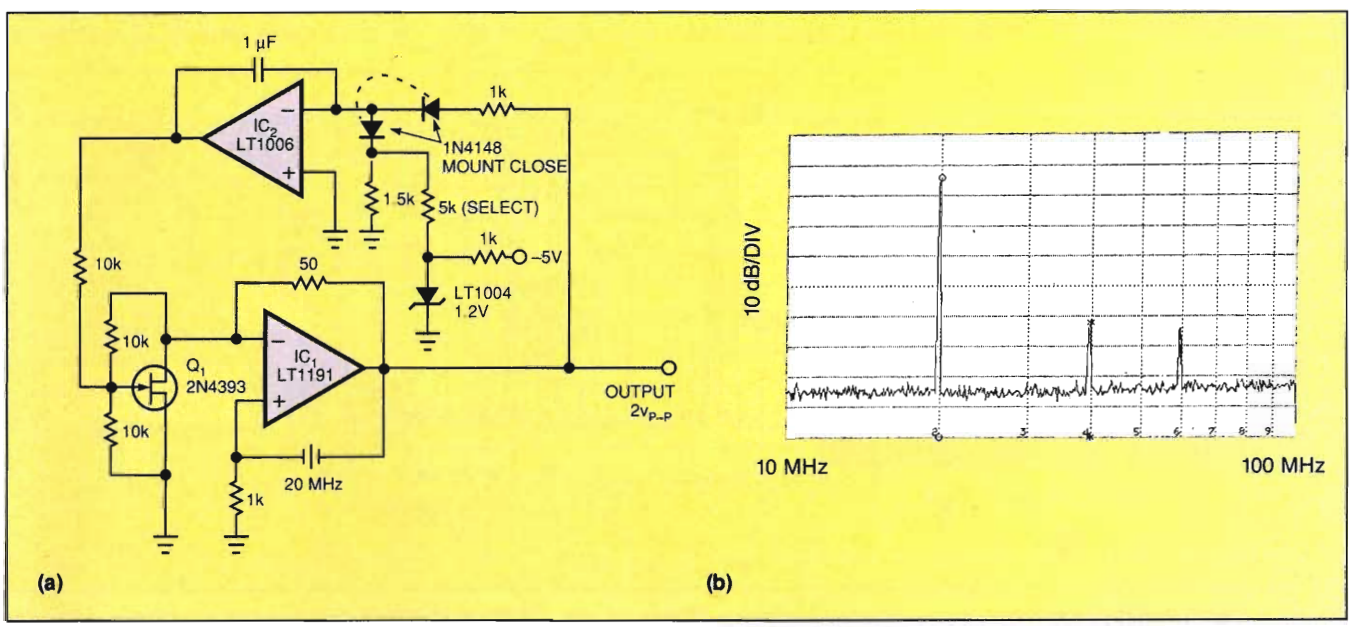



***Fig 5—An electronic gain-control circuit** that uses the voltage-controlled on-resistance of a FET stabilizes the output amplitude of this 20-MHz crystal oscillator (**a**). In **b**, you see that the output's harmonics are at least 47 dB below the fundamental.*

50 dB down, occurs at 60 MHz. Resolution bandwidth for the spectrum analysis is 1 kHz.

The circuit in **Fig 6a** replaces the quartz crystal with a Wien network at $IC_2$'s positive input. $IC_1$ controls $Q_1$ to stabilize the amplitude of $IC_2$'s oscillations. The operation is identical to that of the circuit in the previous figure. Although the Wien network is not nearly as stable as a quartz crystal, it has the advantage of a variable-frequency output. Normally, you vary the frequency by varying either R or C or both. The use of manually adjustable elements, such as dual potentiometers and 2-section variable capacitors is common. The circuit in **Fig 6a** uses fixed, 360Ω Wien-network resistors and uses varactor diodes as capacitors. The varactor diodes' voltage-variable capacitance allows dc tuning of the oscillator. Applying 0 to 10V dc to the varactors shifts the oscillation frequency from 1 to 10 MHz. The 0.1-μF capacitor blocks the dc bias from $IC_2$'s positive input but lets the Wien network function normally. $IC_2$'s 2V p-p output minimizes the varactors' junction effects and thereby limits distortion.

This 5V-powered circuit requires a voltage step-up to develop adequate varactor drive. $IC_3$ and the

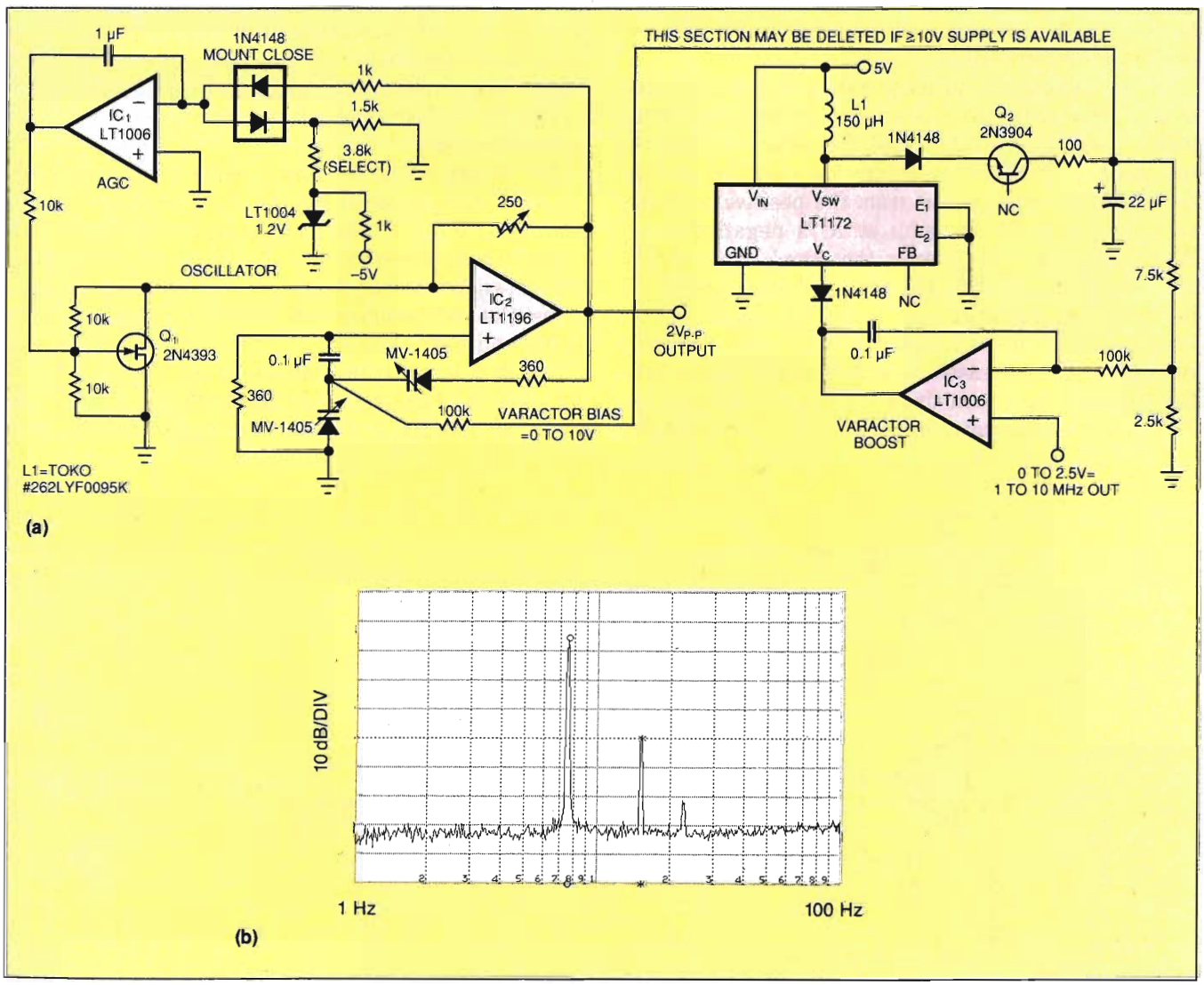



***Fig 6—A pair of varactor diodes*** *lets you tune this Wien-bridge oscillator* ***(a)*** *from 1 MHz to 10 MHz by applying a 0 to 10V signal. Adding the components in the right half of the schematic lets you operate the circuit from a 5V supply and permits controlling the frequency with a 0 to 2.5V signal. The spectrum analysis in* ***b*** *shows that the sinusoidal output is quite clean.*

LT1172 switching regulator form a simple voltage step-up regulator. $IC_3$ controls the LT1172 to produce whatever output voltage is required to close a loop at $IC_3$'s negative input. The 22-μF output capacitor stores $L_1$'s high-voltage inductive-flyback pulses after they have been rectified by the diode-and-zener-connected $Q_2$. The 7.5-kΩ/2.5-kΩ divider closes the loop by providing a sample of the output value to $IC_3$'s negative input. The 0.1-μF capacitor stabilizes this feedback action. $IC_2$'s zener drop allows the circuit to produce controlled outputs at voltages as small as zero. This arrangement permits a 0 to 2.5V input at $IC_3$ to produce a corresponding 0 to 10V varactor bias. **Fig 6b**, a spectral plot of the circuit running at 7.6 MHz, shows the second harmonic down 35 dB and the third harmonic down almost 60 dB. The resolution bandwidth is 3 kHz.

**Fig 7a** shows the schematic of an AM radio station—complete from microphone to antenna, but lacking a Federal Communications Commission license. $IC_1$, set up as a quartz-stabilized oscillator similar to the one in **Fig 4**, generates the carrier. $IC_1$'s output feeds $IC_2$, which functions as a modulated RF power-output stage. The bias applied to offset pins 1 and 8 restricts $IC_2$'s input-signal range. (See the LT1194 data sheet for details.) $IC_3$, a microphone amplifier, supplies bias to the offset pins, resulting in an amplitude-modulated RF carrier at $IC_2$'s output. The dc voltage summed with the microphone output biases $IC_3$'s output to the appropriate level for good quality modulation characteristics. Calibrating this circuit involves trimming the 100Ω potentiometer in the oscillator for a stable 1V p-p 1-MHz output from $IC_1$.

**Fig 7a** does not show on-air personalities—or, in keeping with current trends in AM radio—a means of providing any kind of program other than a talk show. There is no phonograph pickup or connection to the output of a compact-disc player. Nevertheless, you can connect such a music source to the microphone input. **Fig 7b** shows a typical AM carrier output at the antenna. In a throw-back to the days when top-40 formats reigned on the AM band, the modulating signal is Mr Chuck Berry singing the rock-'n'-roll classic "Johnny B. Goode."

### Start with a triangle; end up with a sine

The oscillators presented to this point have limited tuning-frequency range. Although the circuit in **Fig 8a** is not a true oscillator, it produces a synthesized sine-wave output over a wide dynamic range. Many applications such as audio, shaker-table driving, and automatic test equipment require voltage-controlled oscillators (VCOs) that have sine-wave outputs. This circuit meets this need, spanning a range of 1 Hz to 1 MHz (equal to 6 decades or 120 dB) for a 0 to 10V input. The circuit maintains 0.25% frequency linearity and 0.40% distortion.

To understand the circuit, assume $Q_5$ is on and its collector (**Fig 8b**, trace A,) is at −15V, cutting off $Q_1$. $IC_3$, which inverts the positive input voltage and biases the summing node of integrator $IC_1$ through the 3.6-kΩ

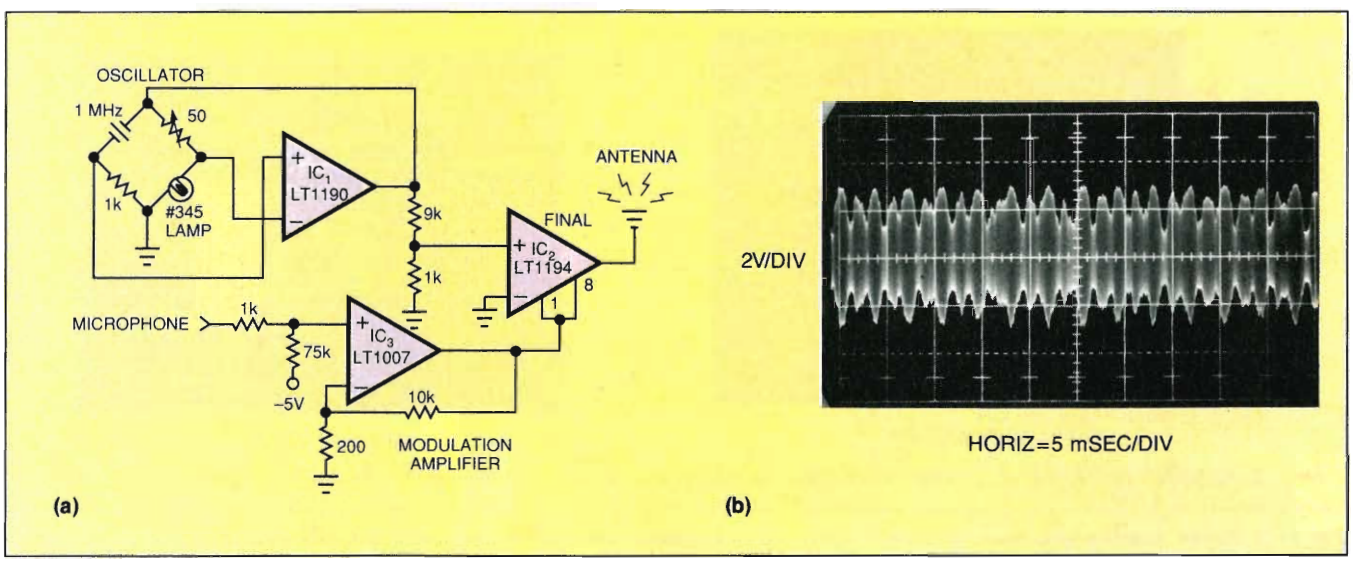



***Fig 7—Though perhaps not worthy of Wolfman Jack** or Dick Biondi, the circuit of **a** is still a complete AM radio station. When Chuck Berry picks his guitar and belts out "Johnny B. Goode," the modulated output looks like what you see in **b**.*

resistor and the self-biased FET's, pulls a current, $-I$, from the summing point. $IC_2$, a precision op amp, provides dc stabilization of $IC_1$. $IC_1$'s output, (trace B,) ramps positive until $IC_5$'s input, (trace C,) crosses zero and causes $IC_5$'s inverting output to go negative. The $Q_4/Q_5$ level shifter then turns off, and $Q_5$'s collector goes to $+15V$, allowing $Q_1$ to come on. The values of the resistors in $Q_1$'s path result in a current, $+2I$, exactly twice the absolute magnitude of the current, $-I$, that flows out of the summing node. As a result, the net current into the junction becomes $+I$, and $IC_1$ integrates negatively at the same rate it did during its positive-going excursion.

When $IC_1$ integrates far enough in the negative di-

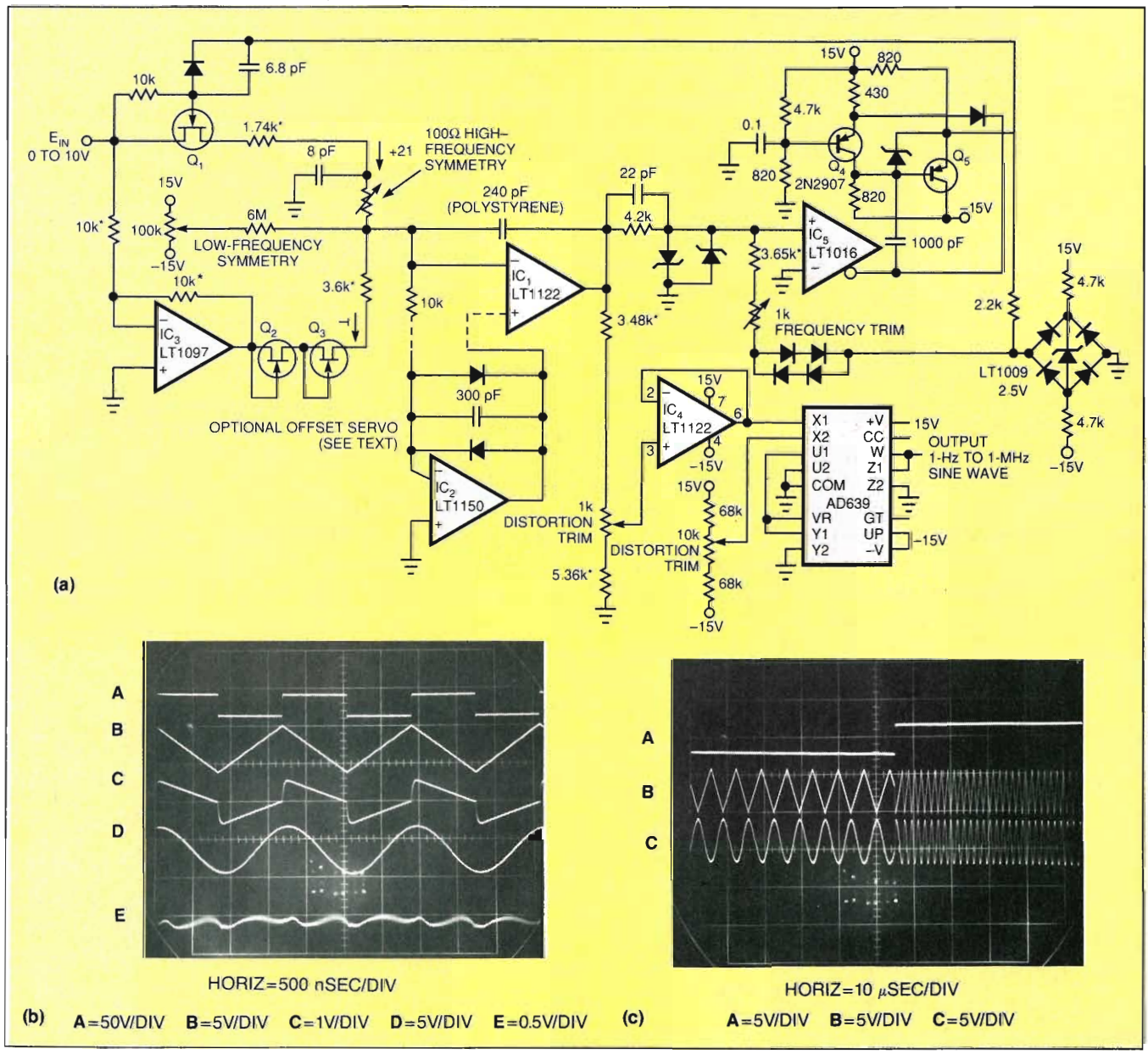



***Fig 8—A classic function generator, a,*** *creates square and triangular waves whose frequency you can control with a dc voltage. A trigonometric-function generator IC converts the triangle to a sine. The traces in* ***b*** *show waveforms within the circuit. The lowest trace shows the residual distortion after you remove the output's fundamental-frequency component. In* ***c,*** *you see the circuit's quick and clean response to a command to change frequency.*

rection, $IC_5$'s + input crosses zero and the circuit's two outputs change state. The state change switches the $Q_4/Q_5$ level shifter's state, causing $Q_1$ to go off and the entire cycle to repeat. The result is a triangular waveform at $IC_1$'s output. The frequency of this triangle depends on the circuit's input voltage and varies from 1 Hz to 1 MHz with a 0 to 10V input. The LT1009 diode bridge and the series-parallel diodes provide a stable bipolar reference that always opposes the sign of $IC_1$'s output ramp. The Schottky diodes bound $IC_5$'s + input, ensuring its clean recovery from overdrive.

### Sine of the times

The AD639 trigonometric function generator, biased via $IC_4$, converts $IC_1$'s triangular output into a sine wave, (trace D). To avoid output distortion, you must supply the AD639 with a triangular wave that does not vary in amplitude. At higher frequencies, delays in the $IC_1$-integrator switching loop result in late turn-on and turn-off of $Q_1$. Unless you minimize these delays, the triangle amplitude will increase with frequency and cause the distortion level to increase. $IC_5$, the $Q_4/Q_5$ level shifter, and $Q_1$ generate a total delay of 14 nsec. This small delay, combined with the 22-pF feedforward network at $IC_5$'s input, keeps distortion to just 0.40% over the entire 1-MHz range. At 100 kHz, the distortion is typically less than 0.2%. The 8-pF capacitor in $Q_1$'s source line minimizes the effects of gate-source charge transfer, which occurs whenever $Q_1$ switches. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. FETs $Q_2$ and $Q_3$ compensate for the temperature-dependent on-resistance of $Q_1$ and keep the $+2I/-I$ relationship constant with temperature.

This circuit responds very rapidly to input changes—something most sine-wave generators cannot do. **Fig 8c** shows what happens when the input switches between two levels, (trace A). $IC_1$'s triangle output (trace B), shifts frequency immediately, with no glitches or poor dynamics. The sine output, (trace C), reflecting this action, is similarly clean. To adjust this circuit, apply 10.00V and trim the 100Ω potentiometer for a symmetrical triangle output at $IC_1$. Next, apply 100 μV and trim the 100-kΩ potentiometer for triangle symmetry. Then, apply 10.00V again and trim the 1-kΩ frequency-trim adjustment for a 1-MHz output frequency. Finally, adjust the distortion-trim potentiometers for minimum distortion as measured on a distortion analyzer (**Fig 8b**, trace E). You may have to readjust the other potentiometers slightly to achieve the lowest possible distortion. If you won't operate the circuit below 100 Hz, you can delete the $IC_2$-based dc-stabilization stage. If you make this change, you should ground $IC_1$'s positive input.

Many of the filter and oscillator circuits presented here are simple as well as useful. Their simplicity shows that clever circuit designers often take a minimalist approach. When you speak or write, you are more likely to get your point across if you use short words that are familiar to your audience. So it is with circuits. The simplest design that does the job usually costs the least and operates more reliably than complex alternatives. EDN

## Author's biography

*For more information on this article's author, turn to pg 163 in the October 10, 1991, issue.*

THE
JIM WILLIAMS
PAPERS

# High-speed communications circuits

High-frequency communications signals need wideband analog circuits. High-speed monolithic amplifiers let you build simple, effective circuits to meet this need for both optical and RF transmission.

Jim Williams, *Linear Technology Corp*

Megahertz-range data transmission and communications requires wideband linear circuitry. By designing around a monolithic high-speed amplifier, you can easily implement a variety of standard high-performance communications circuits. The following circuits detail several such designs for both optical and RF transmission. All have been carefully worked out and can serve as good idea sources.

Amplifying fast photodiode signals over a wide range of optical intensity is one common optical-communications requirement. **Fig 1a**'s fast FET amplifier gives wideband operation for 5 decades of photocurrent. You set up the photodiode in the conventional manner and use a −15V bias to aid diode response. Photocurrent feeds directly to $IC_1$'s summing point, which causes $IC_1$'s output signal to move to whatever level is required to maintain virtual ground at the negative input pin. **Fig 1b** details the circuit's operating characteristics when using the HP5082-4204 photodiode.

You must use care when frequency-compensating this circuit. The diode has approximately 2 pF of parasitic capacitance, which creates a significant lag at $IC_1$'s summing point. Without a feedback capacitor, the circuit's high-speed dynamics are poor. **Fig 1c** illustrates this point by showing the circuit's response to a photocurrent input pulse (trace A) when the 3-pF feedback capacitor is removed. $IC_1$'s output voltage (trace B) overshoots and saturates before finally ringing down to its final value. Replacing the feedback capacitor gives **Fig 1d**'s results. The same input pulse (trace A) produces a cleanly damped output voltage (trace B). The capacitor, however, imposes a 50% speed penalty (note that the horizontal scale of **Fig 1d** is faster than that of **Fig 1c**). This penalty is unavoidable because suppressing the parasitic ringing's relatively low frequency mandates significant roll-off.

### Basic amplifier has many uses

You can use the basic photodiode amplifier as the foundation for a variety of measurement and communications circuits. One such measurement circuit is **Fig 2a**'s photointegrator. The output voltage represents the integral of the diode's photocurrent over a time period defined by the control line. This circuit is par-

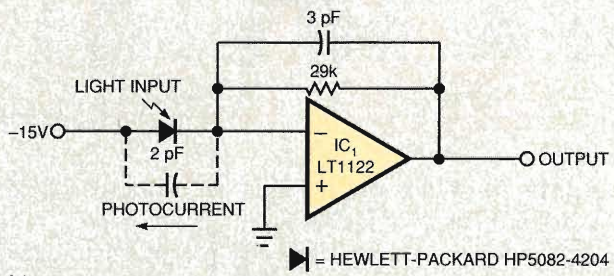
ticularly useful for measuring the total energy in a light pulse or pulses. The circuit is a fast integrator and uses $IC_{2A}$ as a reset switch. $IC_{2B}$, which the control input signal switches simultaneously with $IC_{2A}$, compensates for $IC_{2A}$'s charge-injection error.

When the control input line is low (**Fig 2b,** trace A) and no photocurrent is present, $IC_{2A}$ is closed and $IC_1$ acts as a grounded follower. Under these conditions, $IC_1$'s output signal (trace C) sits at 0V. When the control input line goes high, $IC_1$ becomes an integrator as soon as $IC_{2A}$ opens. Due to the switch delay, $IC_2$ opens approximately 150 nsec after the control input line goes high.

When $IC_{2A}$ opens, it delivers some parasitic charge to $IC_1$'s summing point. $IC_{2B}$ provides a compensatory charge-based pulse at $IC_1$'s positive terminal to cancel the effects of $IC_{2A}$'s charge error. The combined effect of the two charge pulses shows up as a fast, small amplitude event in $IC_1$'s output, which settles rapidly back to 0V. You can see this event on trace C near the 400-nsec mark.

Once the switches have opened, the integrator is ready to receive and record a light pulse. When a light pulse (trace B) falls on the photodiode, $IC_1$ responds by integrating (trace C). With the circuit as shown in **Fig 2a,** $IC_1$ integrates rapidly until the light pulse ceases. $IC_1$'s voltage after the light event is over is related to the total energy the photodiode sees during the event. In typical operation, the control line then returns low, which resets $IC_1$ for the next light event.

When the circuit has only 10 pF of integration capacitance, its output droop rate is about 0.2V/μsec. You

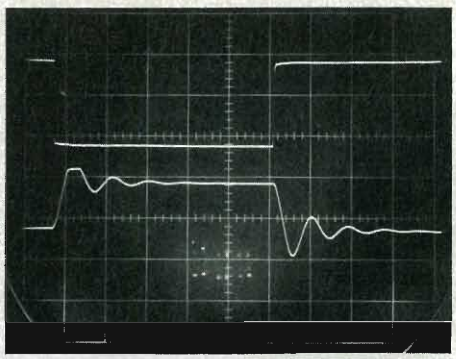



(a)

**RESPONSE DATA**

| LIGHT (900 nm) | DIODE CURRENT | CIRCUIT OUTPUT |
|---|---|---|
| 1 mW | 350 μA | 10.0V |
| 100 μW | 35 μA | 1V |
| 10 μW | 3.5 μA | 0.1V |
| 1 μW | 350 nA | 0.01V |
| 100 nW | 35 nA | 0.001V |

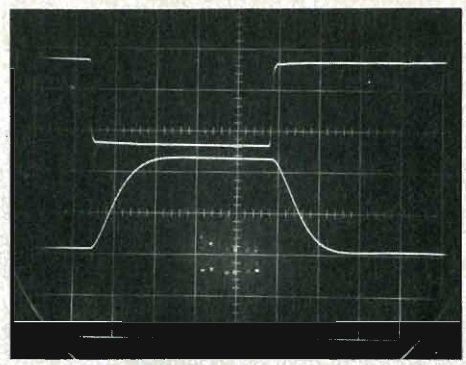
(b)




HORIZONTAL SCALE=500 nSEC/DIV

| TRACE | VERTICAL SCALE |
|---|---|
| A | 175 μA/DIV |
| B | 10V/DIV |

(c)




HORIZONTAL SCALE=200 nSEC/DIV

| TRACE | VERTICAL SCALE |
|---|---|
| A | 175 μA/DIV |
| B | 5V/DIV |

(d)

***Fig 1—This basic photodiode amplifier circuit (a)*** *handles 5 decades of light intensity. The table* ***(b)*** *details the circuit's operating characteristics with the HP5082-4204 diode. Parts* ***c*** *and* ***d*** *show the circuit's response (trace B) to an input signal (trace A) without and with compensation, respectively.*

can increase the capacitance, but the integration speed will suffer accordingly. As shown, the circuit accommodates integration times of nanoseconds to milliseconds and photocurrents ranging from nanoamperes to hundreds of microamperes. Thus, light pulses with optical-power intensities spanning microwatts to milliwatts over wide ranges of duration are practical input signals.

The primary factors restricting the circuit's accuracy are $IC_1$'s 75-pA bias current and 12V output swing and the effectiveness of the charge-cancellation network. Typically, the circuit can achieve full-scale accuracy within several percent if you trim the charge-cancellation network. To trim the network, make sure that no light falls on the diode while you repetitively pulse the control line. Adjust the trimmer capacitor to achieve a 0V output at $IC_1$ immediately after the disturbance associated with the $IC_{2A}$-$IC_{2B}$ switching settles.

A communications circuit that relies on the basic photodiode amplifier is the simple fiber-optic receiver in **Fig 3a.** $IC_1$, a photocurrent-to-voltage converter similar to **Fig 1a,** feeds comparator $IC_2$. $IC_2$ compares $IC_1$'s output voltage to a dc level established by the

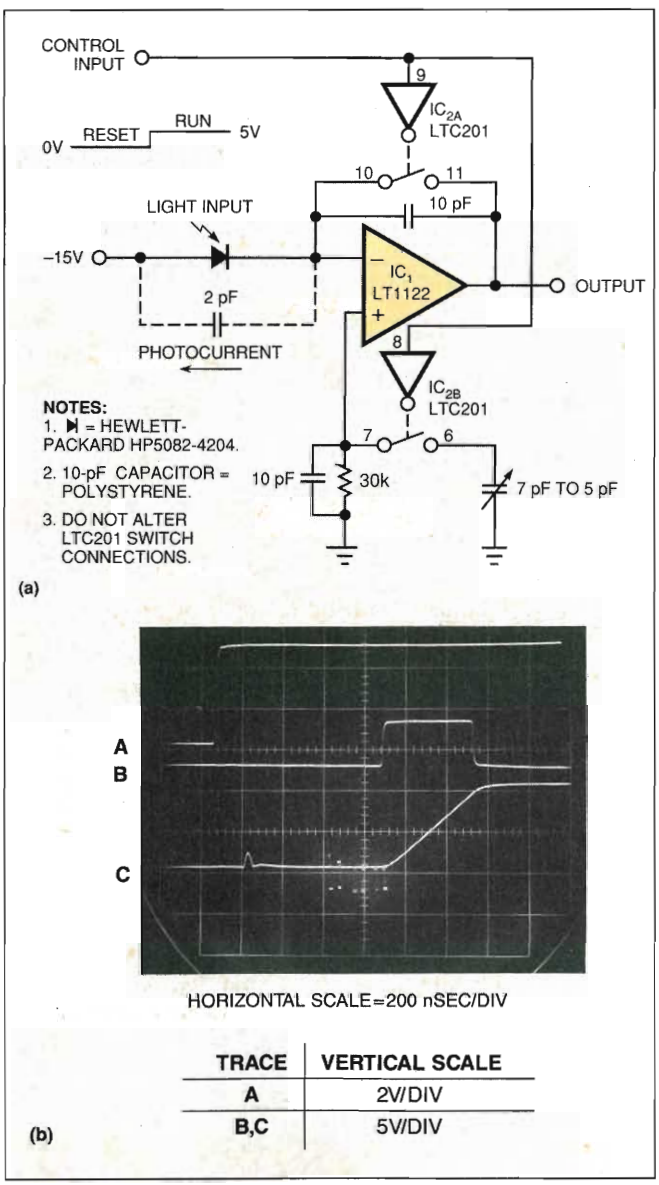



***Fig 2—The basic photodiode amplifier is the basis for this integrator,*** *which has a resettable output* ***(a).*** *When the control line is high* ***(b,*** *trace A), the circuit integrates (trace C) the incoming signal (trace B).*

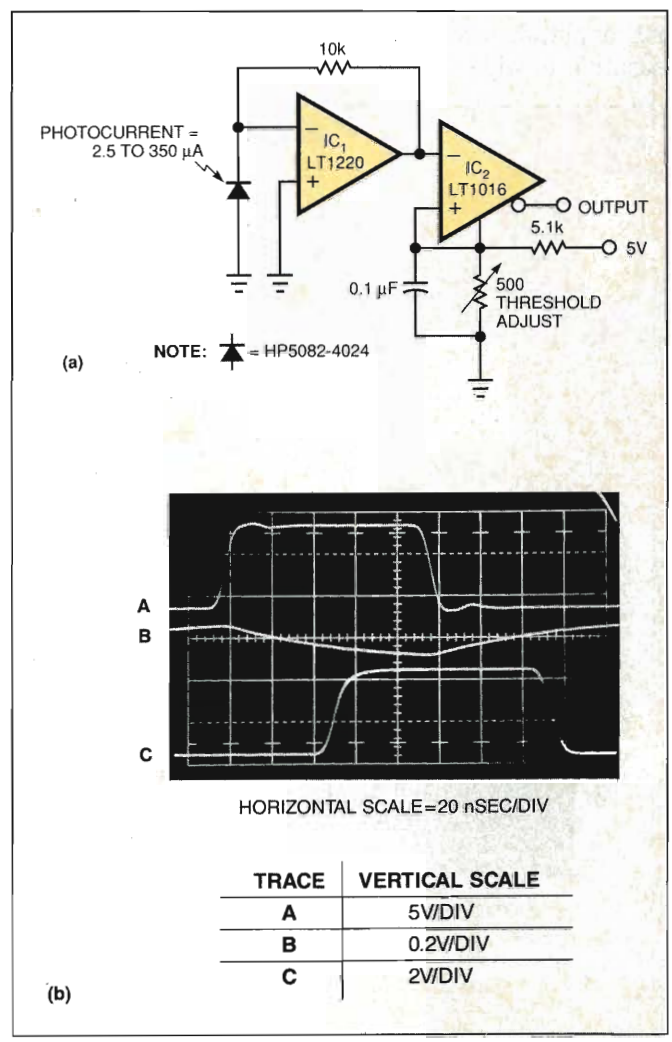



***Fig 3—This simple optical receiver (a)*** *has a fixed signal threshold. The outputs of $IC_1$ (**b,** trace B) and $IC_2$ (trace C) lag the input signal (trace A).*

threshold-adjust potentiometer, thus producing a logic-compatible output signal. **Fig 3b** shows this circuit's typical waveforms. Trace A is a pulse associated with a light input signal. Trace B is $IC_1$'s response, and trace C is $IC_2$'s output signal. The phase shift between the photocurrent input signal and $IC_2$'s output signal is due to $IC_1$'s delay in reaching the threshold level. Reducing the threshold level will help reduce the shift but moves the circuit's operation closer to the noise floor. Additionally, the fixed threshold level cannot account for response changes in the emitter and detector diodes and the fiber-optic line over time and temperature. These response changes manifest as changes in the apparent amplitude of the signal.

Receiving high-speed fiber-optic data with such input amplitude variations is not easy, especially if the variation is wide. Unless the receiver is carefully designed, the high-speed data and uncertain intensity of the light level can cause erroneous results. **Fig 4a** addresses the previous circuit's fixed-threshold limitation and offers significant performance advantages. This receiver reliably conditions fiber-optic input signals as fast as 40 MHz. The peak-to-peak amplitude of input signal can vary by as much as 40 dB. The circuit's digital output stage has an adaptive threshold trigger that accommodates signal intensity variations due to component aging and other causes. The circuit has an analog output signal that you can use to monitor the detector's output.

The PIN photodiode detects the optical signal, which $IC_1$ then amplifies. A second stage, $IC_2$, further amplifies the signal. The output voltage of this second stage biases a 2-way peak detector ($Q_1$ through $Q_4$). $Q_2$'s emitter capacitor stores the signal's maximum peak while

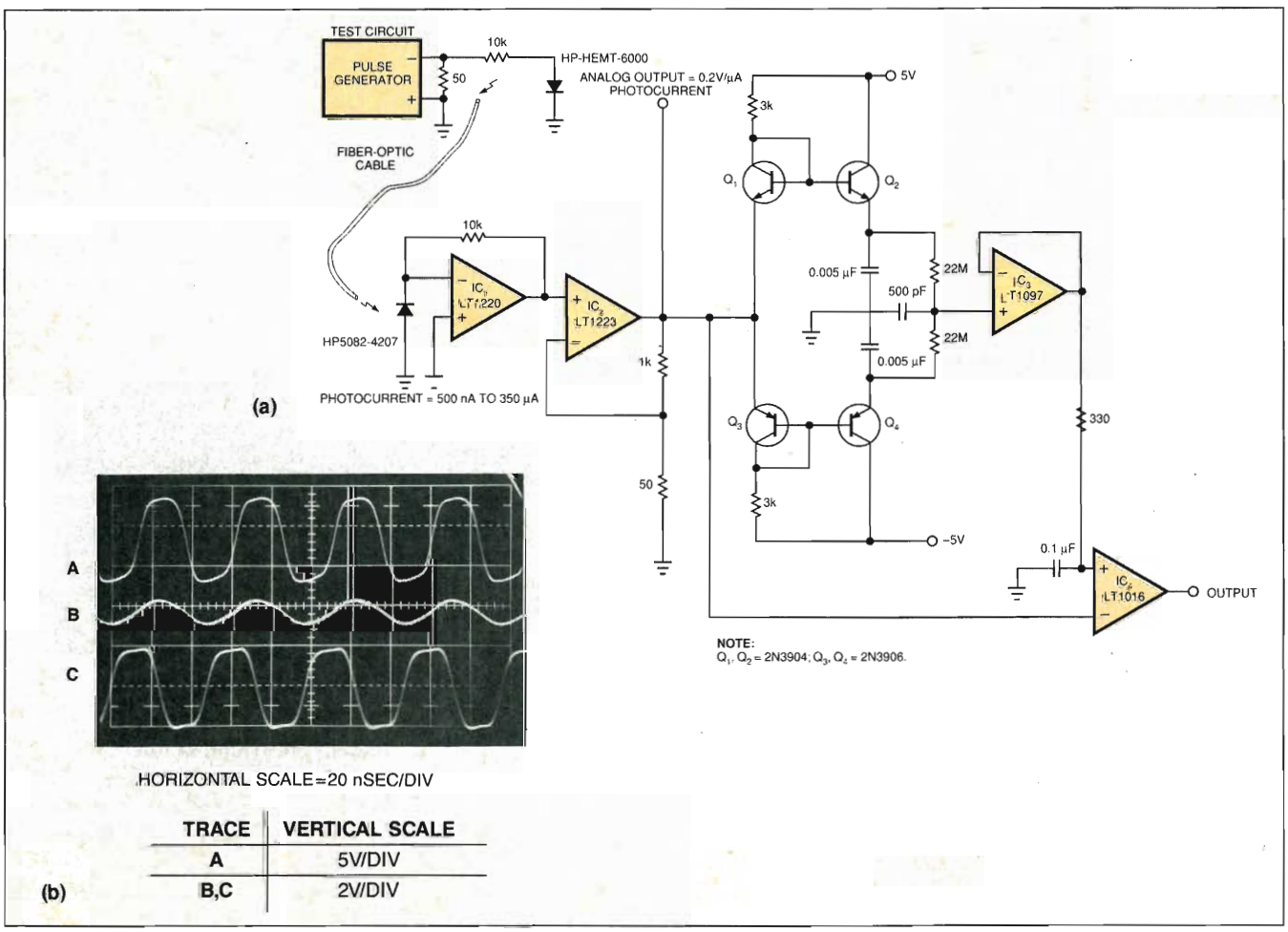



***Fig 4—A self-adapting threshold*** *is the hallmark of this optical receiver* ***(a)****. Driven by a test signal* ***(b****, trace A), the circuit lets you monitor the detector's current (trace B) in addition to producing a final output (trace C).*

# Protective circuit can save you a load

Some type of fuse or circuit breaker helps protect integrated circuits during developmental probing and expensive loads during trimming and calibration. **Fig Aa** shows a simple circuit that will turn off current in a load 18 nsec after that current exceeds a preset value. The circuit is especially versatile because one side of the load is grounded.

Under normal conditions, $Q_1$'s emitter is biased on and supplying power to the load via the 10Ω current shunt. Differential amplifier $IC_1$'s output signal resides below comparator $IC_2$'s voltage-programmed trip point, and $Q_2$ is off.

When an overload occurs, $Q_1$'s emitter current begins to increase (**Fig Ab,** trace A, just prior to the third vertical division). $IC_1$'s output voltage (trace B) begins to rise as it tracks the increase in voltage across the 10Ω shunt. The 9-kΩ, 1-kΩ voltage dividers keep $IC_1$'s input pins within their common-mode range. $Q_1$'s emitter voltage (trace C) begins to drop as the transistor beta-limits. When $IC_1$'s version of the load current exceeds $IC_2$'s trip point, $IC_2$ goes high (trace D), which turns on $Q_2$. (Local positive feedback at $IC_2$'s latch pin causes $IC_2$ to latch in this off state.) $Q_2$ steals $Q_1$'s base drive, thus turning off the load current.

Once you've cleared the load fault, you can use the push button to reset the circuit. The delay from the onset of excessive load current to complete circuit shutdown is less than 18 nsec. (When interpreting the **Fig Ab** waveforms, note that trace A's current probe has a 4-nsec delay.) To calibrate the circuit, ground $Q_2$'s base and install a 250-mA load. Adjust the 200Ω trim for a 2.5V output signal at $IC_1$. Next, remove the load, unground $Q_2$'s base, and press the reset button. Finally, set the desired trip voltage, and the circuit is ready for use.

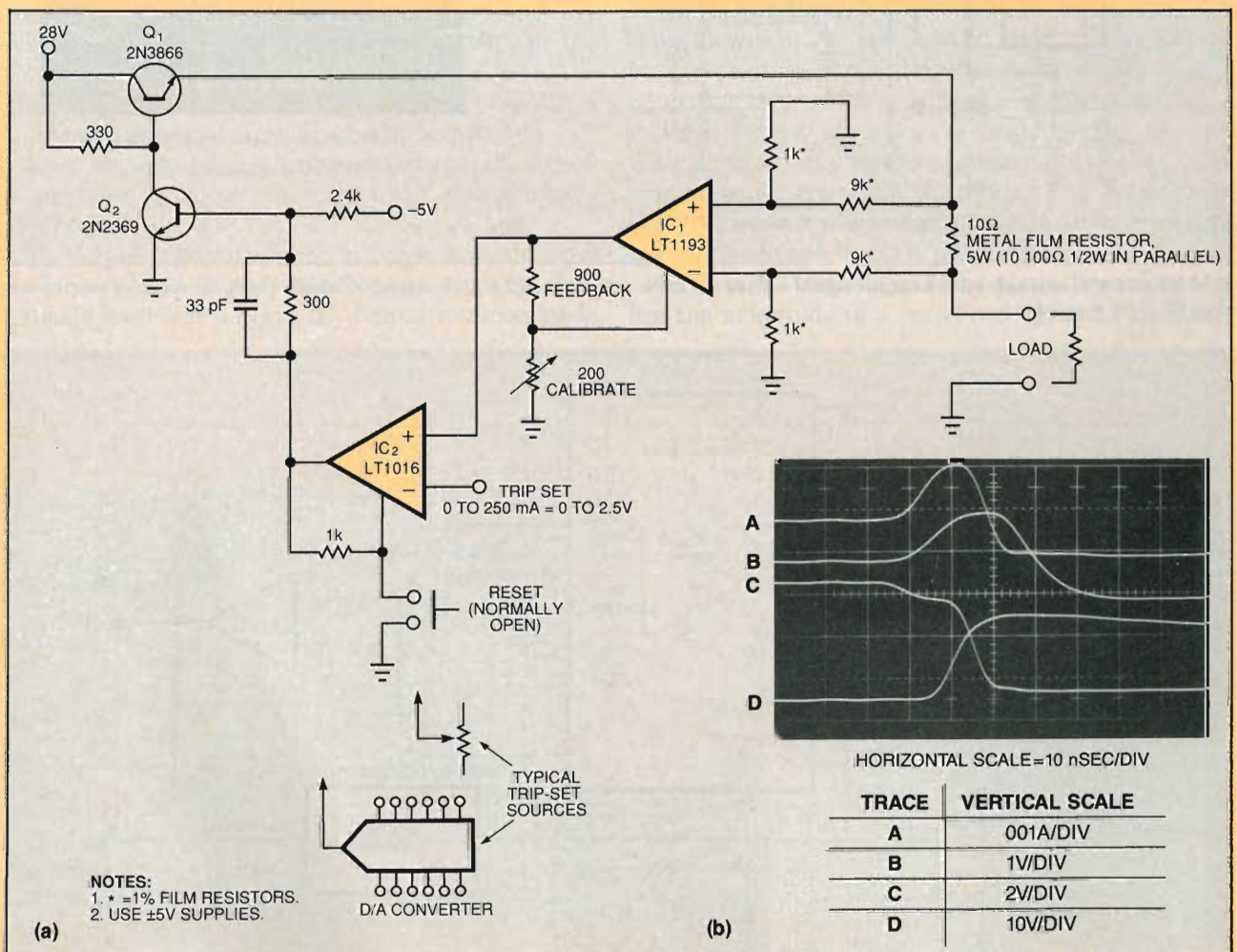



***Fig A—This circuit breaker (a) trips** in as little as 18 nsec. The circuit shuts down the load (**b,** trace C) when the load current (trace A) exceeds the trip point. Trace B represents $IC_1$'s output voltage; trace D represents $IC_2$'s output voltage.*

$Q_4$'s emitter capacitor retains the minimum excursion. The dc value of the midpoint of $IC_2$'s output signal appears at the junction of the 500-pF capacitor and the 22-MΩ resistors. This point will always be midway between the signal's excursions, regardless of the signal's absolute amplitude. The low-bias LT1097 op amp ($IC_3$) buffers this signal-adaptive voltage to set the trigger voltage at $IC_4$'s positive input pin. $IC_4$'s negative input pin is biased directly from $IC_2$'s output.

**Fig 4b** shows the results of using the test circuit of **Fig 4a**. The pulse generator's output signal is trace A; $IC_2$'s analog output voltage is trace B. $IC_4$'s output signal is trace C. The waveforms were recorded using a 5-μA photocurrent at about 20 MHz as the test signal.

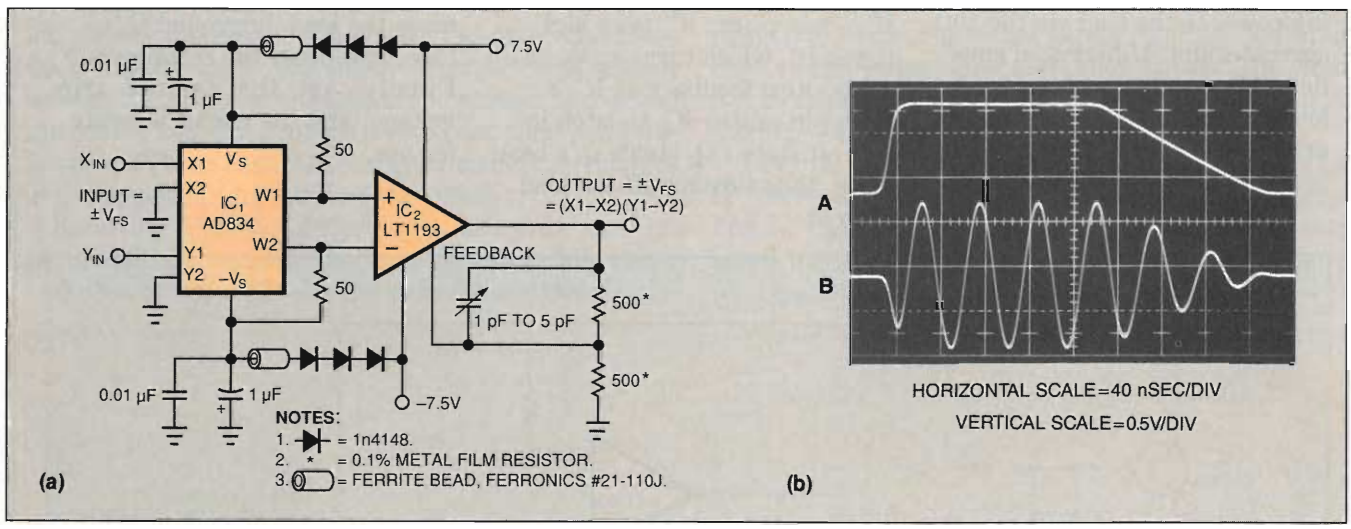



***Fig 5—This mixer's (a) single-ended output signal** is easier to work with than differential signals. Trace B **(b)** is the result of mixing trace A with a 20-MHz sine wave.*

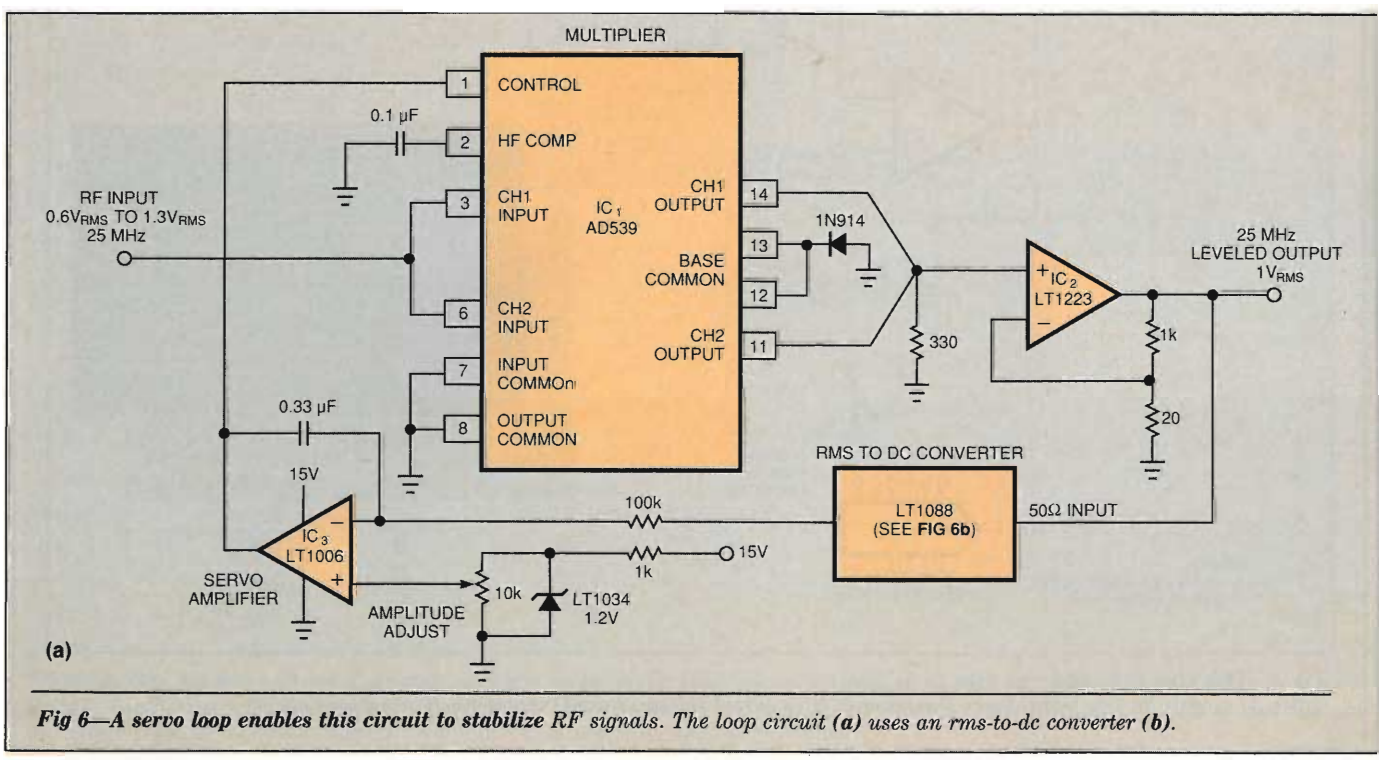



***Fig 6—A servo loop enables this circuit to stabilize** RF signals. The loop circuit **(a)** uses an rms-to-dc converter **(b)**.*

Note that $IC_4$'s output transitions (trace C) correspond with the midpoint (plus $IC_4$'s 10-nsec propagation delay) of $IC_2$'s output signal (trace B), in accordance with the adaptive-trigger circuit's operation.

### Mixer yields single-ended signal

Another common communications requirement, particularly for RF work, is mixing signals for modulation or heterodyning. Analog multipliers can mix signals, but they have a drawback; their output signals take a differential form. These differential signals, which have substantial common-mode content, are frequently inconvenient to work with. You can use RF transformers to convert them to single-ended signals, but you lose dc and low-frequency information in the process. **Fig 5a** illustrates a better approach. The circuit uses the LT1193 differential amplifier ($IC_2$) to accomplish the differential-to-single-ended transition. Set up $IC_1$ in the configuration **Ref 1** recommends. The LT1193 takes the differential signal from $IC_1$'s 50Ω-terminated output lines and provides a single-ended output signal. The amplifier's gain of 2 yields an 11V output signal at full scale.

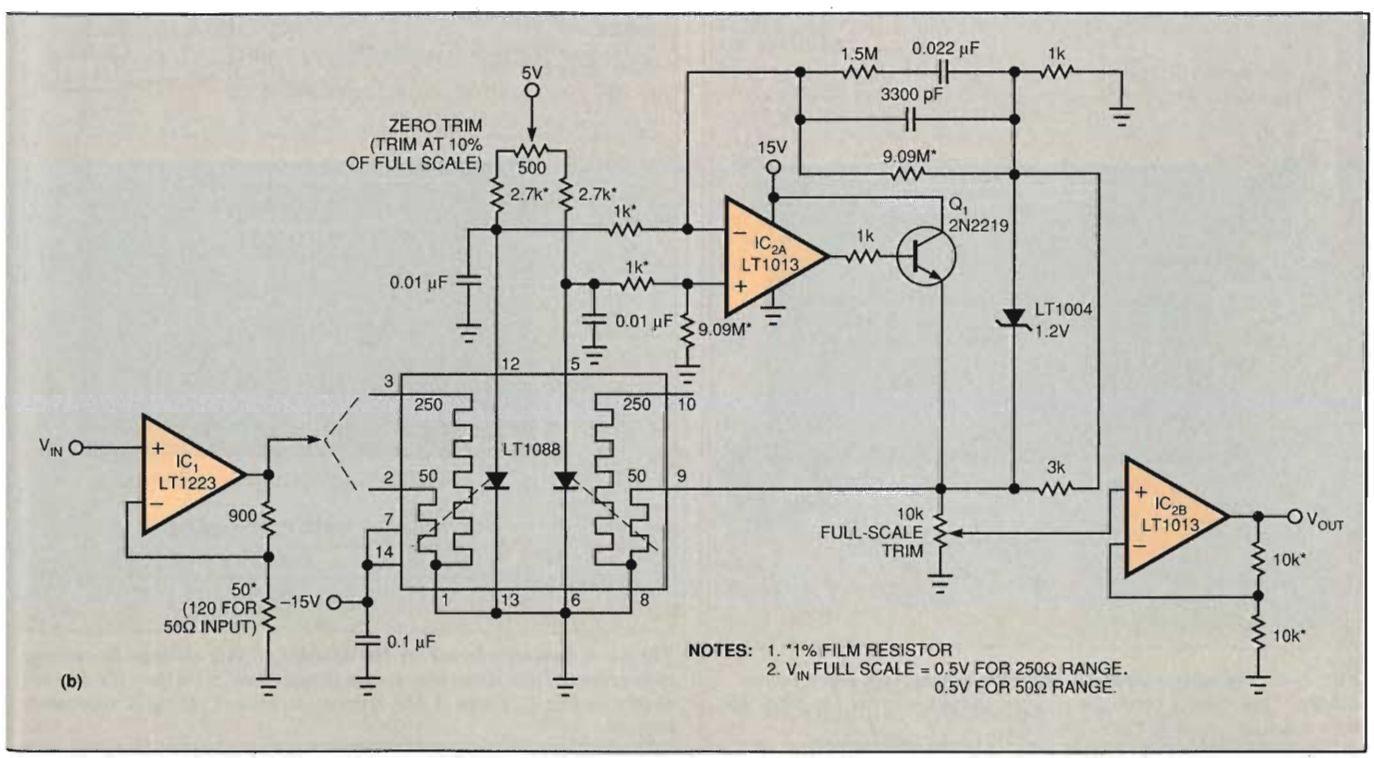
$IC_1$'s output signals ride on a common-mode level quite close to the device's positive supply. This common-mode level falls outside $IC_2$'s input common-mode range. The diodes in the 7.5V supply rails drop the supply voltage to $IC_1$, which biases $IC_1$'s output signals within $IC_2$'s input range. This scheme avoids the attenuation and matching problems you'd get if you placed a level shift between the multiplier and amplifier. The impedance of the ferrite beads combine with the diodes' impedance to ensure adequate bypassing for the multiplier.

This circuit's performance is quite impressive. Error remains within 2% over dc to 50 MHz, and feedthrough is less than −50 dB. Trimming the circuit involves adjusting the variable capacitor at the amplifier for minimal output square-wave peaking. **Fig 5b** shows the circuit's performance when multiplying a 20-MHz sine wave by trace A's waveform. The output signal (trace B) is a singularly clean instantaneous representation of the X and Y input products.

Often in RF communications you will want to stabilize the amplitude of a waveform against variations in

### Acronyms used in this article

**FET**—Field-effect transistor
**RF**—Radio frequency
**rms**—Root mean square



input signal strength over time and temperature. Instruments and transmitters must often provide this function, which is not easy if the instruments must also maintain waveform purity. **Fig 6a** shows a circuit that stabilizes waveform amplitudes while maintaining waveform purity.

You apply the RF input signal to the AD539 wideband multiplier ($IC_1$), which drives $IC_2$. An LT1088-based rms-to-dc converter **(Fig 6b)** turns $IC_2$'s output to dc. A servo amplifier ($IC_3$) compares that dc output signal with a settable dc reference and biases the multiplier's control channel, thus completing a loop. The 0.33-µF capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo amplifier. The loop maintains the output's 25-MHz rms amplitude at the dc reference's value; it rejects changes in load, input-signal strength, power-supply voltage, and other variables.

All of the previous circuits have a voltage-based output signal. Sometimes, however, you'll want your output in current form. **Fig 7a** shows a voltage-controlled current source that has both the load and control voltage referenced to ground. This simple, powerful circuit produces output current in accordance with the sign

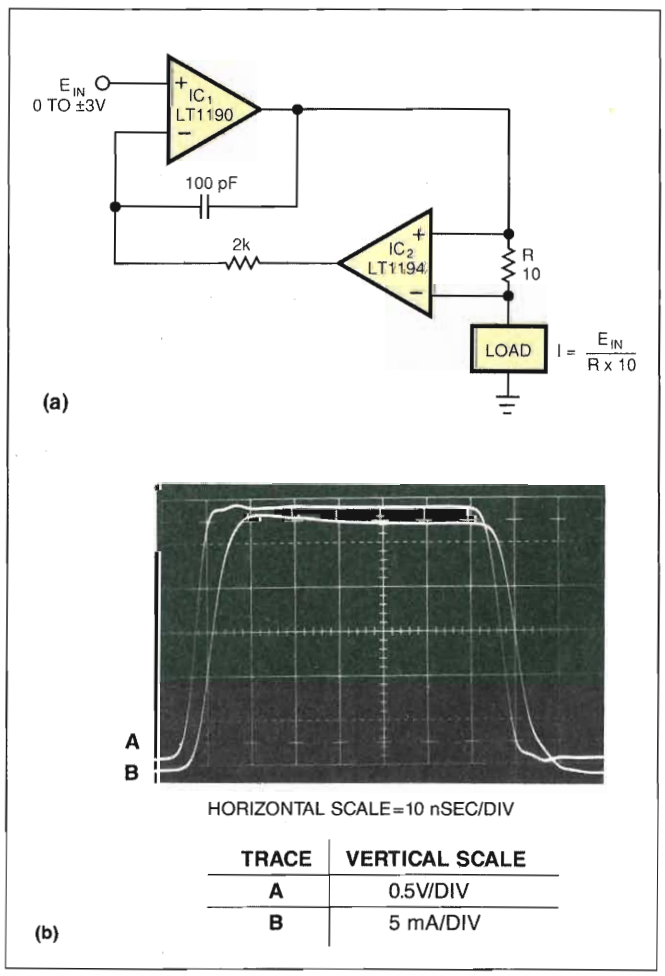



***Fig 7—A voltage-controlled current source (a)*** *often comes in handy. This circuit produces a clean output current (**b**, trace B) 4 nsec after the input voltage (trace A).*

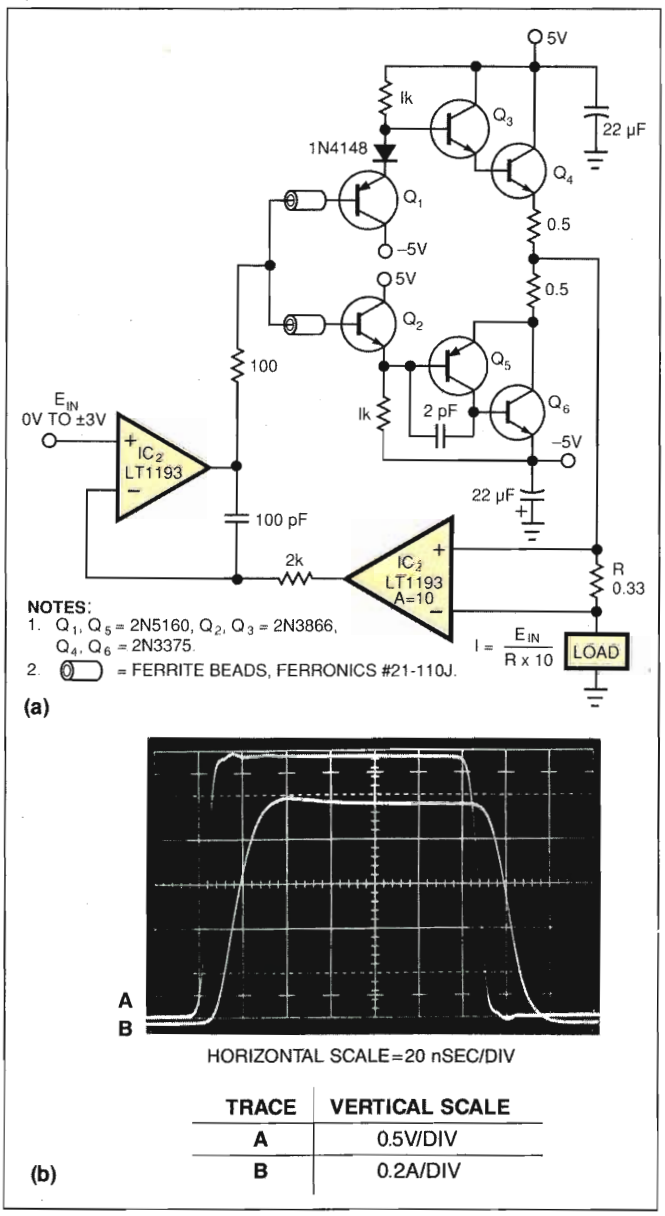



***Fig 8—A booster circuit in the middle of this voltage-to-current converter (a)*** *provides more power to your load than does the current source of **Fig 7**. Trace A **(b)** represents voltage; trace B represents current.*

and magnitude of the control voltage. Resistor R sets the circuit's scale factor.

$IC_1$, biased by $E_{IN}$, drives current through R (in this case 10Ω) and the load. $IC_2$, sensing the differential voltage across R, closes a loop back to $IC_1$. The load current is constant because $IC_1$'s loop forces a fixed voltage across R. The 2-kΩ, 100-pF combination sets roll-off, and the configuration is stable. **Fig 7b** shows the circuit's dynamic response. Trace A is the control input voltage, $E_{IN}$; trace B is the output current. The response has a delay of 5 nsec and no slew residue or aberrations.

**Fig 8a** is **Fig 7a**'s basic current source plus a 1A booster stage to increase output power. Including the booster inside $IC_1$'s feedback loop eliminates the booster's dc errors. Note that the booster needs no current-limiting features because of the circuit's inherent current-limiting operation. **Fig 8b** shows that the circuit's response is as clean as that of the lower-power version, although its delay is about 20 nsec slower. The loop stability considerations involved in placing $IC_2$ and the booster in $IC_1$'s feedback path are significant. This type of circuit receives detailed treatment in **Ref 2.** EDN

## References

1. Analog Devices Inc, *Linear Products Databook*, AD834 Datasheet, pgs 6-43.
2. Williams, Jim, "Subduing high-speed op-amp problems," *EDN*, October 24, 1991, pg 135.

## Author's biography

*For more information on this article's author, turn to pg 163 in the October 10, 1991 issue.*

THE JIM WILLIAMS PAPERS

# High-speed data-conversion circuits

The variety of circuits that prove useful in high-speed data conversion is almost limitless. Here is a collection of circuits that can turn out to be lifesavers in several situations.

Jim Williams, *Linear Technology Corp*

Any reasonably complete listing of the types of circuits that you can use in data conversion and analog/digital data acquisition would be long indeed. Although books have been written just on D/A and A/D converters, such circuits are hardly the only ones that prove useful in acquiring fast-changing analog signals. You almost can't mention ADCs without also bringing up sample and hold (S/H) circuits. Voltage-to-frequency converters offer a very attractive alternative to more conventional ADCs, especially where you need signal isolation or outstanding linearity. Comparators are the heart of any analog-to-digital conversion scheme. Trigger circuits let you view and capture waveforms that recur at intervals that aren't perfectly periodic. Time-to-voltage converters let you see how pulse widths and time intervals vary as a function of time, and rms-to-dc converters extract an important property of ac signals—their heating value. There is a measure of commonality among the techniques you use to design such circuits. Here for your entertainment and edification is a potpourri of useful circuits that perform diverse functions.

In **Fig 1a**, the LT1016 comparator and the LT1122 high-speed FET amplifier combine to form a high-speed V/F converter. A variety of circuit techniques yields a 1-Hz to 10-MHz output. The circuit continues to function with a 20% overrange ($V_{IN}=12V$; $f_{OUT}=12$ MHz). This circuit has a wider dynamic range (140 dB, or seven decades) than any unit available commercially. The 10-MHz full-scale frequency is 10× as high as that of currently available monolithic V/F converters.

The theory of operation depends on the identity $Q=CV$. Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (7). The circuit's input furnishes a comparison current at the summing node and a monitoring amplifier's feedback capacitor integrates the difference signal. The amplifier controls the circuit's output-pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency at which the pumped charge just offsets the current produced by the input signal. Thus, the output frequency is linearly proportional to the input voltage.

$IC_1$ is the integrating amplifier. Stabilizing $IC_1$ with $IC_2$, a chopper-stabilized op amp, produces 0.05 μV/°C of offset drift. $IC_2$ measures the dc value of the negative input, compares it with ground, and forces the positive input to maintain the offset balance in $IC_1$.

Note that $IC_2$ is an integrator that cannot see high-frequency signals. It functions only at dc and low frequencies.

Integrator $IC_1$ has a 68-pF feedback capacitor. When you apply a positive voltage to the input, $IC_1$'s output integrates in a negative direction (**Fig 1b,** trace A). During this period, $IC_5$'s inverting output is low. The paralleled HCMOS inverters form a reference-voltage switch. The LT1034s (driven by the LM134 current source and the $Q_3/Q_4$ combination) establish the reference voltage; a small input-voltage-related term adds to the reference, improving overall circuit linearity.

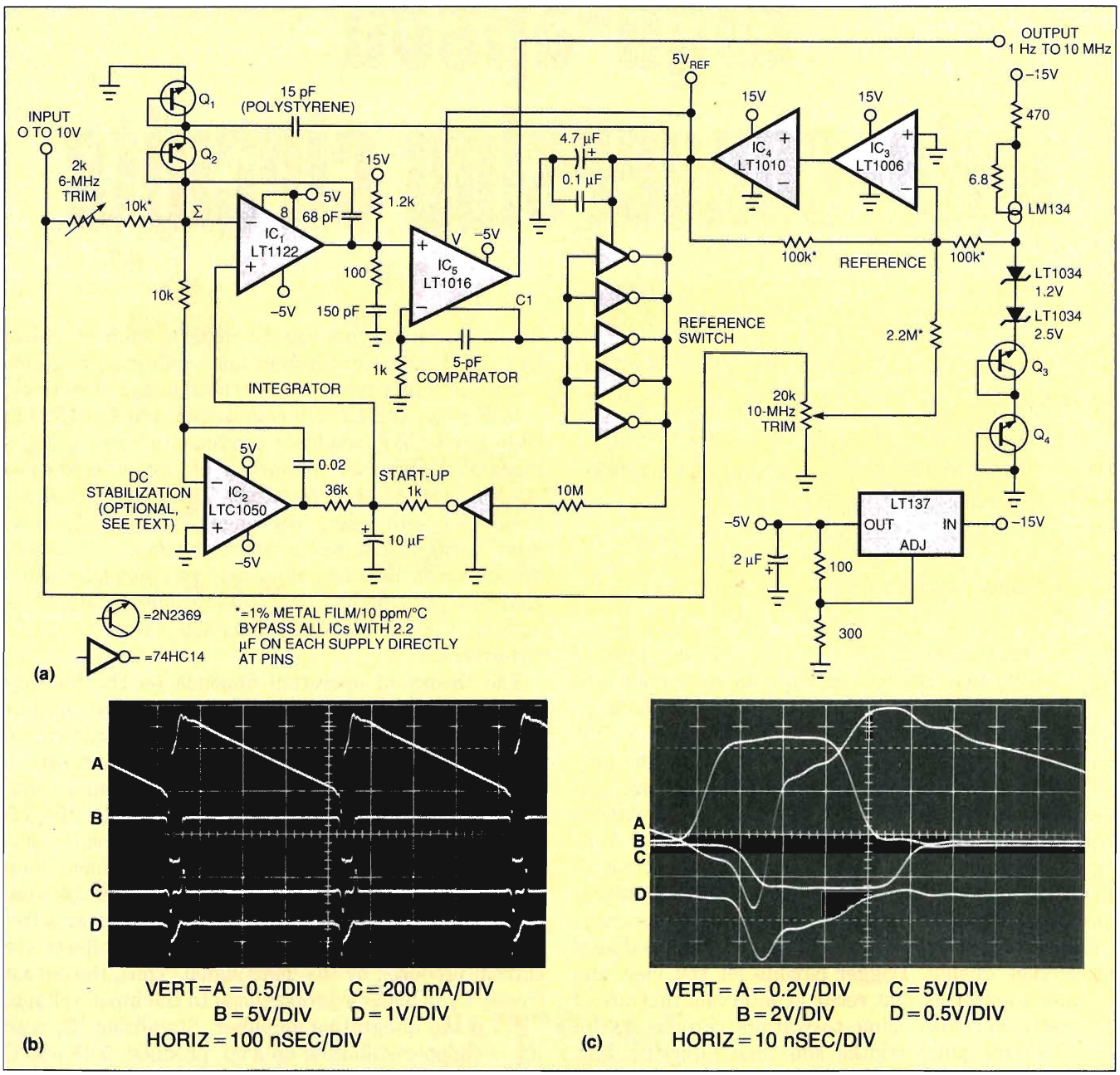



***Fig 1—A voltage-to-frequency converter*** *with a maximum output frequency of 10 MHz and a 140-dB dynamic range is only moderately complex (**a**). In **b**, you see the circuit waveforms; **c** is an expanded view of the discharge-reset sequence upon which the circuit performance depends.*

$IC_3$ and $IC_4$ provide low-drift buffering and present a low-impedance reference to the supply pins of the paralleled inverters. The HCMOS outputs give essentially error-free low-resistance switching. The reference switch's output charges the 15-pF capacitor via the path that includes $Q_1$.

When $IC_1$'s output crosses zero, $IC_5$'s inverting output goes high and the reference switch (trace B) goes to ground, causing the 15-pF capacitor to dispense charge into the summing node via $Q_2$'s base-emitter junction. The amount of charge dispensed is a direct function of the voltage that had existed across the 15-pF capacitor ($Q=CV$). $Q_3$ and $Q_4$ in the reference string provide temperature compensation for $Q_1$ and $Q_2$. The current that flows through the 15-pF capacitor (trace C) reflects the charge-pumping action. Removing current from $IC_1$'s summing junction (trace D) drives the junction negative very quickly. The initial negative-going 15-nsec transient at $IC_1$'s output results from amplifier delay.

The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (trace A) slew limits as the amplifier attempts to regain control of the summing node. The 1.2-kΩ pull-up resistor and the RC damper at $IC_1$'s output enhance the amplifier's recovery from slewing. The amount of time the reference switch remains at ground depends on the 5-pF/1000Ω hysteresis network at $IC_5$ and on how long $IC_1$ takes to recover. A 60-nsec interval is long enough for the 15-pF capacitor to fully discharge. After the discharge, $IC_5$ changes state, the reference switch swings positive, the capacitor recharges, and the entire cycle repeats. The frequency at which this oscillation occurs is directly proportional to the current into the summing junction, and, in turn, to the input voltage. Any input current will dictate an oscillation frequency that holds the summing point at an average value of zero.

At MHz frequencies, maintaining a linear relationship between the input voltage and the output frequency places severe restrictions on the circuit timing. The key to achieving a 10-MHz full-scale operating frequency is the ability to transmit information around the loop very quickly. The discharge-reset sequence detailed in **Fig 1c** is particularly critical.

**Fig 1c**, trace A is the output of integrator $IC_1$. Its ramp output crosses zero at the first vertical graticule division on the left. A few nsec later, $IC_5$'s inverting output begins to rise (trace B), switching the reference switch to ground (trace C). The reference switch begins to head towards ground about 16 nsec after $IC_1$'s output crosses zero. Two nanoseconds later, the summing point (trace D) begins to go negative as current flows from it through the 15-pF capacitor. At 25 nsec, $IC_5$'s inverting output is fully positive, the reference switch is at ground, and the summing point is at its negative extreme. Now, $IC_1$ begins to take control. Its output (trace A) slews rapidly in the positive direction, restoring the summing point. At 60 nsec, $IC_1$ is in control of the summing node and the integration ramp begins again.

### Come on, get going

Start-up and overdrive conditions could force $IC_1$'s output to go to the negative rail and stay there. The ac-coupled nature of the charge-dispensing loop can preclude normal operation and cause the circuit to latch. The remaining HCMOS inverter provides a "watchdog" function for this condition. If $IC_1$'s output goes to the negative rail, the reference switch tries to stay at ground. The remaining inverter goes high, lifting $IC_1$'s positive input, causing $IC_1$'s output to slew positive, and thus initiating normal circuit action. The 1-kΩ/10-μF combination and the 10-MΩ resistor in series with the inverter input limit the loop bandwidth during start-up, preventing unwanted outputs.

The LM134 current source that drives the reference string has a built-in 0.33%/°C thermal coefficient, causing a slight voltage modulation in the $Q_3/Q_4$ pair over temperature. This small change (~+120 ppm/°C) opposes the −120 ppm/°C drift in the 15-pF polystyrene capacitor and reduces the temperature coefficient of the complete circuit.

### Acroynms used in this article

**ac**—Alternating current
**A/D**—Analog-to-digital
**ADC**—Analog-to-digital converter
**D/A**—Digital-to-analog
**DAC**—Digital-to-analog converter
**dc**—Direct current
**FET**—Field-effect transistor
**LSB**—Least-significant bit
**RC**—Resistance-capacitance
**rms**—Root-mean-square
**S/H**—Sample and hold
**TTL**—Transistor-transistor logic
**V/F**—Voltage to frequency
**VFC**—Voltage-to-frequency converter

To trim this circuit, apply exactly 6V at the input and adjust the 2-kΩ potentiometer for 6.000-MHz output. Next, put in exactly 10V and trim the 20-kΩ potentiometer for a 10.000-MHz output. Repeat these adjustments until both points stay fixed. $IC_2$'s low drift eliminates a zero adjustment. If operation below 600 Hz is not required, you can delete $IC_2$ and its associated components.

Nonlinearity of this circuit is 0.03% and full-scale drift is 50 ppm/°C. Zero-point error, controlled by $IC_2$, is 0.05 Hz/°C.

**Fig 2a** shows a simple, very fast S/H circuit. This circuit will acquire a 5V input to 8-bit accuracy in 100 nsec. The hold step amplitude is less than ¼ LSB, and hold settling time is less than 25 nsec. The aperture time is 4 nsec, and the droop rate is about ½ LSB in 1 μsec.

Inverting buffer $IC_1$ feeds the input to a Schottky switching bridge. The Schottky bridge, which is similar to types used in sampling oscilloscopes, switches in 1 nsec and eliminates the charge pump-through that an FET switch would contribute. The switching bridge's output feeds output-amplifier $IC_2$. $IC_2$, configured as

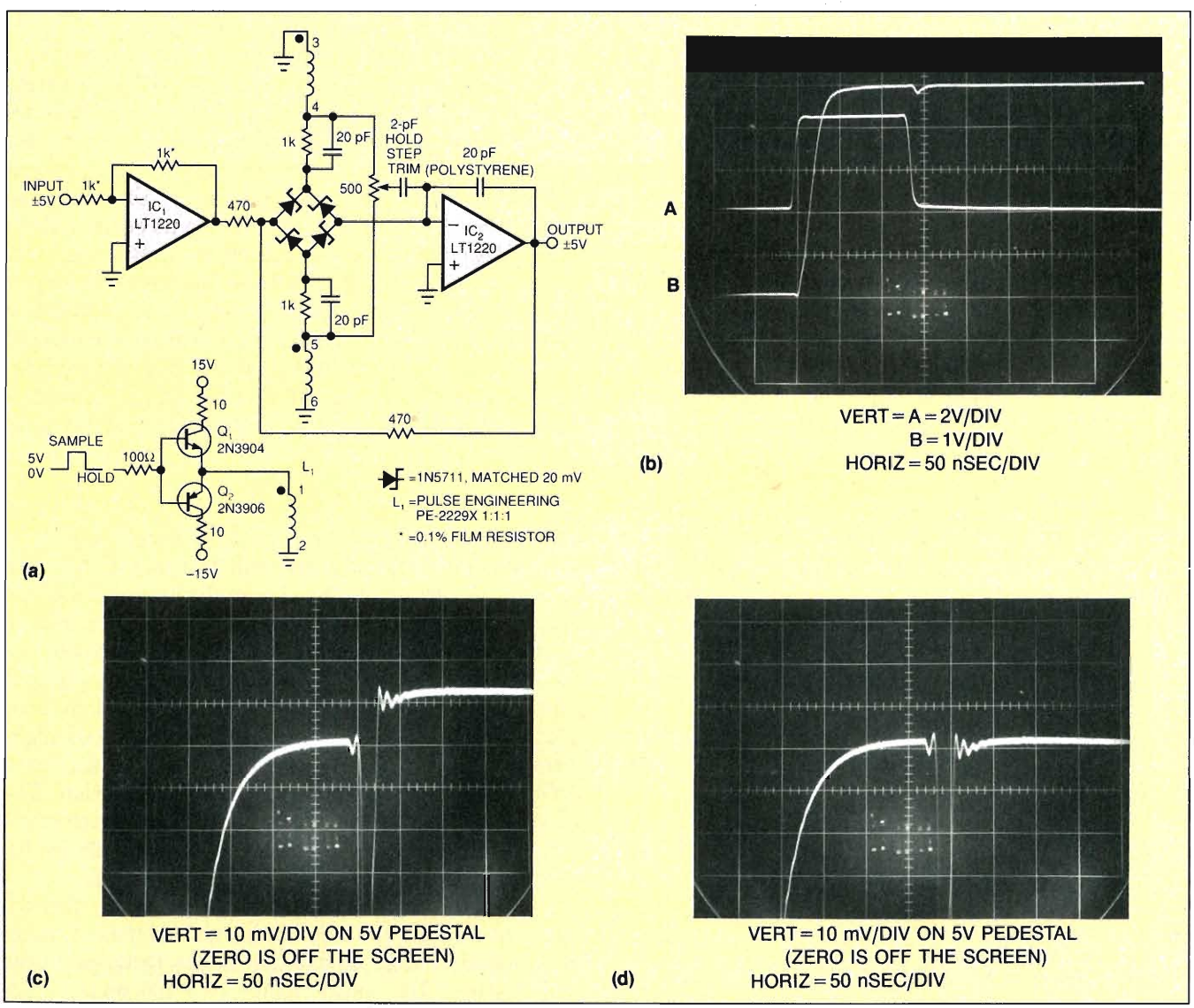



***Fig 2—This very fast S/H circuit (a),*** *acquires signals to 8-bit accuracy in 100 nsec. In* ***b*** *you see the waveforms within the circuit. Accurate operation depends on cancellation of the switching signals that feed through the bridge. In* ***c****, the compensation is disconnected. In* ***d****, you can see the effect of the compensation.*

an integrator, is the actual hold amplifier. Its output feeds back to the switching bridge's input, forming a summing point with $IC_1$'s output resistor. This feedback loop enhances accuracy by placing the bridge within a loop.

Driving the S/H input line switches the bridge. $Q_1$ and $Q_2$ drive $L_1$'s primary. $L_1$'s secondaries provide complementary drive to the bridge with negligible time skew.

**Fig 2b** shows the circuit acquiring a full-scale step. Trace A is the input command; trace B is $IC_2$'s output. The aberration (that is, the "hold step") visible in $IC_2$'s output when the circuit switches into the hold mode is the result of minute residual ac imbalances in the bridge. **Fig 2c** illustrates this effect in high-resolution detail, with the "hold-step trim" deliberately disconnected. After $IC_2$'s output nominally settles at final value, the circuit switches into the hold mode. The bridge imbalance dumps a small parasitic charge into $IC_2$'s summing point, in this case causing $IC_2$ to step 10 mV higher. Properly connected and adjusted, the trim supplies a small compensatory charge during switching. **Fig 2d** shows the effect of this compensation on the output. The settled hold-mode output is the same as the acquired input voltage. To trim this circuit, ground the input while pulsing the S/H control line. Next, adjust the trim for a minimal amplitude step between the S/H states.

In contrast to low-frequency S/H circuits, this circuit, if left in the sample mode, cannot pass a signal. The transformers' inherent ac coupling prevents the circuit from providing a dc output. Moreover, extending the sample-mode duration beyond 500 nsec will saturate the transformers, causing erroneous outputs and excessive dissipation in $Q_1$ and $Q_2$. If the control input can remain in the high state for extended periods, you should ac-couple the control signal.

### Compare currents in 15 nsec

**Fig 3a** shows a way to build a high-speed current comparator with resolution in the 12-bit range. Comparing currents, which is the fastest way to compare DAC outputs with analog values, is a common technique in high-speed instrumentation, especially in high-speed A/D converters. $IC_1$ is a Schottky-bounded amplifier. The bounding diodes hold down the response time by preventing summing-point overdrive from causing $IC_1$ to saturate. Select the capacitor—it compensates for the DAC output capacitance—for the best amplifier damping; the 3-pF value shown is typical. The feedback resistor maximizes the circuit's gain-bandwidth product; the 10-kΩ value shown is also typical. Voltage gains of 4 to 10 are common.

**Fig 3b** shows the circuit's performance. Trace A, a test input, causes $IC_1$'s output (trace B) to slew through zero (the screen's center horizontal line). When $IC_1$ crosses zero, $IC_2$'s input goes negative and $IC_2$ responds 10 nsec later with a TTL output (trace C). The total time from when the test input reaches the TTL high threshold until the comparator output level becomes a TTL high is <15 nsec.

**Fig 4a** is an extremely versatile trigger circuit. Designing a fast, stable trigger is not easy, and often entails a considerable number of discrete components.

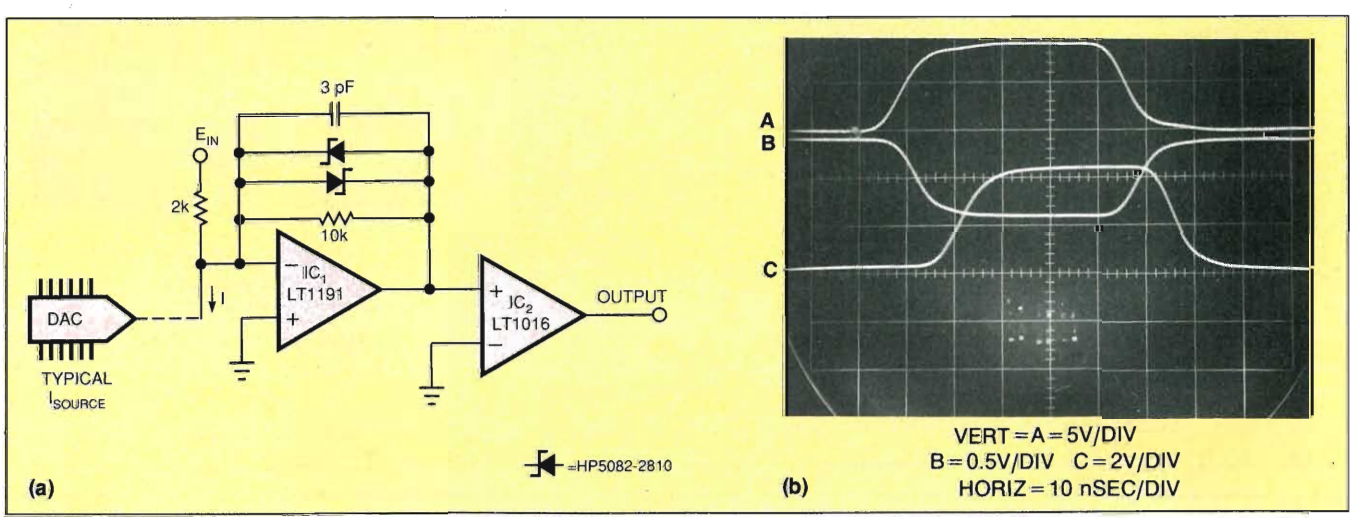



***Fig 3—Only two ICs yield a fast** summing comparator **(a)**. In **b**, you can observe key waveforms as the circuit operates.*

This circuit, without level adjustment, triggers reliably from dc to 50 MHz over a 2 to 300-mV input range.

$IC_1$, a gain-of-10 preamplifier, feeds an adaptive trigger configuration that maintains the output comparator's ($IC_3$'s) trip point at one-half the input-signal amplitude, regardless of the signal's magnitude. The self-adjusting trip point ensures reliable automatic triggering over a wide input-amplitude range, even for very low-level inputs. As an option, the network (shown in dashed lines in **Fig 4a**) permits changing the trip threshold. The adjustment lets you select any point on the input-waveform edge as the trigger point.

**Fig 4b** shows the performance for a 40-MHz input sine wave (trace A). At $IC_1$'s output (trace B), the input signal has received voltage gain with little or no phase shift. Comparator $IC_3$ gives a clean logic output (trace C). At the highest frequencies, bandwidth limiting can occur in $IC_1$, but it is irrelevant; the adaptive trigger threshold will simply vary in proportion to the input to maintain the circuit output.

The circuit of **Fig 5a** lets you determine very short pulse widths (in this case, 250 nsec full scale) with a typical error of 1%. Digital methods of achieving similar results dictate GHz clock speeds, and thus result in cumbersome implementations. In addition, processor-based approaches that use averaging techniques require repetitive pulses; this circuit does not. Circuits of the type shown in **Fig 5a** frequently appear in automatic test equipment and nuclear and high-energy physics work, where measuring the width of short pulses is a common requirement.

The circuit functions by charging a capacitor for the duration of the pulse. When the pulse ends, the charging ceases, and the voltage across the capacitor is proportional to the width of the pulse.

The pulse whose width is to be measured (**Fig 5b**, trace A) simultaneously biases the 74C221 dual one-shot and $Q_3$. $Q_3$, aided by Baker clamping, feed-forward capacitance, and optimized dc base biasing, turns off in a few nsec. Current source $Q_2$'s emitter becomes forward biased, and $Q_2$ supplies constant current to the 100-pF integrating capacitor. $Q_1$ supplies temperature compensation for $Q_2$ and the 2.5V LT1009 provides the current-source reference. The 100-pF capacitor at $Q_2$'s collector charges in ramp fashion (trace B). $IC_1$ supplies a buffered output (trace C). When the input

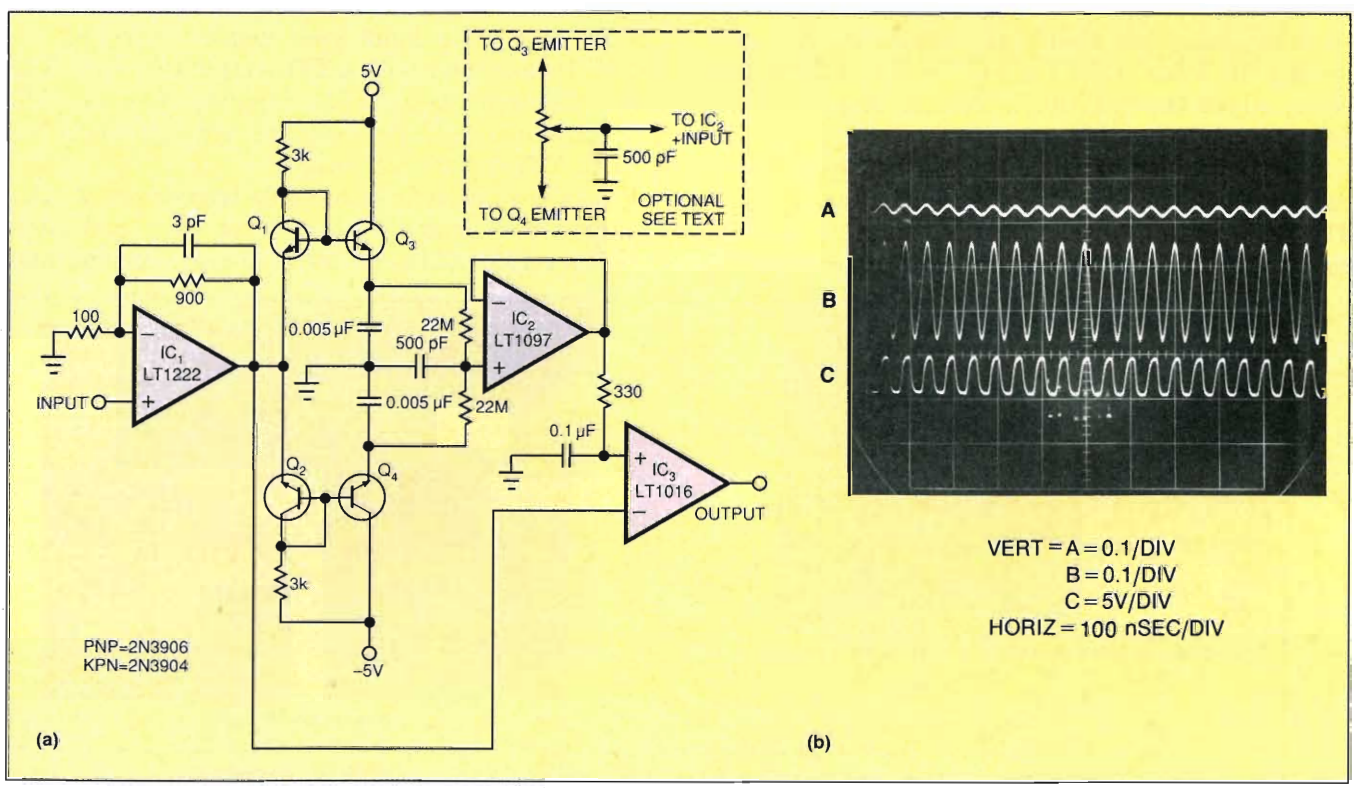



***Fig 4—An extremely versatile trigger*** *circuit (**a**) consists of three ICs and two pairs of transistors, each connected as a current source. The circuit adjusts its threshold as the amplitude of the incoming signal varies. In **b**, you see waveforms during circuit operation.*

pulse ends, $Q_3$ turns on rapidly, reverse-biasing $Q_2$'s emitter and turning off the current source. $IC_1$'s voltage is directly proportional to the input pulse width. A monitoring A/D converter can acquire this data.

After an interval set by the 74C221's delay (a resistor and a capacitor set the delay), a pulse appears at the circuit's $Q_2$ output (trace D). This pulse turns on $Q_4$, discharging the 100-pF capacitor to zero and readying the circuit for the next input pulse.

This circuit's accuracy and resolution depend strongly on keeping the delay in switching the $Q_1/Q_2$ current source very short. **Fig 5c** provides amplitude and time-expanded versions of critical circuit waveforms. Trace A is the input pulse and trace B is $IC_1$'s input, showing the beginning of the ramp's ascent. Trace C, $IC_1$'s output, shows a delay of about 13 nsec from $IC_1$'s input. Traces D and E, also $IC_1$'s input and output, record similar delays introduced by $IC_1$ at the ramp turn-off. The photo reflects the extremely fast current-source switching; $IC_1$ causes most of the delay. $IC_1$'s delay is far less critical than the current-source-switching delays. $IC_1$ will always settle to the correct

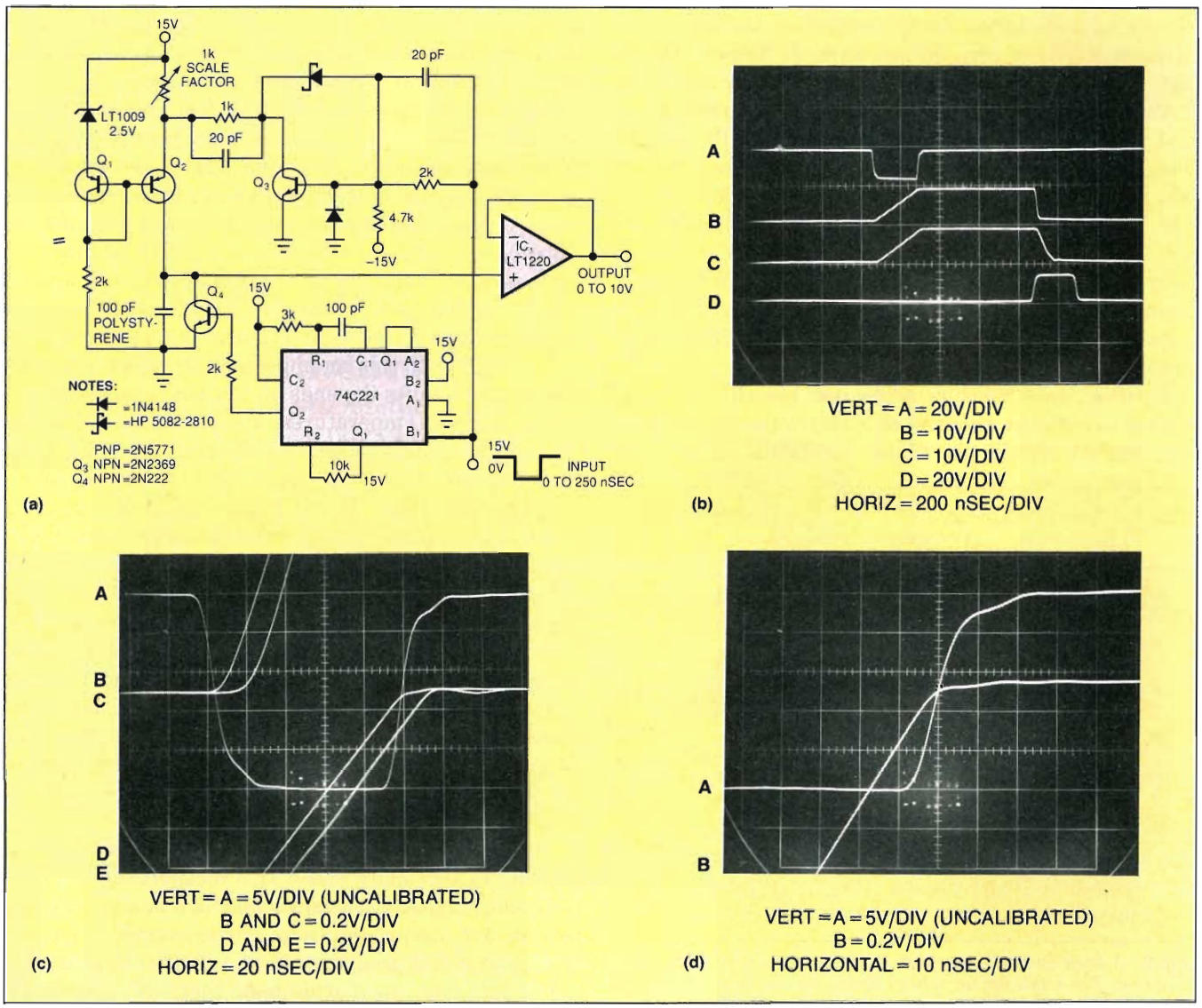



***Fig 5—Changing pulse widths to voltages*** *provides a convenient way to monitor changes in time intervals that occur as a function of time. The circuit in* ***a*** *performs this function. In* ***b*** *you see circuit waveforms. These waveforms appear in expanded form in* ***c****. The current-source turn-off appears in* ***d****.*

value well before the one-shot resets the circuit. In practice, you should not trigger a monitoring A/D converter until about 50 nsec after the circuit's input pulse has ceased. This delay gives $IC_1$ plenty of time to catch up to the 100-pF capacitor's settled value.

As mentioned, fast current-source switching is essential for good results. **Fig 5d** details the current-source turn-off. Trace A is the circuit's input-pulse rising edge, and trace B shows the "top" of the ramp. Turn-off occurs in a few nanoseconds. Similar speed is characteristic of the input's falling edge (current-source turn-on). In addition, note that the circuit's accuracy and resolution limits depend on the difference in current-source turn-on and turn-off delays. Therefore, the effective overall delay is extremely small.

To calibrate this circuit, apply a 250-nsec-width pulse and trim the 1-kΩ potentiometer for a 10V output. The circuit will convert pulse widths between 20 and 250 nsec to voltages with an accuracy that is typically 1%. The 20-nsec minimum-measurable width is the result of the 100-pF capacitor's inability to discharge fully. If you must measure the width of pulses narrower than 20 nsec, you can replace $Q_4$ with a lower-saturation-voltage device or you can offset $IC_1$'s output.

Most ac rms measurements use logarithmic techniques to compute a waveform's rms value. Such methods work with signals whose bandwidth is below 1 MHz and whose crest factor is less than about 10. Practically speaking, a waveform's ability to heat a resistive load defines its rms value. Specialized instruments employ thermally based assemblies that compute the rms values of input signals. Compared with logarithmically based converters, thermal methods work over a substantially wider bandwidth and produce accurate results with signals that have much higher crest factors (ratio of peak to rms voltage).

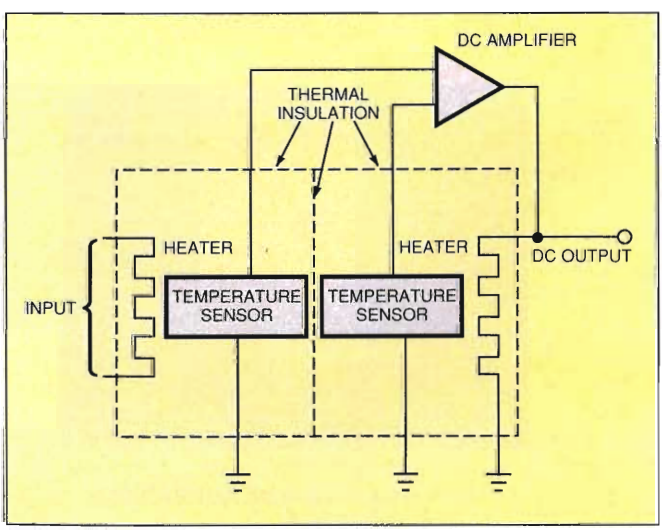



***Fig 6—A basic thermal rms-to-dc converter*** *uses a pair of heating elements. The unknown ac voltage drives one; a dc voltage drives the other. By using a high-gain amplifier to provide the dc voltage, you force the heating effect of the dc to equal that of the ac. Hence the rms value of the dc and ac are equal. Thus, when you measure the dc voltage, you are measuring the rms ac voltage.*

Thermal rms-to-dc converters are direct acting, thermoelectronic analog computers. The thermal technique is explicit, relying on "first principles"—that is, on the *definition* of rms. The simple operation permits wide-band performance unattainable with implicit, indirect methods based on logarithmic computing.

**Fig 6** shows a classic scheme for implementing a thermally based rms-to-dc converter. Here, the dc amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the pair driven by the input. This differentially sensed, feedback-enforced loop makes ambient-temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal interaction is nonlinear, the input-output voltage relationship is linear and has a gain of 1.

The ability of this arrangement to reject ambient-temperature shifts depends on the heater-sensor pairs being at equal temperatures. You can achieve this condition by thermally insulating the sensors with a thermal time constant well below that of any ambient-temperature shifts. If you match the time constants of the heater-sensor pairs, ambient temperature-terms will affect the pairs equally and the dc amplifier will reject this common-mode term. Note that, even though the pairs are at equal temperatures, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This interaction would cause unfavorable signal-to-noise performance and limit the dynamic operating range. The output of **Fig 6**'s circuit is linear because the matched thermal pairs' nonlinear voltage-temperature relationships cancel each other.

The advantages of this approach have made its use popular in thermally based rms measurements. Typically, the assembly consists of matched heater resistors, sensors, and thermal insulation. These assemblies are relatively large and producing them is rather expensive.

**Fig 7a**'s economical wide-band thermally based voltmeter uses a monolithic thermal converter. The LT1223 amplifier provides gain and drives the LT1088 rms-to-dc thermal converter. The supply biases the

LT1088's temperature-sensing diodes. $IC_1$, set up as a differential servo amplifier with a gain of 9000, extracts the diode's difference signal and biases $Q_1$. $Q_1$ drives one of the LT1088's heaters, completing a loop. The 3300-pF capacitor gives a stable roll-off. The 1.5-MΩ/0.0225-μF combination improves settling by reducing the gain during output slewing. The LT1088's square-law thermal gain makes the overall loop gain lower for small inputs. Normally, the low gain would cause slow settling for values below about 10 to 20% of full scale. The LT1004 1-kΩ/3-kΩ network provides a simple breakpoint that boosts the amplifier gain at low signal levels to improve settling. $IC_2$, a gain-trimmable output stage, compensates for gain variations in the two sides of the LT1088.

To trim the circuit, apply a dc signal of about 10% of full scale (that is, 0.05V) and adjust the "zero trim" so that $V_{OUT} = V_{IN}$. Next, apply a full-scale dc input and set the full-scale trim for a full-scale output. Repeat the trims until both errors are well below 1% of full-scale. An alternate trimming scheme involves applying no input, grounding $Q_1$'s base, and adjusting the zero trim until $IC_1$'s output is active. Then you disconnect $Q_1$'s base from ground, apply a full-scale input, and trim the full-scale adjustment to produce a full-scale output.

**Fig 7b** is a plot of the circuit's error vs input fre-

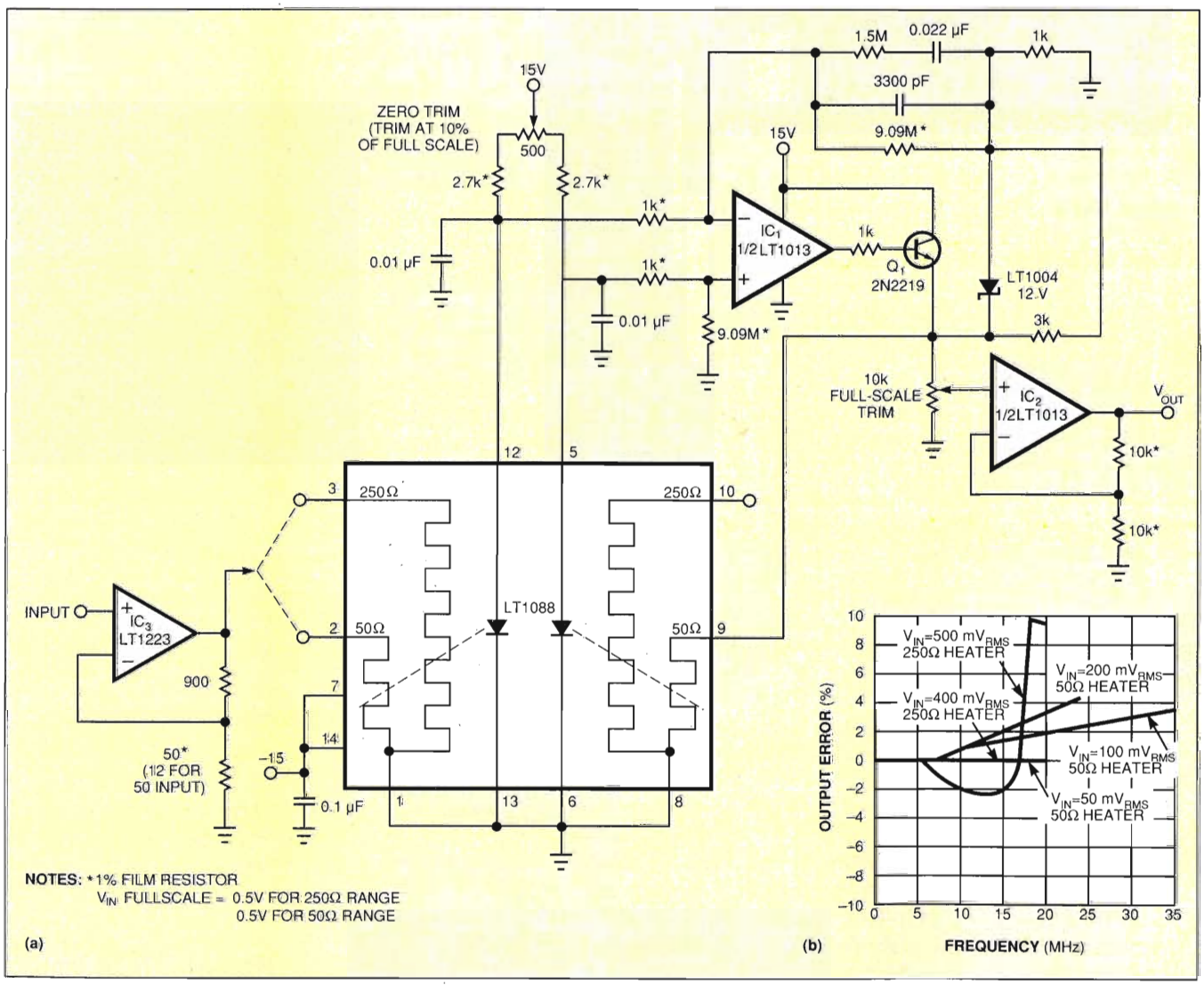



***Fig 7—A functioning rms-to-dc converter*** *appears in* ***a****. In* ***b****, you see the circuit's error vs frequency for several input-signal amplitudes and for two values of heater resistance.*

quency. When you apply your input to one of the 50Ω heaters, the LT1088's error spec is 2% to 100 MHz; using a 250Ω heater, the spec is 1% to 20 MHz. Most of the error shown results from bandwidth restrictions in $IC_3$, but the performance is still impressive. The plots include data taken at various input levels into both a high and a low-resistance heater. The error in the response to a 500-mV input into the 250Ω heater rises to 1% at 8 MHz, and 2.5% at 14 MHz before peaking badly beyond 17 MHz. This input level forces a 9.5V-rms output at $IC_3$, and introduces large-signal bandwidth limitations. The 400-mV input to the 250Ω heater produces essentially flat response to 20 MHz, the LT1088's 250Ω-heater specification limit.

The 50Ω heater provides significantly wider bandwidth, although in the circuit of **Fig 7a**, $IC_3$'s 50-mA output limits the maximum input to about 100-mV rms (1.76V rms at the LT1088).

As you can see, the circuits discussed here are useful in their own right. They are also thought provoking. You can combine and modify them virtually without limit, and in so doing, produce new circuits that perform many other useful functions. EDN

## Author's biography

*For more information on this article's author, turn to pg 163 in the October 10, 1991 issue.*

# AC supply lights cold-cathode fluorescents

**Jim Williams, Linear Technology Corp, Milpitas, CA**

Cold-cathode fluorescent lamps provide the highest-efficiency light source for applications such as backlighting LCDs. These lamps require high-voltage ac. A supply for these lamps should be very efficient and should deliver a sine-wave output to minimize RFI.

The circuit in **Fig 1** meets these requirements. Efficiency is 75% for an input-voltage range of 4.5 to 20V; if you drive the lamp from a separate low-voltage supply (eg, 5V), efficiency is about 82%. Additionally, users can vary a lamp's intensity smoothly from off to full intensity.

In operation, applying power drives the switching regulator's ($IC_1$) feedback pin, $V_{FB}$, below the device's internal 1.23V reference, causing full duty-cycle modulation at $IC_1$'s $V_{SW}$ pin (trace A, **Fig 2**). $L_2$ conducts current (trace B, **Fig 2**), which flows from $L_1$'s center tap, through the transistors, into $L_2$. $IC_1$ conducts $L_2$'s current to ground in switched fashion.

$L_1$ and the transistors compose a current-driven Royer converter, which oscillates at a frequency set by $L_1$'s characteristics and the 0.02-µF capacitor. $L_2$, as switched by $IC_1$, sets the magnitude of the $Q_1/Q_2$ tail current, and hence $L_1$'s drive level. The 1N5818 diode maintains $L_2$'s current flow when $IC_1$ is OFF. $IC_1$'s 40-kHz clock rate is not synchronous with the Royer converter's (≈60 kHz), accounting for trace B's (**Fig 2**) waveform thickening.

The 0.02-µF capacitor combines with $L_1$'s characteristics to produce sine-wave voltage drive at $Q_1$'s and $Q_2$'s collectors (traces C and D, respectively, of **Fig 2**). $L_1$ furnishes voltage step-up, and about 1400V p-p appears at its secondary (trace E, **Fig 2**). Current flows through the 33-pF capacitor into the lamp.

On negative waveform cycles, $D_1$ steers the lamp's current to ground. $D_2$ steers positive waveform cycles to the ground-referenced 562Ω/50-kΩ-potentiometer chain. The positive half-sine appearing across these resistors (trace F, **Fig 2**) represents ½ the lamp's current. The 10-kΩ/1-µF pair filters this signal and presents it to $IC_1$'s feedback pin. This connection closes a control loop that regulates lamp current. The 2-µF capacitor at $IC_1$'s $V_C$ pin provides stable loop compensation. The loop forces $IC_1$ to switch-mode modulate $L_2$'s

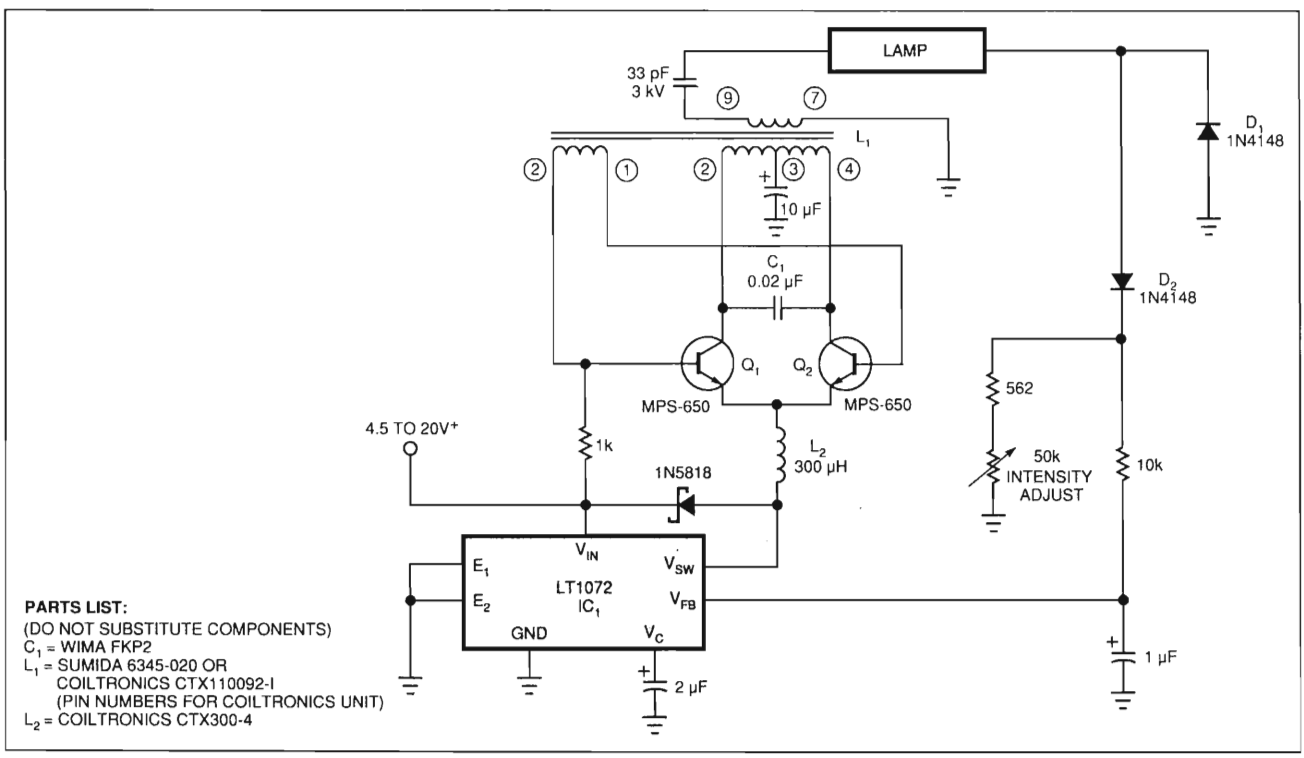



**Fig 1—This high-voltage circuit supplies a constant-current, user-variable, sine-wave drive for cold-cathode fluorescent lamps.**

average current to whatever value is required to maintain a constant current in the lamp. The potentiometer varies the constant current's value, and hence the lamp's intensity. This constant-current drive allows 0- to 100% intensity control with no lamp dead zones or "pop-on" at low intensities. In addition, lamp life is enhanced because current cannot increase as the lamp ages.

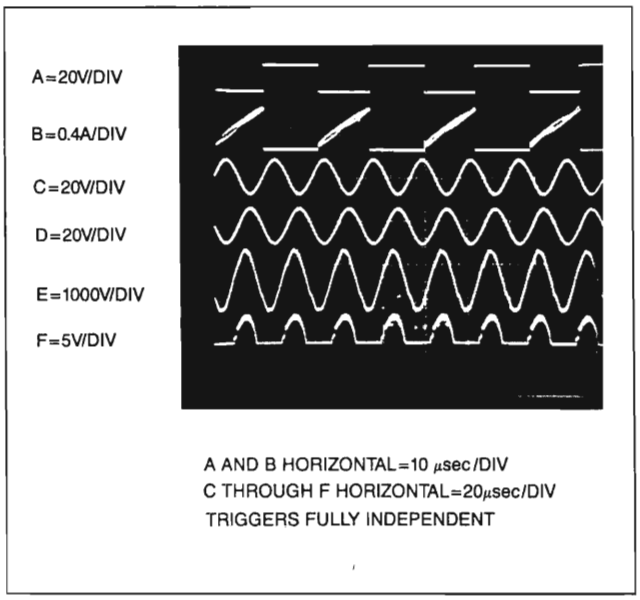



**Fig 2—The circuit in Fig 1 produces a sinusoidal 1400V output (trace E).**

You must keep several points in mind to observe this circuit's operation safely: You can monitor $L_1$'s high-voltage secondary only with a wideband, high-voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if you use them for this measurement.* Tektronix probe type P-6009 (acceptable) or types P6013A and P6015 (preferred) are examples of probes you can use safely.

Another consideration involves observing waveforms. $IC_1$'s switching frequency is completely asynchronous from the Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. A dual-beam oscilloscope (Tektronix 556) produced **Fig 2.** Single-beam oscilloscopes having alternate sweep and trigger switching (eg, Tektronix 547) will also work, but are less versatile and are restricted to four traces.

**EDN BBS /DI_DIG #1091** EDN

# Designing supplies for powering LCD backlighting

Jim Williams, Linear Technology Corp

***Supplies for powering LCD backlights have some unique requirements. The units must be very efficient, have a variable sine-wave output, and include provisions for intensity and contrast control.***

Current-generation portable computers and instruments use backlighted LCDs. Cold-cathode fluorescent lamps (CCFLs) provide the most efficient way for backlighting the display. These lamps require high-voltage ac to operate, so you'll need an efficient high-voltage dc/ac converter. In addition to high efficiency, the converter should deliver the lamp drive in the form of a sine wave to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrade overall operating efficiency. The circuit should also provide for lamp-intensity control from zero to full brightness with no hysteresis or pop-on. The LCD also requires a bias supply for contrast control. The supply's negative output should be regulated and variable over a considerable range.

The small size and battery-powered operation associated with LCD-equipped apparatus mandate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture, and long battery life is usually a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, these components, including pc board and all hardware, usually must fit within the LCD enclosure, which has a height restriction of 0.25 in.

Any discussion of CCFL power supplies must consider lamp characteristics. These lamps are difficult to drive (particularly for a switching regulator) because they have a negative resistance characteristic—the starting voltage is significantly higher than the operating voltage. Typically, the starting voltage is about 1000V and the operating voltage is about 300 to 400V. These are typical figures and they can vary for different bulbs. CCFL bulbs will operate from dc, but migration effects within the bulb will quickly damage them. Therefore, the waveform must be ac—no dc content should be present.

The negative-resistance characteristic, combined with the frequency-compensation problems associated with switching regulators, can cause severe loop instabilities, particularly on startup. Once the lamp is in its operating region, it assumes a linear load characteristic, easing stability criteria. Bulb operating frequencies are typically 20 to 100 kHz, and a sine-wave drive is preferred. The sine wave's low harmonic content minimizes RF emissions, which could cause interference and efficiency degradation.

The circuit in **Fig 1a** meets CCFL drive requirements. Circuit efficiency is 78% with an input-voltage range of 4.5 to 20V. If you can drive the LT1172 from a 3 to 5V input, 82% efficiency is possible. Additionally, lamp intensity is continuously and smoothly variable from zero to full intensity. When power is applied, the

Waveform monitoring is another consideration. The LT1172's switching frequency is completely asynchronous from the $Q_1$-$Q_2$ Royer converter's switching rate. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. To obtain waveforms like those in **Fig 1b** requires a dual-beam oscilloscope. LT1172-related waveforms (Traces A and B) are triggered on one beam, while the remaining traces are triggered on the other beam. You can also use single-beam instruments with alternate sweep and trigger switching, but they are less versatile and will only display four traces.

### Be sure of efficiency measurements

Obtaining and verifying high electrical efficiency requires some amount of diligence. The optimum efficiency values given for $C_1$ and $C_2$ are typical and will vary for specific types of lamps. $C_1$ sets the circuit's resonance point which varies, to some extent, with the lamp's characteristic. $C_2$ ballasts the lamp, effectively buffering its negative resistance characteristic. Small values of $C_2$ provide the most load isolation but require relatively large transformer output voltage for loop closure. Large $C_2$ values minimize transformer output voltage but degrade load buffering. Also, $C_1$'s best value is somewhat dependent on the type of lamp used. Typical values for $C_1$ are 0.01 to 0.047μF. $C_2$ usually ends up in the 10 to 47 pF range. $C_1$ must be a low-loss capacitor, and it would be wise to use the type listed in **Fig 1a**.

A poor-quality dielectric for $C_1$ can easily degrade efficiency by 10%. You select $C_1$ and $C_2$ by trying different values for each and iterating toward a minimum-

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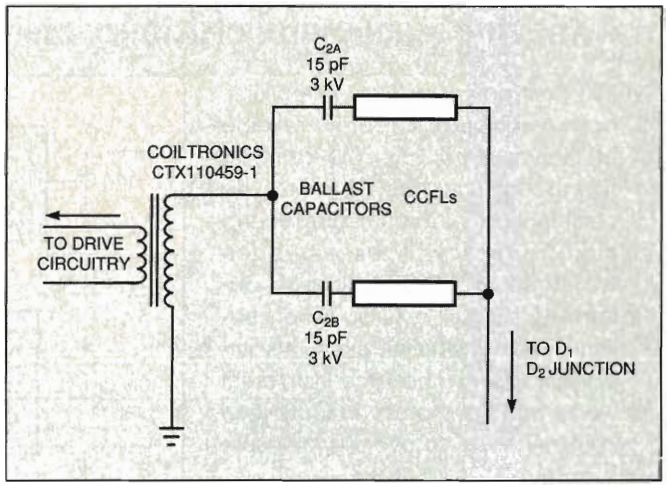



**Fig 2—The drive circuit must deliver more power when the backlighting scheme involves two CCFLs. The transformer in this circuit can develop an 11-mA output—the transformer in Fig 1a delivers only 7.5 mA.**

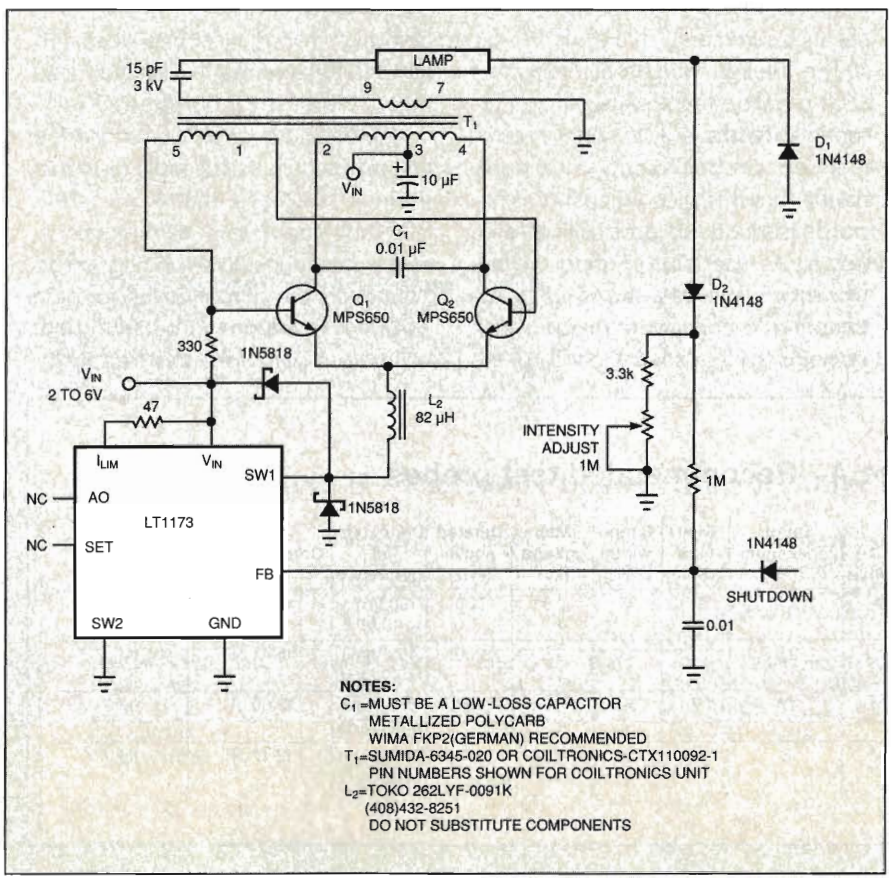



**Fig 3—Optimized for low-current operation, this drive maintains control down to tube currents of 1 mA—a very dim light. This design suits applications that need to maximize battery life. Primary supply drain ranges from hundreds of microamperes to 100 mA with tube currents of microamperes to 1 mA.**

# Achieving meaningful efficiency measurements

You must pay attention to measurement techniques to obtain reliable efficiency data for cold-cathode fluorescent-lamp (CCFL) circuits. The combination of high voltage and high-frequency harmonic-laden waveforms makes it difficult to obtain meaningful results. When selecting test instrumentation, it's important to know how the instrument works and how to use it. Only then can you hope to avoid unpleasant surprises.

Consider the case of test probes, for example. The selected probes must respond accurately under a variety of conditions. Measuring across the resistor in series with the CCFL is the most favorable circumstance because you can use a standard 1× probe to make this low-voltage, low-impedance measurement. The probe's relatively high input capacitance does not introduce significant error. You can also use a 10× probe for this measurement, but you must be sure to address frequency compensation issues.

On the other hand, the high-voltage measurement across the lamp is considerably more demanding on the probe. The waveform fundamental in this case is in the 20- to 100-kHz range, and harmonics can range into the megahertz region. This activity occurs at peak voltages in the kilovolt range.

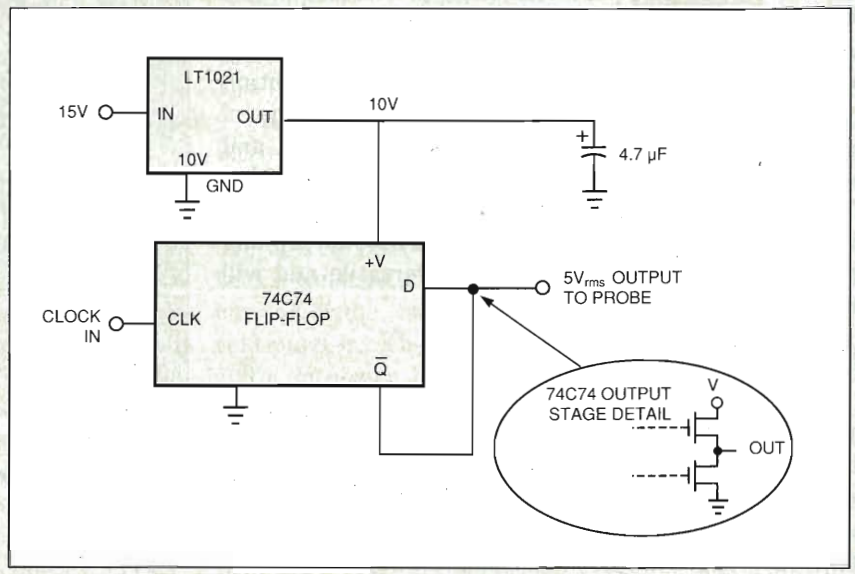



**Fig A—To generate a known rms voltage, this circuit takes advantage of a voltmeter's insensitivity to waveform shape.**

The probe must have a high-fidelity response under these conditions. Additionally, the probe should have low-input capacitance to avoid loading effects that would corrupt the measurement.

The design and construction of such a probe requires significant attention. **Table A** lists some recommended probes along with pertinent characteristics. Almost all standard oscilloscope probes will fail if you try to use them to measure the waveform across the CCFL. Attempting to circumvent probe shortcomings by resistively dividing the lamp voltage also creates problems because large-value resistors often have significant voltage coefficients and shunt capacitance that is high and unpredictable. Similarly, common high-voltage probes designed for dc measurement will have large errors because of ac effects.

The P6013A and P6015 are the preferred probes for making measurements across the CCFL; their 100-MΩ input and small capacitance introduce low-loading error. You sacrifice output level to gain 1000× attenuation, but the right voltmeters can make this tradeoff.

## Table A—Recommended test probes

| Tektronix probe type | Attenuation factor | Accuracy | Input resistance | Input capacitance (pF) | Rise time (nsec) | Bandwidth (MHz) | Max voltage (kV) | Derated above (kHz) | Derated to at frequency | Compensation range | Assumed termination resistance |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P6007 | 100x | 3% | 10M | 2.2 | 14 | 25 | 1.5 | 200 | 700 Vrms at 10 MHz | 15-55 pF | 1M |
| P6009 | 100x | 3% | 10M | 2.5 | 2.9 | 120 | 1.5 | 200 | 450 Vrms at 40 MHz | 15-47 pF | 1M |
| P6013A | 1000x | Adjustable | 100M | 3 | 7 | 50 | 12 | 100 | 800 Vrms at 20 MHz | 12-60 pF | 1M |
| P6015 | 1000x | Adjustable | 100M | 3 | 1.4 | 250 | 20 | 100 | 2000 Vrms at 20 MHz | 12-47 pF | 1M |

All of the recommended probes are designed to work into an oscilloscope input. Such inputs typically have an impedance of 1 MΩ in parallel with a capacitance of 10 to 22 pF. Appropriate voltmeters have significantly different input characteristics **(Table B)**. As a result, you must compensate oscilloscope probes to accommodate the voltmeter's input characteristics. Normally, you can readily determine and adjust the optimum compensation point by observing probe output on an oscilloscope. Using a square input of known amplitude (usually from the oscilloscope calibrator), you can adjust the probe for the correct response.

Using the probe with the voltmeter presents an unknown impedance mismatch and makes it difficult to determine when compensation is correct. The impedance mismatch occurs at low and high frequency. You can correct the low-frequency term by placing an appropriate value resistor in shunt with the probe's output. For a 10 MΩ voltmeter input, a 1.1 MΩ resistor is suitable. This resistor should be built into the smallest possible BNC-equipped enclosure to maintain a coaxial environment. Do not use any cable connections; you should locate the enclosure directly between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates for the low-frequency impedance mismatch.

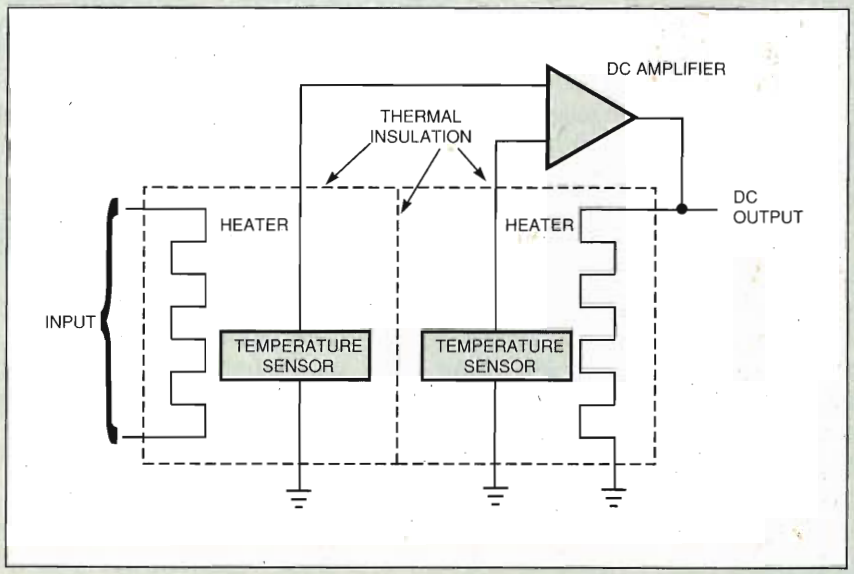



**Fig B—The conceptual thermal rms/dc converter will reject ambient temperature shifts only if the heater sensor pairs are isothermal.**

Correcting the high-frequency mismatch term is more involved. The range of voltmeter input capacitances combined with the added shunt resistor's effects presents problems. One solution is to feed a predetermined rms signal to the probe-voltmeter combination and adjust compensation for a proper reading. **Fig A** shows a simple way to generate a known rms voltage. This scheme takes advantage of the recommended voltmeter's insensitivity to waveform shape. A stable 10.00V source drives the CMOS flip-flop. The CMOS output stage, which is purely ohmic, switches error between the supply and ground rails. Clocking the flip-flop generates a square wave output with a 10.00V amplitude. The result is a known 5.00V rms output. Now, you adjust the probe's compensation for a 5.00V voltmeter reading. This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match.

*Text continued on pg 130*

## Table B—Thermally based rms voltmeter characteristics

| Manufacturer and model | Full-scale ranges | Accuracy at 1 MHz | Accuracy at 100 kHz | Input resistance and capacitance | Max bandwidth | Crest factor |
|---|---|---|---|---|---|---|
| Hewlett-Packard 3400 Meter Display | 1 mV to 300V, 12 ranges | 1% | 1% | 0.001 to 0.3V range=10M and <50 pF, 1 to 300V range=10M and <20 pF | 10 MHz | 10:1 at full scale, 100:1 at 0.1 scale |
| Hewlett-Packard 3403C Digital Display | 10 mV to 1000V, 6 ranges | 0.5% | 0.2% | 10- and 100-mV range=20M and 20 pF±10%, 1 to 1000V range=10M and 24 pF±10% | 100 MHz | 10:1 at full scale, 100:1 at 0.1 scale |
| Fluke 8920A Digital Display | 2 mV to 700V, 7 ranges | 0.7% | 0.5% | 10M and <30 pF | 20 MHz | 7:1 at full scale, 70:1 at 0.1 scale |

input supply current. You can ensure that loop closure is maintained during this procedure by monitoring the LT1172's feedback pin, which should be at 1.23V. Several trials usually produce the optimum $C_1$ and $C_2$ values. Note that the highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at $Q_1$, $Q_2$, and the output.

### Maintaining circuit efficiency

Other issues influencing efficiency include bulb-wire length and energy leakage from the bulb. The high-voltage side of the bulb should have the smallest practical lead length. Excessive length results in radiative losses, which can easily reach 3% for a 3-in. wire. Similarly, no metal should contact or be in close proximity to the bulb. This prevents energy leakage, which can exceed 10%.

Because of the high voltage at the output, pay special attention to the layout of the circuit board. You must place the output coupling capacitor carefully to minimize leakage paths on the circuit board. A slot in the board will further minimize leakage. Such leakage can permit current flow outside the feedback loop, which wastes power. In the worst case, long-term contamination buildup can increase leakage inside the loop, resulting in starved lamp drive or destructive arcing. Another technique for minimizing leakage is to evaluate and specify the silk-screen ink for its ability to withstand high voltages.

Once you follow these procedures, you can measure efficiency by calculating bulb current and voltage. To measure the current, you can measure the rms voltage across the 562Ω resistor (short the potentiometer). The bulb current is

$$I_{bulb} = 2(E/R)$$

## Achieving meaningful efficiency measurements *(continued)*

Efficiency measurements require a voltmeter with an rms response. This instrument must respond accurately at high frequency to irregular and harmonically loaded waveforms. These considerations eliminate almost all ac voltmeters, including digital voltmeters with ac ranges. There are a number of ways to measure rms ac voltage. Three of the most common include average, logarithmic, and thermal. Averaging instruments are calibrated to respond to the average value of the input waveform, which is almost always assumed to be a sine wave. Deviation from an ideal sine-wave input produces errors. Logarithmically based voltmeters attempt to overcome this limitation by continuously computing the input's true-rms value. Although these instruments are real-time analog computers, their 1% error bandwidth is well below 300 kHz and the crest-factor capability is limited. Almost all general-purpose DVMs use a logarithmically based approach and, thus, are not suited for CCFL efficiency measurements.

Thermally based rms voltmeters are direct acting thermo-electronic analog computers. They respond to the input's rms heating value. This technique is explicit, relying on the very definition of rms (the heating power of the waveform). By turning the input into heat, thermally based instruments achieve vastly higher bandwidth than other techniques. Additionally, thermal voltmeters are insensitive to waveform shape and easily accommodate large crest factors. These characteristics are necessary for the CCFL efficiency measurements.

**Fig B** shows a conceptual thermal rms-to-dc converter. The input waveform warms a heater, increasing the output from its associated temperature sensor. A dc amplifier forces a second identical heater-sensor pair to match thermal conditions of the input-driven pair. This differentially sensed feedback-enforced loop makes ambient-temperature shifts a common-mode term, eliminating their effect. Although the voltage and thermal interaction is nonlinear, the input-output rms voltage relationship is linear with unity gain. In order for this arrangement to reject ambient-temperature shifts, the heater-sensor pairs must be isothermal.

You can make the pairs isothermal by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The dc amplifier will reject this common-mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms, causing unfavorable signal-to-noise performance and limited dynamic operating range.

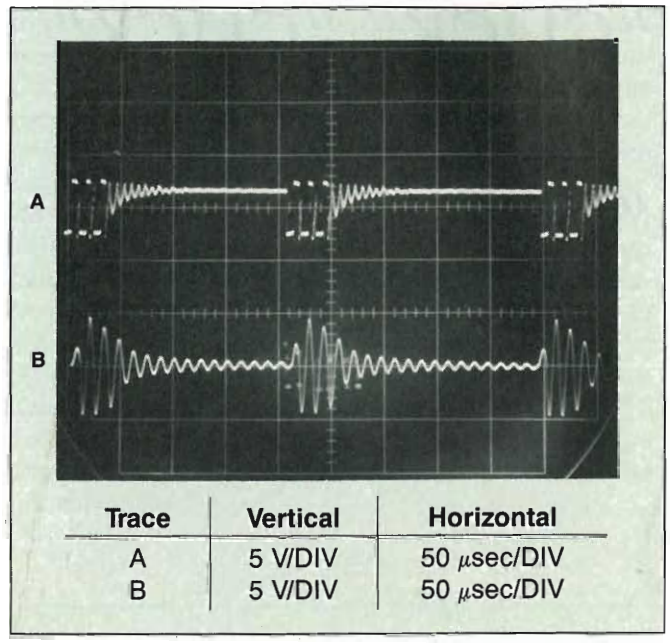
The output in **Fig B** is linear because the matched thermal pair's nonlinear voltage-temperature relationships cancel each other. The instruments listed in **Table B** are typical of what is required for meaningful results. The HP 3400A and the Fluke 8920A are currently available from their manufacturers. The HP 3403C is no longer produced but is readily available on the secondary market.

**POWER SUPPLIES**

The 2x factor is necessary because the diode steering dumps the current to ground on negative cycles. The shunting effects of the 10 kΩ-1 μF RC network across the 562Ω resistor introduce a small current-measurement error. To maximize accuracy, you can temporarily insert a 1%, 562Ω resistor in the ground lead of the negative-current steering diode and measure the voltage across it. Once this measurement is complete, you can delete this second resistor and again return the negative-current steering diode directly to ground. You can measure bulb rms voltage at the bulb with a properly compensated high-voltage probe. Multiplying these two results gives power in watts, which you can compare to the dc input supply EI product. In practice, the lamp's current and voltage contain small out-of-phase components, but their error contribution is negligible. Both the current and voltage measurements require a wideband, true-rms voltmeter. The meter must use a thermal-type rms converter—the more common logarithmically based instruments are inappropriate because their bandwidth is too low.

Some displays require two lamps instead of the more popular single-lamp approach. These 2-lamp designs usually require more power. You'll need separate ballast capacitors to accommodate two lamps (**Fig 2**), but circuit operation is similar to that for the single-lamp circuit. Higher power may require a different transformer rating. **Fig 1**'s transformer can supply 7.5 mA, although more current is possible with appropriate transformer types. For reference, the transformer in **Fig 2** has an 11-mA capability.

The **Fig 2** design reflects slightly different loading back through the transformer's primary winding. $C_2$ usually ends up in the 10- to 47-pF range. Note that $C_{2A}$ and $C_{2B}$ appear with their lamp loads in parallel




| Trace | Vertical | Horizontal |
|---|---|---|
| A | 5 V/DIV | 50 μsec/DIV |
| B | 5 V/DIV | 50 μsec/DIV |

**Fig 4—When the regulator comes on (Trace A), it delivers bursts of output current to the $L_1$,$Q_1$-$Q_2$ high-voltage converter. The converter responds with bursts of ringing at its resonant frequency.**

across the transformer's secondary winding. As such, $C_2$'s value is often smaller than in a single-lamp circuit using the same type lamp. Ideally, the transformer's secondary current splits evenly between the two capacitor lamp branches, with the total load current being regulated. In practice, differences between $C_{2A}$ and $C_{2B}$ and differences in lamp-wiring layout preclude a perfect current split. However, these differences are small and the lamps appear to emit equal amounts of light.

The design in **Fig 3** (the so-called dim backlight) is

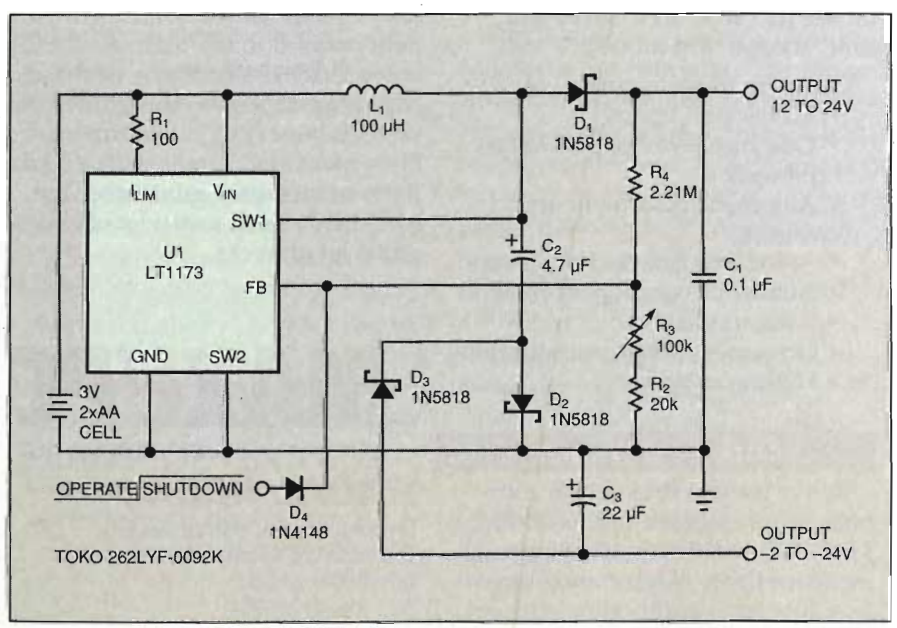



**Fig 5—To develop bias for an LCD, this generator circuit converts the 3V input to a 24V output. The circuit will deliver 7 mA from a 2V input at 75% efficiency.**

**POWER SUPPLIES**

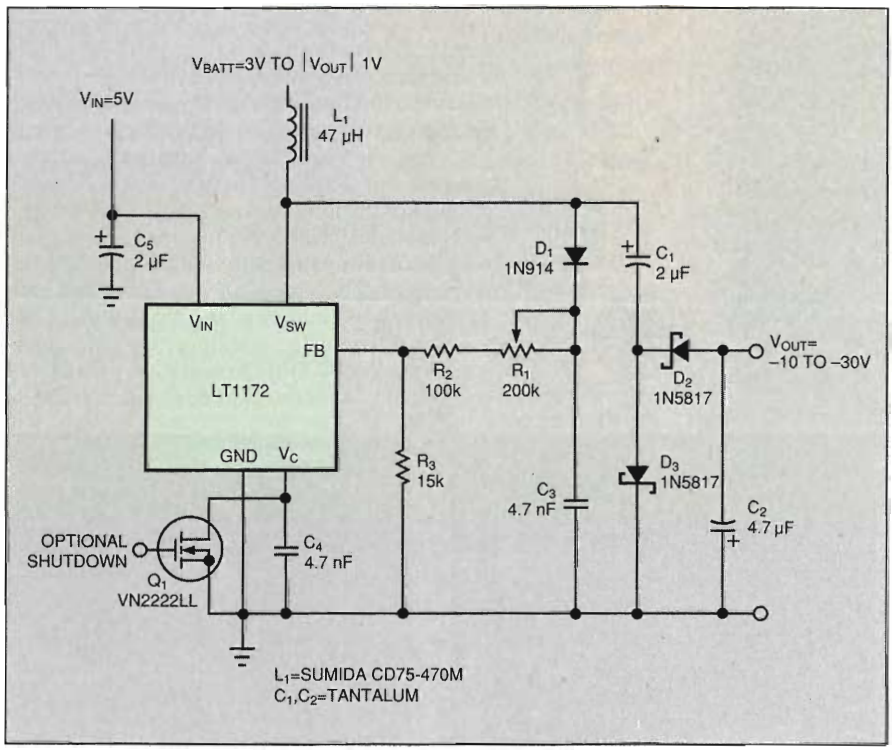



**Fig 6—To generate negative bias for LCD drivers, this circuit combines switching regulator and charge pump techniques. The variable −10 to −30V output can provide contrast control for the display.**

optimized for single-tube operation at very low currents. The circuit is designed for use at low-input voltages—typically 2 to 6V. **Fig 1a**'s circuit drives 5 mA max, but the low-power design tops out at 1 mA. The circuit in **Fig 3** maintains control down to tube currents of 1 mA—a very dim light. This design is aimed at applications looking to maximize battery life. Primary supply drain ranges from hundreds of microamperes to 100 mA with tube currents of microamperes to 1 mA. In shutdown, the circuit draws only 110 mA.

The basic design requires some modifications to maintain high efficiency at low tube currents. The operating current level in **Fig 1a**'s circuit must be lowered to achieve high efficiency. To do this, the circuit uses an LT1173 in place of the LT1172. The LT1173 is a burst-mode type regulator. When the 1173's feedback pin voltage is too low, the unit delivers a burst of output-current pulses, putting energy into the transformer and restoring the feedback point. The regulator maintains control by appropriately modulating the burst duty cycle. The ground-referred diode at the VSW pin prevents substrate turn-on due to excessive $L_2$ ring-off.

During the off periods, the regulator is essentially shut down. This type of operation limits available output power but cuts quiescent current losses. In contrast, **Fig 1a**'s LT1172 pulse-width modulator-type regulator maintains housekeeping current between cycles. This design results in more available output power, but higher quiescent currents. **Fig 4** shows operating waveforms. When the regulator comes on (Trace A), it delivers bursts of output current to the $L_1$,$Q_1$-$Q_2$ high-voltage converter. The converter responds with bursts of ringing at its resonant frequency. The circuit's loop operation is similar to that of **Fig 1a**.

### Providing bias for LCDs

LCDs also require a bias supply for contrast control. The supply's variable negative output permits adjustment of display contrast. Relatively little power is involved, which eases RF radiation and efficiency requirements. The logic sections of display drivers operate from single 5V supplies, but the actual driver outputs swing between +5V and a negative bias potential. Varying this bias causes the contrast of the display to vary.

The design in **Fig 5** is an LCD bias generator. In this circuit, $IC_1$ is an LT1173 micropower dc/dc converter. $IC_1$'s switch, $L_2$, $D_1$, and $C_1$ convert the 3V input. The switch pin (SW1) also drives a charge pump composed of $C_2$, $C_3$, $D_2$, and $D_3$ to generate 24V. Line regulation is 0.2% min with 2- to 3.3V inputs. Load regulation measures 2% with a 1- to 7-mA load. The circuit will deliver 7 mA from a 2V input at 75% efficiency.

If you need more output power, you can drive the **Fig 5** circuit from a 5V source. You have to change $R_1$ to 47Ω and $C_3$ to 47 µF. With a 5V input, the circuit

will output 40 mA at 75% efficiency. To obtain shutdown, simply bring the anode of $D_4$ to a logic high, which forces the feedback pin of $IC_1$ to go above the internal 1.25V reference voltage. Shutdown current is 110 mA from the input source and 36 mA from the shutdown signal.

**Fig 6** shows a boost converter that can provide negative bias from a 5V supply. The converter is half switcher and half charge pump. The flying node at $V_{SW}$ drives the charge pump ($C_1$, $C_2$, $D_2$, and $D_3$). The output is variable from 10 to 30V and provides contrast control for the display. On low voltage supplies (6V or less), you can tie $V_{IN}$ and $V_{BATT}$ together. To obtain higher efficiency with higher battery voltages, run the LT1172 $V_{IN}$ pin from 5V. Shutting off the 5V supply automatically turns off the LT1172. The maximum value for $V_{BATT}$ is equal to the negative output +1V. Also, the difference between $V_{BATT}$ and $V_{IN}$ must not exceed 16V. $R_1$, $R_2$, and $R_3$ have large values that minimize battery drain in shutdown because they are permanently connected to the battery via $L_1$ and $D_1$. Efficiency is about 80% at $I_{OUT}$=25 mA. EDN

## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Lab at the Massachusetts Institute of Technology. A former student at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

# 1.5 to 5V converter supplies 200 mA

**Jim Williams, Linear Technology Corp, Milpitas, CA**

Some 1.5V-powered systems, such as survival 2-way radios and remote, transducer-fed data-acquisition systems, require much more power than stand-alone IC regulators can provide. The converter in **Fig 1** supplies 200 mA at 5V from a 1.5V input.

The circuit is essentially a flyback regulator. The LT1170 ($IC_1$) switching regulator's low saturation losses and ease of use permit high-power operation and design simplicity. Unfortunately, the device has a 3V minimum supply requirement. Bootstrapping its supply pin from the 5V output is possible but requires some form of start-up mechanism. The 1.5V-powered LT1073 switching regulator ($IC_2$) provides a start-up loop. When power is applied, $IC_2$ runs and its $SW_1$ pin periodically pulls current through L1. L1 responds with high-voltage flyback events. The circuit rectifies these events, and the 470-μF capacitor stores the rectified voltage, thus producing the circuit's dc output. The output divider-string values cause $IC_2$ to turn off when the circuit output crosses approximately 4.5V.

Once $IC_2$ turns off, it obviously can no longer drive L1, but $IC_1$ can. There is some overlap between the time the start-up loop turns off and $IC_1$ turns on, but it has no detrimental effect. The start-up loop functions over a range of loads and battery voltages. Start-up currents approach 1A, so you must pay attention to $IC_2$'s saturation and drive characteristics. The worst case for the start-up loop is a nearly depleted battery and heavy output loading.

**Fig 2a** is a plot of the input and output characteristics for the circuit. Note that the circuit will start into all loads with $V_{BATTERY}$=1.2V. Start-up is possible down to 1.0V at reduced loads. Once the circuit has started, the plot shows it will drive 200-mA loads down to $V_{BATTERY}$=0.6V. **Fig 2b** shows the circuit's efficiency at two supply voltages over a range of output currents. At lower currents, the circuit's quiescent power degrades efficiency. At lower supply voltages, fixed junction-saturation losses are responsible for the lower overall efficiency. **EDN BBS /DI_SIG #1186.** EDN

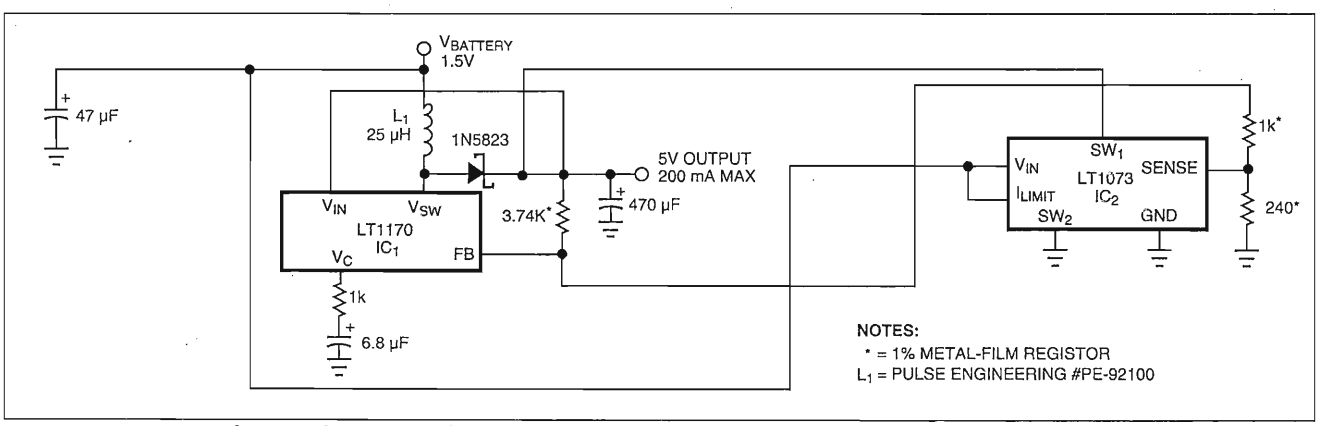



**Fig 1—Using two switching regulators—one for low-voltage start up—this converter provides 200 mA at 5V from a 1.5V source.**

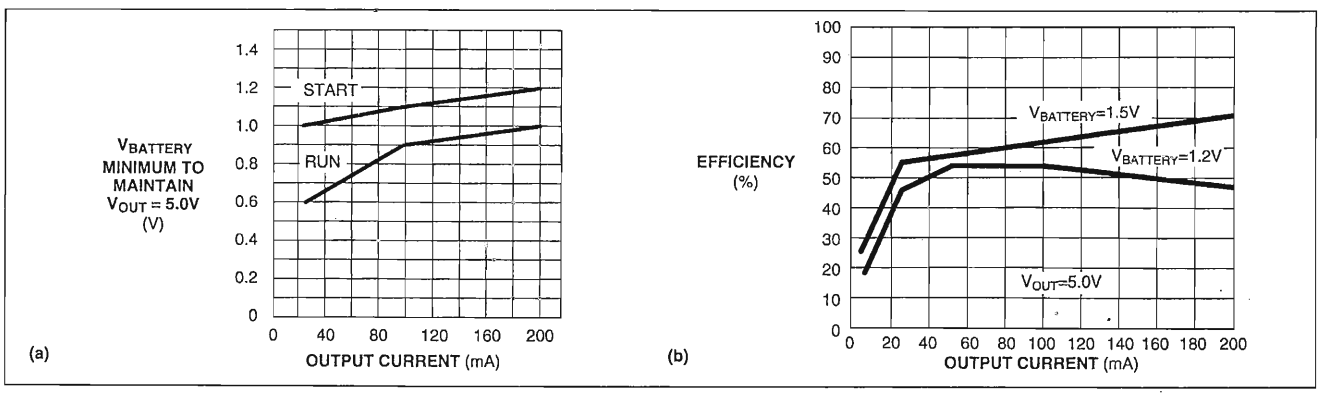



**Fig 2—Performance curves of input vs output (a) and efficiency vs output (b) show this converter's start-up voltage of 1.2V and its high efficiency at higher output currents.**

# Techniques illuminate backlit LCDs with high efficiency

Jim Williams, Linear Technology Corp

***Getting a backlight LCD lamp to turn on is just the first step in the design process. Achieving and maintaining high efficiency requires attention to both circuit-design and physical-layout details.***

A practical, 92%-efficient LCD-backlight design for cold-cathode fluorescent lamps (CCFLs) is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and its physical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing, and other items have a major effect on electrical characteristics. To achieve a practical, highly efficient LCD backlight, you must take the greatest care in every detail. Getting the lamp to light is just the beginning. (Note: The circuits and design principles that this article presents improve the efficiency of the author's initial LCD backlight design, which appeared in the October 29, 1992, issue of EDN (**Ref 1**).)

CCFLs are complex transducers, and many variables affect their ability to convert electrical current to light. Factors influencing conversion efficiency include the lamp's current, temperature, drive-waveform characteristics, length, width, gas constituents, and proximity to nearby conductors. These and other factors are interdependent, resulting in a complex overall response. **Fig 1** shows two curves of typical lamp characteristics: current (**Fig 1a**) and temperature (**Fig 1b**) vs emissivity. These curves don't correspond to any particular lamp but show general characteristics averaged over a dozen lamps from different manufacturers. These curves hint at the difficulty in predicting lamp behavior as operating conditions—including current and temperature as well as lamp voltage and length—vary.

The lamp's current and temperature are clearly critical to emission, although high electrical efficiency may not necessarily correspond to the highest optical efficiency. It is possible, for example, to construct a CCFL circuit with 94% electrical efficiency that produces less light than an approach with 80% electrical efficiency. Because of this fact, you must often perform both electrical and photometric evaluation of a circuit.

Furthermore, a lossy display enclosure or excessive high-voltage-wire lengths can severely degrade the performance of a very well matched lamp-circuit combination. Display

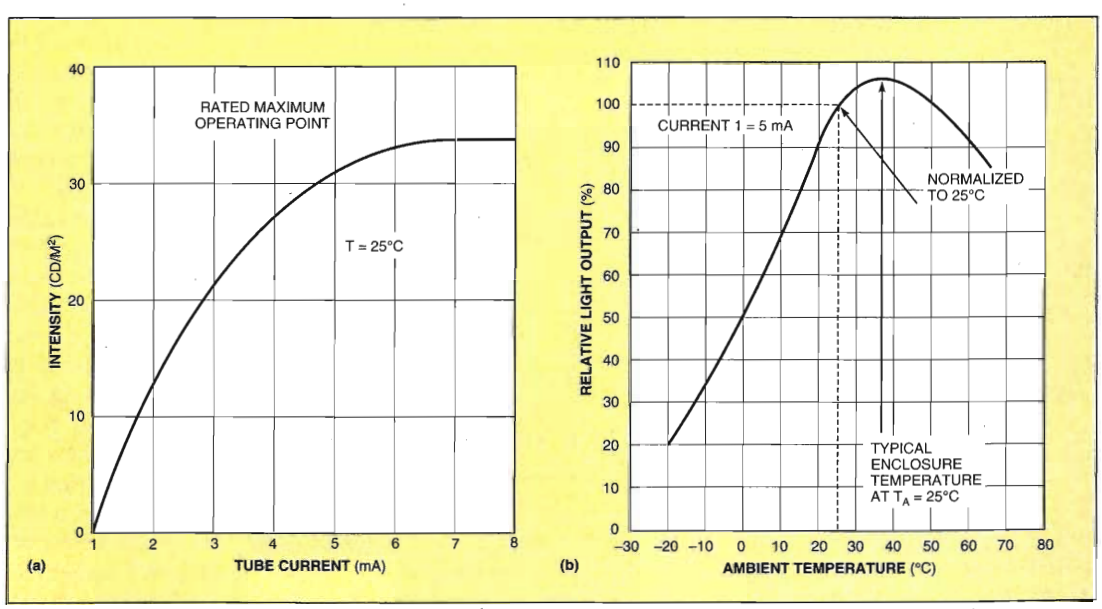



**Fig 1—A typical lamp profile of current vs intensity (a) shows a curve that flattens badly above 6 mA. Ambient temperature also has a decided effect on the lamp's emissivity (b).**

## LCD-BACKLIGHT DESIGNS

enclosures with too much conducting material near the lamp have huge losses due to capacitive coupling. A poorly designed display enclosure can easily degrade efficiency by 20%. High-voltage wire runs typically cause 1% loss/in. of wire.

Because the LCD backlight can take as much as 50% of a computer's power, any efficiency improvement is noteworthy. The circuit in **Fig 2** improves the efficiency of the original circuit (**Ref 1** and **Ref 2**) by 6 to 88%. However, if you don't have a low-voltage supply available in the display area to drive the LT1172's $V_{IN}$ pin, this efficiency figure degrades by about 3%. The efficiency improvement is primarily due to the transistor's higher gain and lower saturation voltage. You must carefully select the base-drive resistor's value—nominally 1 kΩ—to provide full $V_{CE}$ saturation without inducing base overdrive or beta starvation.

As in the original circuit, the lamp intensity is continuously and smoothly variable from zero to full intensity, and the input voltage range remains the same at 4.5 to 20V.

The details of the circuit's operation are the same as described in **Ref 1** and **Ref 2**. In essence, the circuit is a current-sink-driven resonant Royer converter (**Ref 3**). The LT1172 and $L_1$ form a switch-mode current sink. $Q_1$, $Q_2$, $T_1$, and associated components comprise the resonant Royer converter. Rectified feedback from the Royer converter's output via $D_2$ closes constant-current a loop back to the LT1172's $V_{FB}$ pin.

In addition to improving efficiency, this general circuit approach has other advantages: tight line regulation and extended dimming range. Additionally, the circuit enhances the lamp's operating life because current can't increase as the lamp ages. The circuit's 0.1% line regulation is notably better than that of some other approaches. Tight regulation prevents the lamp intensity from varying when abrupt line changes occur, which typically happens when you connect a battery-powered apparatus to an ac-powered charger. The circuit's excellent line regulation stems from the fact that $T_1$'s drive waveform never changes shape as input voltage varies. This characteristic permits the simple 10-kΩ to 1-μF RC network to produce a consistent response. The RC averaging characteristic has serious error compared to a true rms conversion, but the error is constant and the 562Ω shunt's value calibrates out the error.

The circuit in **Fig 3** is similar to the one in **Fig 2** but uses a transformer with lower copper and core losses to increase efficiency to 92%. The tradeoff is slightly larger transformer size. Value shifts in $C_1$, $L_1$, and the base-drive resistor reflect different transformer characteristics. This circuit also features a dc or pulse-width-controlled dimming input and shutdown via $Q_3$.

Keep several points in mind when observing the operation of these circuits. Only a wideband, high-voltage probe that's fully specified for this type of measurement can monitor $T_1$'s high-voltage secondary. Most scope probes break down and fail to make this measurement (**Ref 4**). To read $T_1$'s output, Tektronix probes types P-6007 and P-6009 are acceptable in some cases, but types P-6013A and P6015 are preferable.

Obtaining and verifying high efficiency takes diligence. The values in **Fig 2** and **Fig 3** for $C_1$ and $C_2$ are typical for achieving high efficiency and vary for specific types of lamps. An important realization is that the term "lamp" includes the *total* load seen by the transformer's secondary. This load, reflected back to the primary, sets the transformer's input impedance. The transformer's input impedance forms an integral part of the LC tank circuit that produces the high-voltage drive. Thus, you must optimize circuit efficiency by arranging the wiring, display housing, and physical layout *exactly* the same way they will be built in production. Deviations from this procedure result in lower efficiency than otherwise possible.

In practice, a first-cut efficiency optimization with best-guess lead lengths and the intended lamp in its display housing usually produces results within 5% of the achievable figure. When the production circuit's physical layout is set, you can fix the values for $C_1$

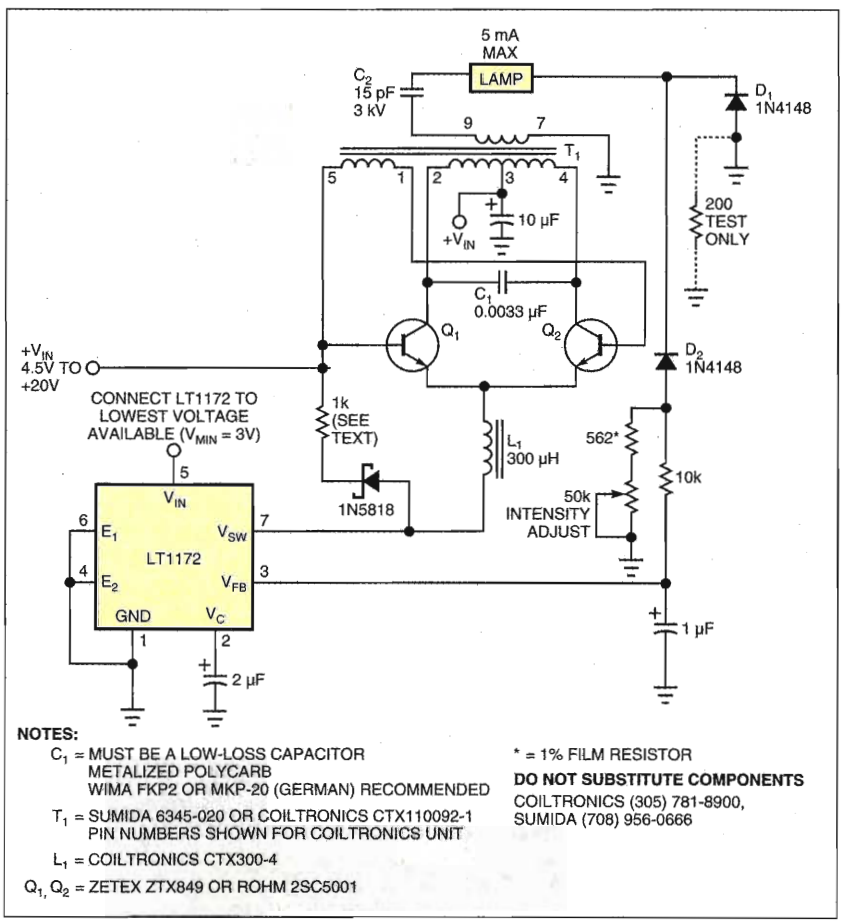



**Fig 2—This current-sink-driven resonant Royer converter powers a cold-cathode fluorescent lamp with 88% efficiency. The circuit's added benefits are 0.1% line regulation and a wide dimming range.**

and $C_2$. $C_1$ sets the circuit's resonance point, which varies to some extent with the lamp's characteristics. $C_2$ ballasts the lamp, effectively buffering its negative-resistance characteristic. Small values of $C_2$ provide the most load isolation but require relatively large transformer output voltage for loop closure. Large $C_2$ values minimize transformer output voltage but degrade load buffering.

**Components' values depend on the lamp**

The best values for $C_1$ and $C_2$ depend on the specific lamp you use. Some interaction occurs between the two capacitors, but generalized selection guidelines are possible. Typical values for $C_1$ are 0.01 to 0.15 µF. $C_2$ usually ends up in the 10- to 47-pF range. $C_1$ must be a low-loss capacitor; substituting a poor-quality dielectric for $C_1$ can easily degrade efficiency by 10%.

Before selecting a capacitor, set the value of the $Q_1$ to $Q_2$ base-drive resistor to a value, such as 470Ω, which ensures saturation. Next, select $C_1$ and $C_2$ by trying different values for each and iterating toward best efficiency. During this procedure, monitor $IC_1$'s feedback pin, which should be at 1.23V, to ensure that the loop is closed. Several trials usually produce the optimum $C_1$ and $C_2$ values. The highest efficiencies are not necessarily associated with the most esthetically pleasing waveshapes, particularly at $Q_1$, $Q_2$, and the output.

Now you should optimize the base-drive resistor's value. This resistor's value, which is nominally 1 kΩ, should provide full $V_{CE}$ saturation without inducing base overdrive or beta starvation. Using full lamp power, the point at which the collector current peaks determines the optimum value. The resistor should equal the largest value that ensures saturation for worst-case transistor beta. You can verify this condition by varying the resistor about the ideal value and noting the small variations in input supply current. The minimum obtainable current corresponds to the best beta-vs-saturation tradeoff. In practice, supply current rises slightly on either side of this point. This double-value behavior is due to excessive base-drive or saturation losses, which degrade efficiency.

Other issues influencing efficiency include the lamp's wire length and energy leakage. The high-voltage side of the lamp should have the smallest practical lead length. Excessive length results in radiative losses, which can easily reach 3% for a 3-in. wire. Similarly, to prevent energy leakage, which can degrade efficiency by 10%, metal should neither contact nor be close to the lamp.

Finally, a custom-designed lamp affords the best possible results. A jointly tailored lamp-circuit combination permits precise optimization of circuit operation to yield the highest efficiency. EDN

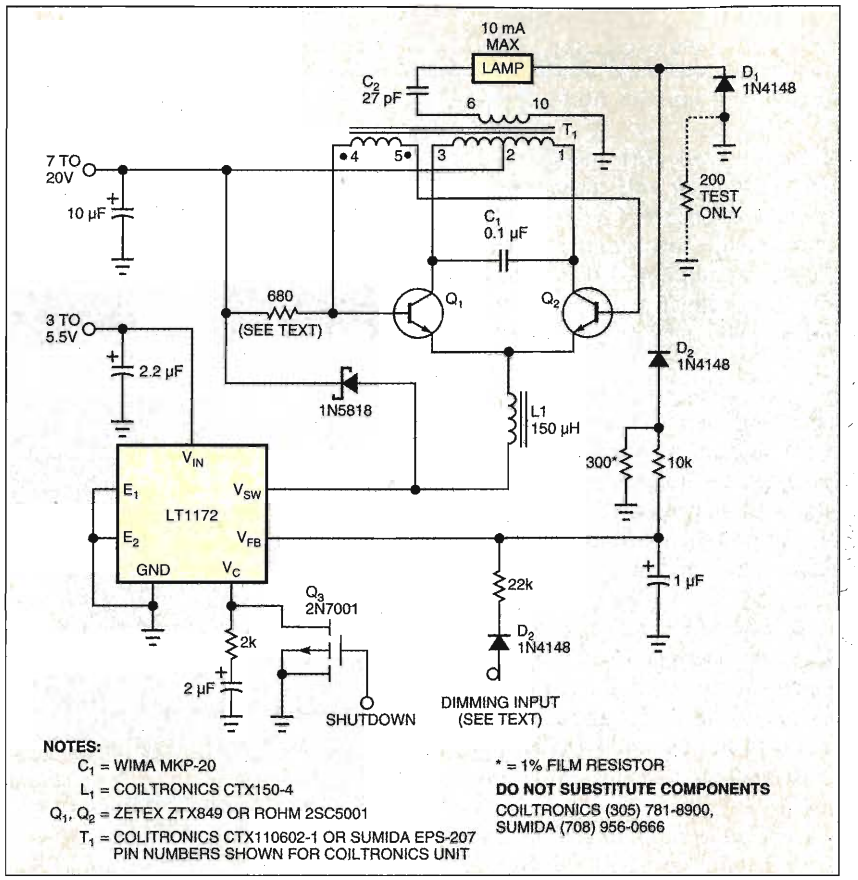



**Fig 3—Using a larger transformer that has lower copper and core losses, this cold-cathode fluorescent-lamp supply features 92% efficiency and adds shutdown- and dimming-control inputs.**

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## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Lab at the Massachusetts Institute of Technology. A former student at Wayne State University (Detroit, MI), Jim enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

# Synchronized regulator produces coherent noise

Jim Williams, Sean Gold, and Steve Pietkiewicz, Linear Technology, Milpitas, CA

By using a gated-oscillator architecture instead of a clocked-PWM one, gated-oscillator-type switching regulators permit high efficiency over extended ranges of output current. This architecture eliminates the housekeeping currents associated with the continuous operation of fixed-frequency designs. Gated-oscillator regulators simply self-clock at whatever frequency is necessary to maintain the output voltage. Typically, loop-oscillation frequency ranges from a few hertz to the kilohertz region, depending on the load.

In most cases, this asynchronous, variable-frequency operation doesn't create any problems. However, some systems are sensitive to the asynchronous characteristics. The system in **Fig 1** slightly modifies a gate-oscillator-type switching regulator by synchronizing its loop-oscillation frequency to the system's clock. The oscillation frequency and its attendant switching noise, albeit variable, become coherent with system operation.

To analyze the system in **Fig 1**, temporarily ignore the flip-flop, and assume the circuit directly connects the $A_{OUT}$ and FB pin of the LT1107 regulator. When the output voltage decays, the set pin drops below $V_{REF}$, causing $A_{OUT}$ to fall. The internal comparator then switches to high, biasing the oscillator and output transistor into conduction. $L_1$ receives drive pulses, and the circuit deposits this inductor's flyback events into the 100-µF capacitor via the diode, ultimately restoring output voltage. This action overdrives the set pin, causing the IC to switch off until it requires another cycle. This oscillator cycle's frequency is load-dependent and variable.

Now, interposing a flip-flop into the path between the $A_{OUT}$ and FB pins, as the **figure** shows, synchronizes the regulator to the circuit-generated clock. When the output decays far enough, the $A_{OUT}$ pin goes low. At the next clock pulse, the flip-flop's $Q_2$ output sets low, biasing the comparator-oscillator. This turns on the power switch, which pulses $L_1$. $L_1$ responds in flyback fashion and deposits its energy into the output capacitor to maintain output voltage. This operation is similar to the previously described case, except that the flip-flop now synchronizes the sequence of events with the system clock. Although the resulting loop's oscillation frequency is variable, the frequency and all attendant switching noise is synchronous and coherent with the system clock.

The circuit requires a start-up sequence because the output provides power for the clock. The circuit connects the flip-flop's remaining section as a buffer to furnish start-up. The flip-flop's connected $CLR_1$ and $CLK_1$ lines monitors output voltage via the 221-, 82.5-, and 100-kΩ resistor string. When power is applied, $Q_1$ sets $CLR_2$ low, which permits the LT1107 to switch, thereby raising the output voltage. When the output goes high enough, $Q_1$ sets $CLR_2$ high, and normal loop operation commences. Although this circuit uses a step-up regulator, the technique also works with other types.

**EDN BBS /DI_SIG #1383**

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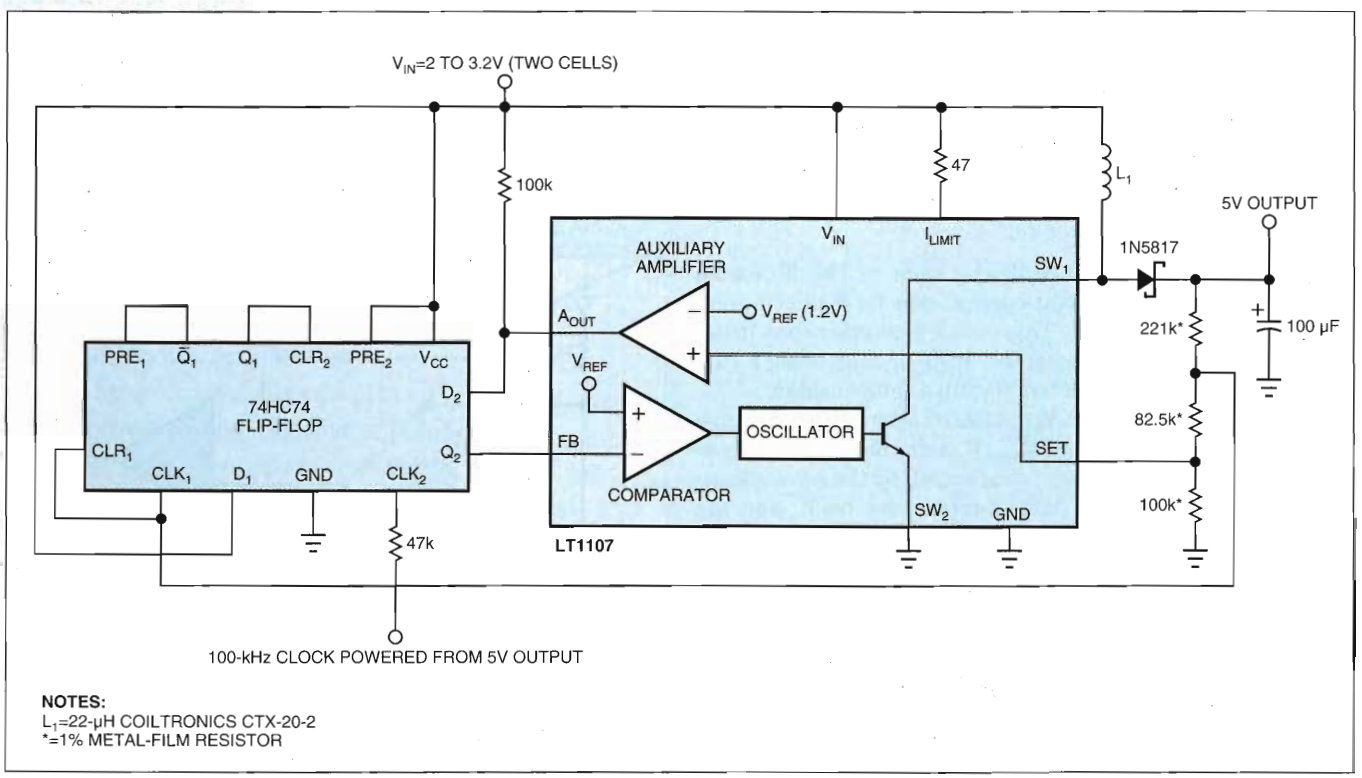



**Fig 1—A synchronizing flip-flop forces the LT1107 gate-oscillator-type switching regulator's noise to be coherent with the 100-kHz clock.**

# Pulse generator verifies test setups

Jim Williams, Linear Technology Corp, Milpitas, CA

Verifying the rise-time limit of wideband test-equipment setups is a difficult task. In particular, you must often know the "end-to-end" rise time of an oscilloscope/probe combination to ensure measurement integrity. **Fig 1**'s circuit provides an 800-psec pulse having rise and fall times shorter than 250 psec. The pulse's amplitude is 10V, and the circuit's source impedance is 50Ω. The circuit is similar to the one **Ref 1** details, except that this circuit is triggerable instead of free-running. This triggering feature permits synchronizing with a clock or another event. You can vary the delay of the output with respect to the trigger by 200 psec to 5 nsec.

The circuit requires a high-voltage bias for operation. A cascoded high-voltage transistor, $Q_2$, combines with a switching regulator $IC_1$ to form a high-voltage, switched-mode supply. $IC_1$ pulse-width-modulates $Q_2$ at a 100-kHz clock rate. $L_1$'s inductive events get rectified and stored in the 2-μF output capacitor. The adjustable resistor divider provides feedback to $IC_1$. The diode and RC combination at $Q_2$'s base damp inductor-related parasitic behavior. The 10-kΩ/1-μF pair filters noise from the supply line.

The $R_3/C_1$ combination applies high voltage to $Q_1$, a 40V-breakdown device. Set the high-voltage "bias-adjust" control at the point where free-running pulses across $R_4$ *just* disappear. This setting puts $Q_1$ slightly below its avalanche point.

Subsequently, applying an input trigger pulse causes $Q_1$ to avalanche. The result is a quickly rising, very fast pulse across $R_4$. $C_1$ discharges, $Q_1$'s collector voltage falls, and breakdown ceases. $C_1$ then recharges to just below the avalanche point. At the next trigger pulse, this sequence repeats.

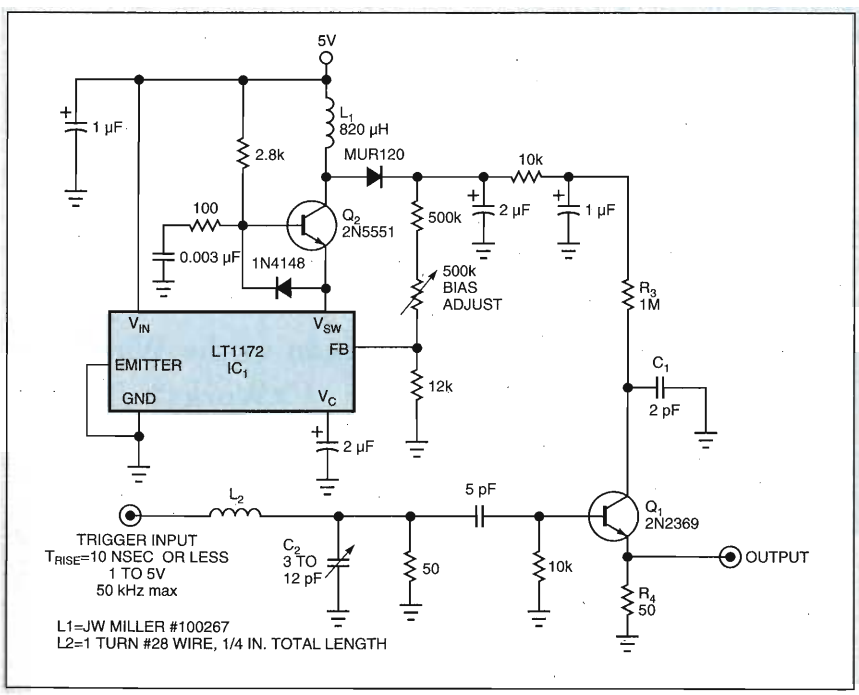



**Fig 1—A trigger pulses causes the carefully biased $Q_1$ to avalanche, producing a fast, short 10V pulse suitable for verifying instrument setups.**

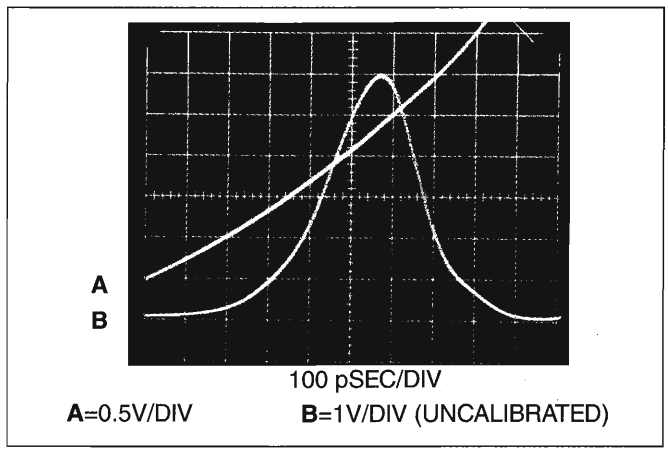



**Fig 2—The input trigger pulse to the circuit in Fig 1 appears as Trace A. A 3.9-GHz Tektronix 661 sampling oscilloscope with 4S2 sampling plug-in measured the pulse, Trace B, as having a 10V amplitude and an 800-psec duration. Rise time is 250 psec, with fall time indicated as 200 psec. The times are probably slightly faster, because the oscilloscope's 90-psec rise time influences the measurement.**

**Fig 2** shows the circuit's waveforms. The input trigger pulse is Trace A. Its amplitude provides a convenient way to vary the delay time between the trigger and output pulses. A 1 to 5V setting range produces a continuous 5-nsec to 200-psec delay range.

The circuit requires some special considerations for optimal performance. $L_2$'s very small inductance combines with $C_2$ to slightly retard the trigger pulse's rise time. This retardation prevents significant trigger-pulse artifacts from appearing at the circuit's output. You should select $C_2$ for the best compromise between output-pulse rise time and waveform purity. You may also have to select $Q_1$ to get the desired avalanche behavior. Such behavior, while characteristic of the device, is not guaranteed.

A sample of 50 Motorola 2N2369s, spread over a 12-year date-code span, yielded 82% usable devices. All "good" devices switched in less than 600 psec. Select $C_1$ for a 10V output amplitude. $C_1$ is typically between 2 and 4 pF. Ground-plane construction with high-speed layout, connection, and termination techniques are essential for good results from this circuit. (DI #1427) EDN

## Reference

1. Williams, Jim, "Measurement and Control Circuit Collection," App Note 45, Linear Technology Corp, 1991, pg 18.

**To Vote For This Design, Circle No. 428**

# Try *fixing it* yourself

JIM WILLIAMS, LINEAR TECHNOLOGY CORP

**Drag out some of that obsolete electronic equipment collecting dust in storage. Your next cutting-edge innovation may come from tinkering with a relic of the past.**

Fall of 1968 found me at the Massachusetts Institute of Technology (MIT), preparing courses, negotiating students' theses topics, and assembling a laboratory. My activities were fairly unremarkable behavior for the locale, but, for a 20-year-old college dropout, the circumstances were charged: This was my one shot at any sort of career. For reasons I'll never understand, my entire education, from kindergarten through college, had been a nightmare, perhaps the greatest impedance mismatch in history. When I got hot, the Detroit Board of Education didn't. Leaving Wayne State University after a dismal year and a half seemed to close the casket on my circuit-design dreams.

All this history conspired to provide me with an unusual outlook, a mix of terror and excitement. But mostly terror. Here I was, back in school, but on the other side of the lectern. Worse yet, my research project, although of my own choosing, seemed open-ended and unattainable. I was scared to death. The capper of this scenario was my social situation: I was younger than some of my students, and my colleagues had at least 10 years over me.

The architect of my unique opportunity was Jerrold R Zacharias, eminent physicist, Manhattan Project and Radiation Lab alumnus, and father of atomic time. Zacharias had waved the magic wand to get me an MIT appointment, a lab, and operating money. He also made it clear that he expected results. He was not the sort to tolerate looking foolish, and, in my mind, to fail him promised a far worse fate than dropping out of school.

Against this backdrop, I received my laboratory-budget request back from review. Zacharias permitted me untrammeled freedom. Everything I requested, even very costly items, had been approved without comment or question. He included just one restriction: no allocation

Daniel Guidera

## *FIX IT* YOURSELF!

for instrument repair and calibration. His handwritten comment read, "You fix everything."

It didn't make sense. Under pressure for results, scared to pieces, I was supposed to waste time by screwing around fixing lab equipment? I went to see Zacharias. I negotiated. I pleaded. I ranted. But I lost. The last thing I heard chasing me out of his office was, "You fix everything."

I soon cooled off, and the issue became irrelevant because nothing broke. At least for a while. Finally, a high-sensitivity, differential-scope plug-in, a Tektronix 1A7, died. Life would never be the same.

### Stealing isn't always a sin

The problem wasn't particularly difficult to find, once I took the time to understand how the thing worked. The manual's level of detail and writing tone were notable; communication was the priority. This seemed a significant deviation from most academic publications, and I was impressed. The instrument more than justified the manual's efforts. It was gorgeous. The integration of mechanicals, layout, and electronics was like nothing I had ever seen. Hours after I fixed the thing, I continued to probe and puzzle through its subtleties. A common-mode bootstrap scheme was particularly interesting; it had direct applicability to my lab work. I resolved to steal the techniques for reducing input current and noise.

Over the next month, I found myself continually drifting away from my research project to take apart test equipment and see how it worked. The practice, alone, was interesting, but what I really wanted was to test my understanding of a piece of equipment by having to fix it. Unfortunately, Fluke, Hewlett-Packard, Tektronix, and the rest of that ilk had done their work well; the stuff didn't break.

I offered free repair services to other labs that would bring me instruments to fix. I had few takers. People had repair budgets and were unwilling to risk their equipment to my unproven care. Finally, in desperation, I paid people, in standard MIT currency (Coke and pizza), to deliberately disable my test equipment so I could fix it.

A few of my students became similarly hooked, and we engaged in all forms of contesting. After a while, the "breakers" developed an armada of incredibly arcane diseases to visit on unsuspecting working instruments. The "fixers" countered with ever more sophisticated analysis capabilities. Various games we created took points off for every test connection made to an instrument's innards, the emphasis being on how close you could get utilizing panel controls and connectors. Fixing without a schematic was highly regarded—a macho test of analytical skill and circuit sense. Still other versions rewarded pure speed of repair, regardless of method. It was great fun. It was also a form of efficient—and serious—education.

The inside of a broken, but well-designed, piece of test equipment is an extraordinarily effective classroom. The age or purpose of the instrument is of minor concern. Its instructive value derives from several perspectives.

It is always worthwhile to look at how a designer dealt with problems using available technology—and within the constraints of cost, size, power, and other realities. Whether the instrument is three months young or 30 years old has no bearing on the quality of thought behind it. Good design is independent of technology, essentially timeless. The clever, elegant, and often interdisciplinary approaches found in many instruments are eye-opening, often directly applicable to your current design work. More important, they force self-examination and, with some luck, prevent rote approaches to problem solving (and the attendant mediocre results). The specific circuit tricks you find are certainly useful and adaptable but not nearly as valuable as studying the thought processes that produced them.

The fact that the instrument is broken provides a unique opportunity; a broken instrument (or whatever is at hand) is a capsulized mystery, a puzzle with a definite and very singular "right" answer. As a result, you are forced to measure your performance against an absolute, nonnegotiable standard. When you're finished, the thing either works or doesn't work.

The reason this scenario is so valuable is that it brutally tests your thinking process. Fast judgments, glitzy explanations, and specious, hand-waving arguments cannot be costumed as "creative" activity or true understanding of a problem. After each ego-inspired lunge or jumped conclusion, you confront the uncompromising reality that the damn thing still doesn't work. The utter closedness of this reality prevents you from fooling yourself. When it's finally over, when the box works—and you know why—then the real work begins. You get to try to fix *yourself*. Poor technique, crummy arguments, and inaccurate conclusions all demand review. It's a humbling and sometimes embarrassing process, but valuable nonetheless. You learn to dance with problems instead of trying to mug them.

### No room for sloppiness

It's scary to wonder how much of this sort of sloppy thinking slips into your own design work. In that arena, the system is not closed. There is no arbitrarily right answer, only choices. Things can work, but not as well as they might if your thinking had been better. In the worst case, things work but for different reasons than you count on. This situation is a disaster and more common than might be supposed.

For me, the most dangerous point in design comes when it works. Ostensibly, this "proves" my thinking correct, which isn't necessarily the case. The luxury the broken instrument's closed intellectual system provides no longer exists. In design work, results are open to interpretation and explanation, which is a dangerous time. When a design "works" is a very delicate stage; psychologically, you are ready for the kill and, consequently, less inclined to continue testing your results and thinking. That's a precarious place to be, and you have to be careful not to get into trouble. The very humanness that drives you to solve a problem can betray you near the finish line.

## *FIX IT* YOURSELF!

What all this means is that fixing things is excellent exercise for doing design work, a sort of bicycle-with-training-wheels that prevents you from getting into too much trouble. In design work, you have to mix your willingness to try anything with what you hope is critical thinking. This seemingly immiscible combination can lead you to a lot of nowheres, but it can also force you to learn, which is the major reason I've been addicted to fixing since that semester back in 1968. I'm fairly sure it was Zacharias' reason for bouncing my instrument-repair allocation. I couldn't understand it then, but he had initiated me. He introduced me to what my life would become for the next 10 years. And no apprenticeship was ever more necessary, better delivered, or, years later, as appreciated.

There are, of course, less lofty adjunct benefits to fixing. You can often buy broken equipment at absurdly low cost. I once paid $10 for a dead Tektronix 454A 150-MHz portable oscilloscope. It had been systematically sabotaged by some weekend-bound calibration technician and tagged "beyond repair." The machine required 30 hours to uncover the various nasty tricks played within its bowels to ensure that it would be scrapped.

This kind of devotion highlights another benefit of fixing. There is a certain satisfaction, a kind of service to a "moral" imperative, that comes from restoring a high-quality instrument. Sure, I'll admit that this is unquestionably a gooey, hand-over-the-heart judgment, and I confess a long-term love affair with instrumentation. But, for me, it seems sacrilegious to let a good piece of equipment die.

And, finally, fixing is simply a lot of fun. I'm probably the only person at an electronic flea market who pays more for the busted stuff than for the equipment that works!

Oh boy, it's broken! Life doesn't get any better than this. EDN

▶ This article is part of Jim Williams' new book, *Another Look at Analog Circuit Design*. It will be published this spring by Butterworth-Heinemann as part of the *EDN* Series for Design Engineers. Contact (800) 366-2655 to order.

## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He was voted EDN's 1992 Innovator of the Year. Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

# Tripping the light fantastic: a case study in circuit design

JIM WILLIAMS, LINEAR TECHNOLOGY CORP

Where do good circuits come from? Do they arrive as lightning bolts in the minds of a privileged few? Are they products of synthesis or derivation based on careful analysis—or do they simply evolve? Where do skill, experience, and luck fit into the equation? I cannot answer all of these weighty questions, but I can recount how the best circuit I ever designed came to be.

**Good circuit design involves a mixture of imagination, experimentation, and a willingness to borrow from the lore of innovators who preceded us.**

Deciding what makes a good circuit is a fairly difficult task, but I can suggest a few guidelines. Its appearance should be fundamentally simple, although it may embody complex and powerful theoretical elements and interactions. For me, that combination is the essence of elegance. The circuit should also find wide use. An important measure of a circuit's value is if lots of people use it and are satisfied with their decision afterward. Finally, the circuit should also generate substantial revenue. My employer is faithful about paying me, so I should hold up my end of the bargain, too. Those are a few general guidelines. Now for the circuit story.

## The postpartum blues

Toward the end of 1991, I was in a rut. In August, I finished a large high-speed-amplifier project, which had required a year of constant, intense, and sometimes ferocious effort, right up to its conclusion. Then it was over. I suddenly had nothing to do. The strange feeling of being abruptly disconnected from an absorbing task had hit me before, and the result was always the same. I go into this funky kind of rut, and I wonder if I'll ever find anything else interesting to do. I also begin to question if I'm even *capable* of doing anything anymore.

I've known myself a long time, so this state of mind doesn't promote quite the panic and urgency it used to. The treatment is always the same. Keep busy with mundane chores at work, read a bit, cruise electronic junk stores, fix things, and, in general, look available so that some interesting problem might ask me to dance. During this time, I take care of the stuff I completely let go while I was immersed in whatever problem owned me. The treatment always seems to work; it usually takes a period of months. In this case it took exactly three.

This article is part of a new book by Jim Williams. *The Art of Analog Circuit Design* will be published this spring by Butterworth-Heinemann as part of the *EDN* Series for Design Engineers. Phone (800) 366-2665 to order.

## What's a backlight?

At Christmas time, my boss, Bob Dobkin, asked me if I ever thought about the liquid-crystal-display (LCD) backlights used in portable computers. I had to admit I didn't know what a backlight was. He explained that LCDs require an illumination source to make the display readable, and that this source consumes about half the power in the machine. In addition, the light source, a form of fluorescent lamp, requires high-voltage, high-frequency ac drive. Bob was wondering how this was done, with what efficiency, and if we could devise a better way—and then market it.

The idea sounded remotely interesting. I enjoy transducer work, and that's what a light bulb is. I thought it might be useful to get my hands on some computers and take a look at the backlights. Then I went off to return some phone calls, attend

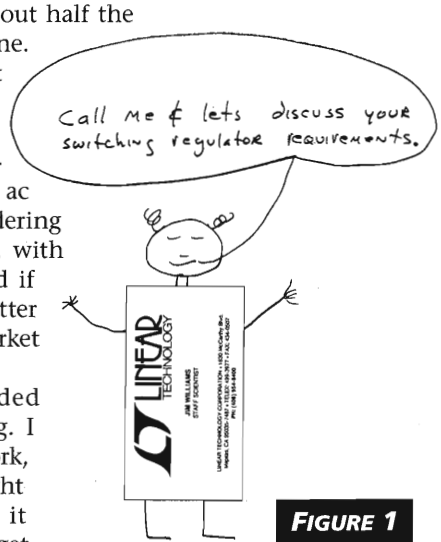



**FIGURE 1**

**This doodle, circa 1989, was instrumental in getting the collaboration on the backlight project started with Apple Computer.**

to housekeeping chores, and basically maintain my funk.

Three days later, the phone rang. A guy named Steve Young from Apple Computer had seen a cartoon (**Fig 1**) I'd stuck on the back page of an application note back in 1989. Steve outlined several classes of switching-power-supply problems he was interested in. His application was portable computers, and a more efficient backlight circuit was a priority. Bob Dobkin's interest in backlights suddenly sounded a lot less academic.

The guy on the phone seemed like a fairly senior type, and Apple was obviously a prominent computer company. Also, he was enthusiastic, seemed easy to work with, and quite knowledgeable. This potential customer also knew what he wanted and was willing to invest a lot of front-end thinking and time to achieve it. It was clear Young wasn't interested in a quick fix; he wanted true, "end-to-end," system-oriented solutions.

What a customer! He knew what he wanted, was open and eager to work, had time and money, and was willing to sweat to find better solutions. On top of all that, Apple had excellent engineering resources. I set up a meeting to introduce him to Dobkin.

The meeting went well. I took the backlight problem. I still wasn't enthralled with backlights, but Young was an almost ideal customer, so I really had no choice.

Steve Young introduced me to Paul Donovan, my primary contact. Donovan outlined the ideal backlight. It should have the highest possible efficiency—that is, the highest possible display luminosity with the lowest possible battery drain. Lamp intensity should be smoothly and continuously variable over a wide range with no hysteresis or "pop-on" and should not be susceptible to supply-voltage changes. RF emissions should meet FCC and system requirements. Finally, parts count and board space should be minimal. The board-height limit was 0.25 in.

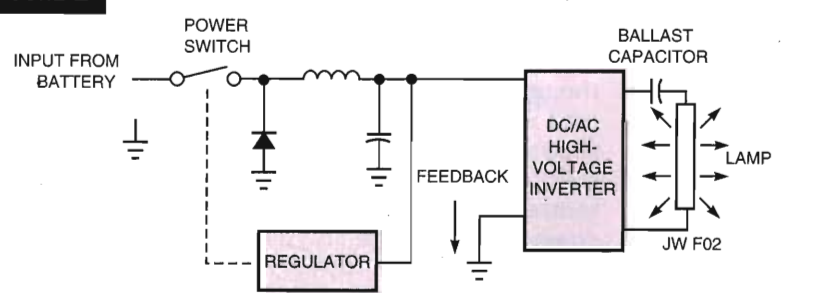
### Learning, Luddite-style

I began by getting a bunch of portable computers and taking them apart. I must admit that the Luddite in me enjoyed throwing away most of the computers while saving only their display sections. I immediately noticed that almost all of them used a purchased, board-level solution to backlight driving. Almost no computer maker actually built the function. The circuits invariably took the form of an adjustable-output, step-down switching regulator driving a high-voltage dc/ac inverter (**Fig 2**). The ac high-voltage output often ran at about 50 kHz and was approximately sinusodial.

The circuits seemed to operate on the assumption that a constant-voltage input to the dc/ac inverter would produce a fixed, high-voltage output. This fixed output would, in turn, produce constant light emission from the lamp. The ballast capacitor's function was not entirely clear, but I suspected it was related to lamp characteristics. There was no form of feedback from the lamp to the drive circuitry.

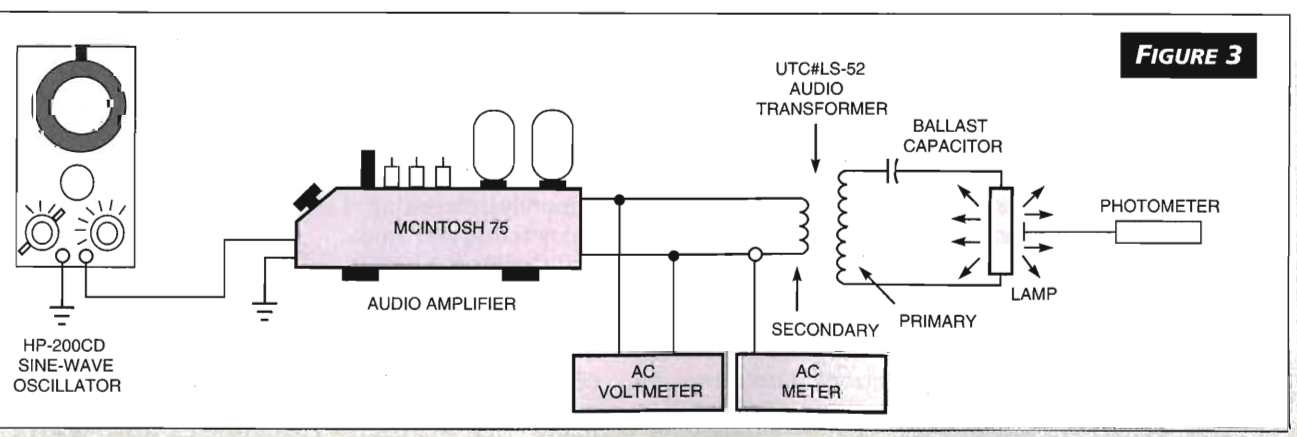
Was there something magic about the 50-kHz frequency? To see, I built up a variable-frequency, high-voltage generator (**Fig 3**) and drove the displays. I varied frequency while comparing electrical drive power to optical emission. Lamp conversion efficiency seemed independent of frequency over a fairly wide range. I did notice, however, that higher frequencies tended to introduce

**FIGURE 2**




**This configuration is most popular for driving backlights in portable computers. The circuit incorporates no feedback from the lamp.**

**FIGURE 3**




**A hi-fi amplifier helped to prove that lamp efficiency is relatively independent of drive frequency, but wiring parasitics can lead to losses at high frequencies.**

losses in the wiring running to the lamp. These losses occurred at all frequencies but became pronounced above approximately 100 kHz or so. Deliberately introducing parasitic capacitances from the wiring or lamp to ground substantially increased the losses. The lesson was clear. The lamp wiring was an inherent and parasitic part of the circuit, and any stray capacitive path was similarly parasitic.

Armed with this information, I returned to the computer displays. I modified things to minimize the wire length between the inverter board and display. I also removed the metal display housing in the lamp area. The result was a measurable decrease in inverter drive power for a given display intensity. In two machines, the improvement approached 20%! My modifications weren't very practical from the mechanical-integrity viewpoint, but that wasn't relevant. I wondered why these computers hadn't been originally designed to take advantage of this "free" efficiency gain.

### Playing with light bulbs

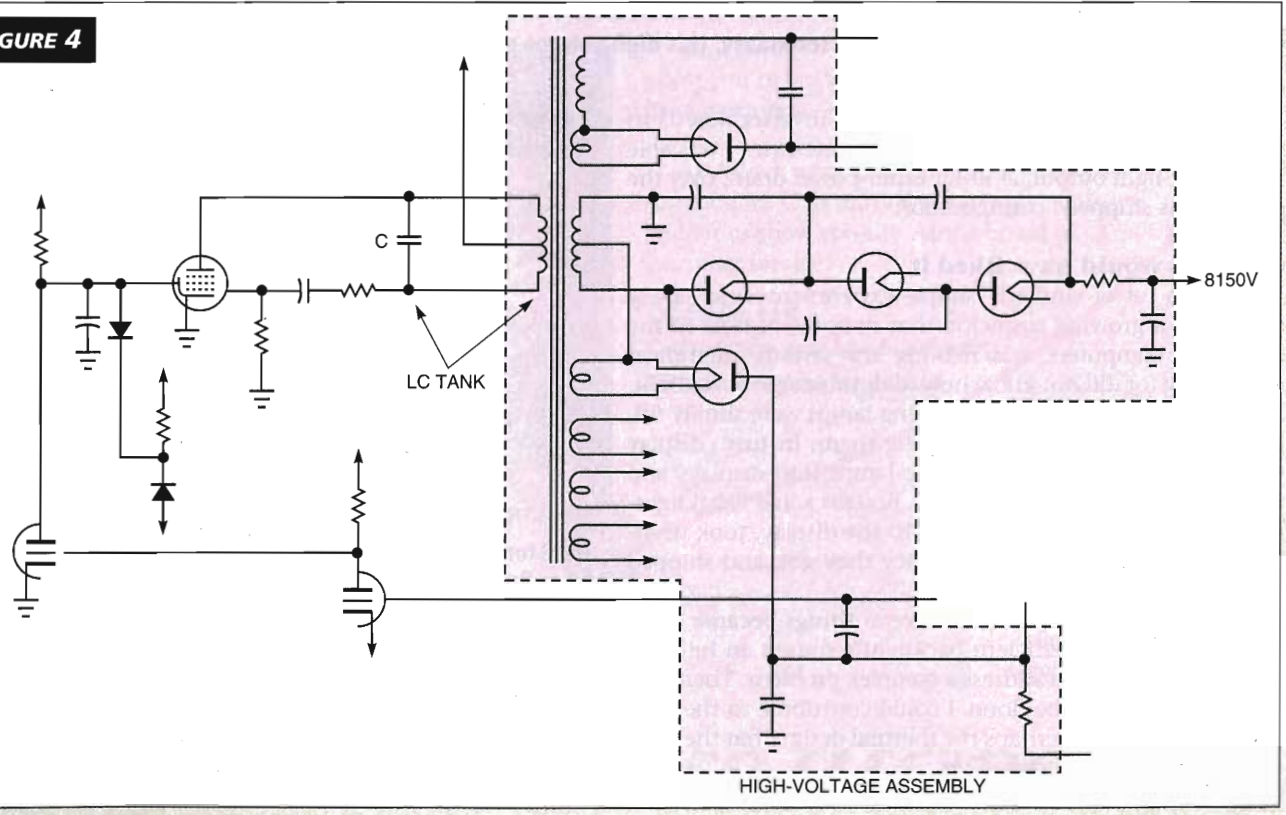
I removed lamps from the displays; all appeared to have been installed by the display vendor, as opposed to being selected and purchased by the computer manufacturer. Even more interesting was the fact that I found identical backlight boards in different computers driving different types of lamps. It appeared that no board changes were made to accommodate various lamps. I then turned my attention to the lamps.

The lamps seemed to be pretty complex, wild animals. I noticed that many of them took noticeable time to arrive at maximum intensity. Some types seemed to emit more light than others for a given input power. Still others had a wider dynamic range of intensities than the rest, although all had a fairly narrow range of intensity control. Most striking was the fact that every lamp's emissivity varied with ambient temperature. Experimenting with a hair dryer, a can of "cold spray," and a photometer, I found that each lamp seemed to have an optimum operating-temperature range. Excursions above or below this region caused emittance to fall.

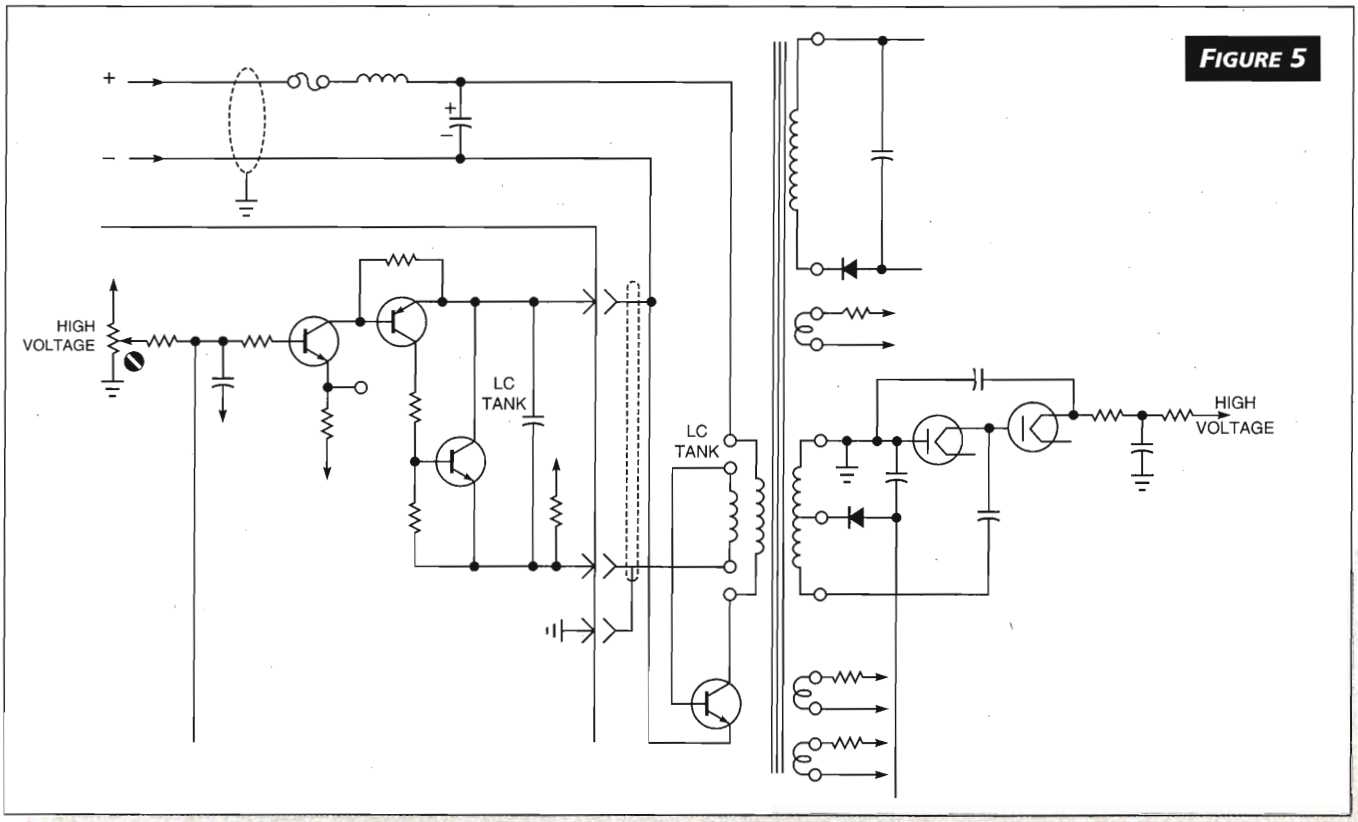
I put a lamp into a reassembled display. With the display warmed up in a 25°C environment, I was able to increase light output by slightly ventilating the lamp enclosure. This move increased steady-state thermal losses, allowing the lamp to run in its optimum temperature range. I also saw screen-illumination shifts arising from the distance between the light entry point at the display edge and the lamp. There seemed to be some optimum distance between the lamp and the entry point.

Simply coupling the lamp as closely as possible did not provide the best results. Similarly, the metallic reflective foil used to concentrate the lamp's output seemed to be sensitive to placement. Additionally, I noted a distinct tradeoff between benefits from the foil's optical reflection and its absorption of high-voltage field energy. Removing the foil reduced input energy for a given lamp emission level. I could watch input power rise as I slipped the foil back along the lamp's length. In some cases, with the foil fully replaced, I

FIGURE 4




**The perhaps-unfamiliar symbols in this diagram for the high-voltage section in the Tektronix 547 oscilloscope are vacuum tubes. The capacitor and primary inductance form a resonant tank circuit.**




**Except for the vacuum-tube diodes in the secondary, this high-voltage circuit is the solid-state version of the circuit in Fig 4.**

could draw sparks from it with my finger!

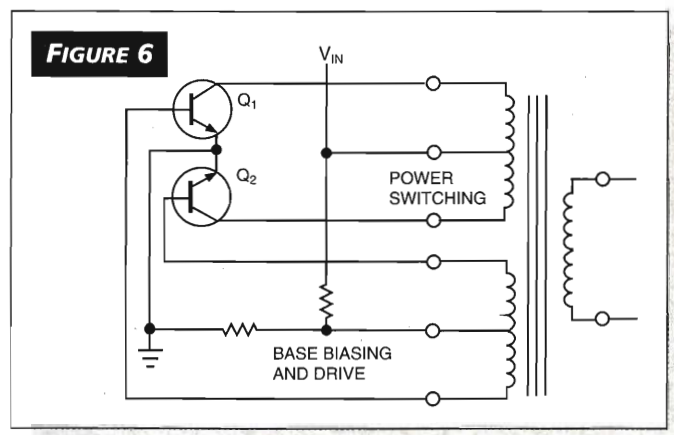
I also assembled lamps, displays, and inverter boards in various nonoriginal combinations. In some cases I was able to increase light output, at lower input-power drain, over the original "as-shipped" configuration.

### Grandpa would have liked it

I tried a lot of similarly simple experiments and slowly developed a growing suspicion that nobody, at least in my sample of computers, was making any serious attempt at optimizing (or did not know how to optimize) the backlight. It appeared that most people making lamps were simply filling tubes up with gas and shipping them. In turn, display manufacturers just dropped these lamps into displays and shipped them. Computer vendors bought some "backlight-power-supply" board, wired it up to the display, took whatever electrical and optical efficiency they got, and shipped the computer.

If I allowed this conclusion, several things became clear. Development of an efficient backlight required an interdisciplinary approach to address a complex problem. There was worthwhile work to be done. I could contribute to the electronic portion, and perhaps the thermal design, but the optical engineering was beyond me.

It was not, however, beyond Apple's resources. Apple had some very good optical types. Working together, we had a chance to build a better backlight, with its attendant display-quality and battery-life advantages. Apple would get a more




**Transformer saturation produces the switching in this circuit from Ref 3. The transistors conduct out of phase, switching each time the transformer saturates.**

saleable product, and my company would develop a valued customer. And, because the endeavor was getting interesting, I saw it as my way out of a rut. Business-school types call this a "synergistic" or "win-win" situation. Other people who "do lunch" on company money might call it "strategic partnering." My grandfather would have called it "such a deal."

Goals for the backlight began to emerge. For best overall efficiency, it was necessary to simultaneously consider the display enclosure, optical design, lamp, and electronics. My

job involved the electronics, although I met regularly with Paul Donovan, who was working on the other issues. In particular, I was actively involved in setting lamp specifications and evaluating lamp vendors.

Obviously, the electronics should be as efficient as possible. The circuit should be physically compact, have a low parts count, and assemble easily. It should have a wide, continuous dimming range with no hysteresis or "pop-on" and should meet all RF and system emission requirements. Finally, it must regulate lamp intensity against wide power-supply shifts, such as those that occur when the computer's ac adapter is plugged in.

Where, I wondered, had I seen circuitry that contained any or all of these characteristics? Nowhere. But, one area to start looking was oscilloscope design. Although oscilloscope circuits do not accomplish what I needed to do, oscilloscope designers use high-frequency sine-wave conversion to generate the high-voltage CRT supply. This technique minimizes noise and reduces transformer and capacitor size. Handling the conversion locally at the CRT eliminates long high-voltage runs from the main power supply.

I examined the schematic of the high-voltage converter in a Tektronix 547 (**Fig 4**). The manual explains that capacitor C and the transformer primary form a resonant tank circuit. More subtly, the "transformer primary" also includes the complex impedance reflected back from the secondary and its load. But that's a detail for the scope circuit, in which the CRT is a relatively linear and benign load. It would be necessary to evaluate the backlight's loading characteristics and match them to the circuit.

This CRT circuit could not be used to drive a fluorescent backlight tube in a laptop computer. For one reason, this circuit isn't very efficient. It doesn't need to be. A 547 pulls over 500W, so efficiency in this circuit wasn't a big priority. Latter versions of this configuration used transistors (**Fig 5**, Tektronix 453) but basically had the same architecture. Both circuits use the resonating technique and a feedback loop to enforce voltage regulation. For another reason, the CRT requires rectifying the high voltage to dc. The backlight requires ac, eliminating the rectifier and filter. And, the CRT circuit had no feedback. Some form of feedback for the fluorescent lamp seemed desirable.

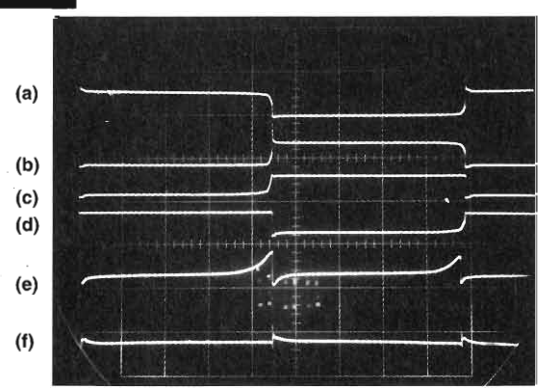
The jewel in the CRT circuit, however, was the resonating technique used to create the sine wave. The transformer does double duty. It helps create the sine wave while simultaneously generating the high voltage. So I needed to figure out how to combine this circuit's desirable resonating characteristics with other techniques to meet the backlight's requirements. One key was a simple, more efficient transformer drive. I knew just where to find it.

In 1954, "Transistors as On-Off Switches in Saturable-Core Circuits" (**Ref 3**) appeared in *Electrical Manufacturing* magazine. George Royer, one of the authors, described a "dc-to-ac converter" as part of this paper. Using Westinghouse 2N74 transistors, Royer reported 90% efficiency for his circuit. The operation of Royer's circuit is well-described in the paper. The Royer converter was widely adopted and used in designs from watts to kilowatts; it is still the basis for a variety of power-conversion systems.

Royer's circuit is not an LC resonant type. The transformer is the sole energy-storage element, and the output is a square wave. **Fig 6** is a conceptual schematic of a typical converter. The input connects to a self-oscillating configuration comprising transistors, a transformer, and a biasing network. The transistors conduct out of phase, switching each time the transformer saturates. In **Fig 7**, **Traces A** and **C** are $Q_1$'s collector and base waveforms; **Traces B** and **D** are $Q_2$'s collector and base waveforms. Transformer saturation causes a rapidly rising, high current to flow (**Trace E**).

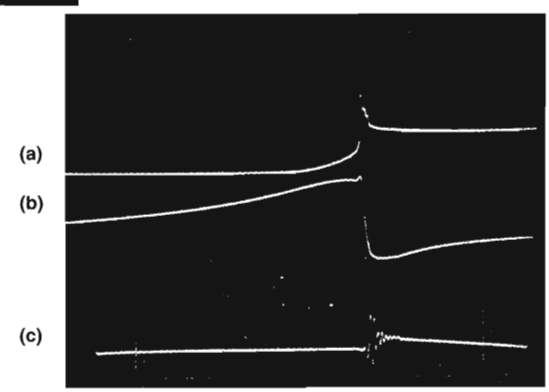
This current spike, picked up by the base-drive winding, switches the transistors. Phase-opposed switching causes the transistors to exchange states. Current abruptly drops in the formerly conducting transistor and then slowly rises in the newly conducting transistor until saturation again forces switching. This alternating operation sets transistor duty cycle at 50%.

**FIGURE 7**




**The first and third and second and fourth traces are the collector and base waveforms, respectively, for the Royer circuit in Fig 6. The base-drive winding delivers the current spike in Trace E to the switching transistors.**

**FIGURE 8**

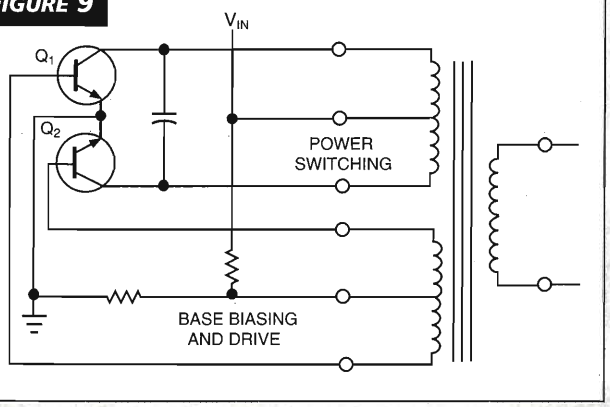



**This expanded display shows the relationship between transformer current (Trace B) and transistor collector voltage (Trace A) in the Royer circuit.**

The photo in **Fig 8** is a time and amplitude expansion of **Traces B** and **E** of **Fig 7**. It clearly shows the relationship between transformer current (**Trace B**) and transistor collector voltage (**Trace A**).

The Royer circuit has many desirable elements that are applicable to backlight driving. Transformer size is small because core utilization is efficient. Parts count is low, the circuit self-oscillates and is efficient, and the output power is variable over a wide range. The inherent nature of operation produces a square-wave output, which is not permissible for backlight driving.

**FIGURE 9**




**The op amp and transistor provide a means to control the output power of the modified Royer circuit in Fig 9. The transistor current sink operates in the linear region and thus wastes power.**

Adding a capacitor to the primary drive (**Fig 9**) should have the same resonating effect that exists in the Tektronix CRT circuits. The beauty of this configuration is its utter simplicity and high efficiency. As the loading (viz, lamp intensity) varies, the reflected secondary impedance changes, causing some frequency shift, but efficiency remains high.

You can control the Royer's output power by varying the primary drive current. **Fig 10** shows a way to investigate this relationship. This circuit works well, except that the transistor current sink operates in its linear region, wasting power. **Fig 11** converts the current sink to switch-mode operation, which yields high efficiency. Obviously, this enhanced efficiency is an advantage for the user; but it's also a good deal for my employer.

I had spent the previous six months playing with light bulbs, reminiscing over old oscilloscope circuits, taking arcane thermal measurements, and pursuing similar dalliances—all the while collecting a paycheck. Finally, I had found an application where I could actually sell something my company manufactured. Linear Technology builds a

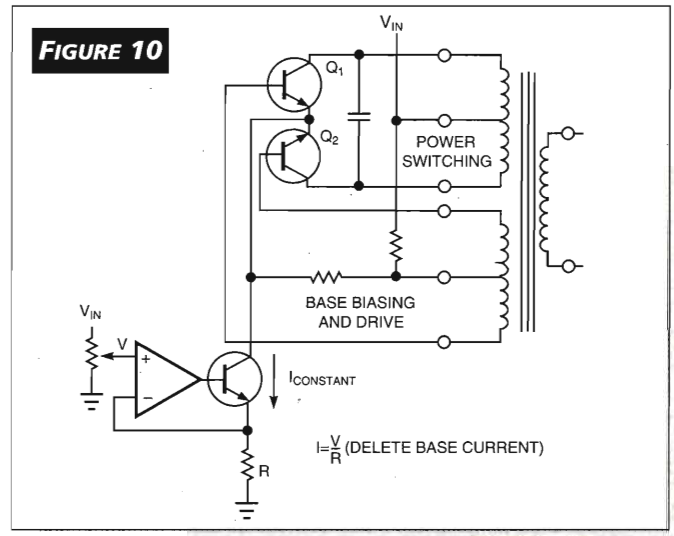
switching regulator called the LT1172. Its features include a high-power, open-collector switch, trimmed reference, low quiescent current and shutdown capability. Additionally, the LT1172 is available in an eight-pin, surface-mount package, a must for board-space considerations. It was also an ideal candidate for the circuit's current-sink portion.

In the design effort, I gained insight not only from the Tektronix scope manuals and the Royer circuit in **Ref 3**, but also from every document in the long list of **references** at the end of this article.

### Dive right in

At about this stage, I sat back and stared at the wall. At some point in every project, you have to gamble. It's time to halt the analytics and theorizing and commit to an approach—and start actually doing something. This realization is often painful, because you never really have enough information and preparation to be confidently decisive. Answers are rare, and choices abound. But, at some point, your gut tells you to put down the pencil and pick up the soldering iron. Physicist Richard Feynman once said "If you're not confused when you start, you're not doing it right." And I think it was an artist who said "Inspiration comes while working." They were both right. It was now obvious to me that you cannot wait for your perfect circuit to design itself.

Everything was still pretty fuzzy, but I had learned a few




**Adding a capacitor to the primary drive in the Royer circuit produces the same LC-tank resonance as exists in the Tektronix high-voltage circuits.**

things. A practical, highly efficient LCD backlight design is a classic study of compromise in a transduced electronic system. Every aspect of the design is interrelated, and the phys-

ical embodiment is an integral part of the electrical circuit. The choice and location of the lamp, wires, display housing, and other items have a major effect on electrical characteristics. The greatest care in every detail is required to achieve a practical high-efficiency LCD backlight. Getting the lamp to light is just the beginning! EDN

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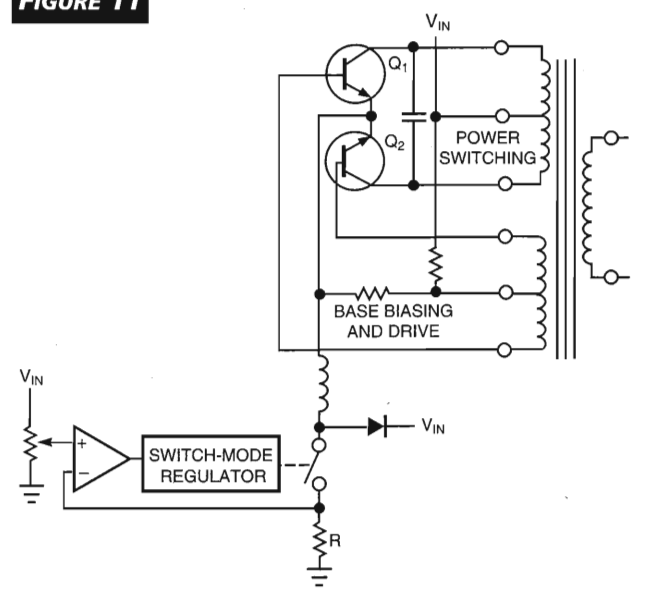
**FIGURE 11**




**The switch-mode regulator eliminates the power waste inherent in the linear regulator of Fig 10.**

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## Author's biography

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ANALOG SPECIAL ISSUE

# Measurements on CCFL-driver circuits pose tricky problems

JIM WILLIAMS, LINEAR TECHNOLOGY

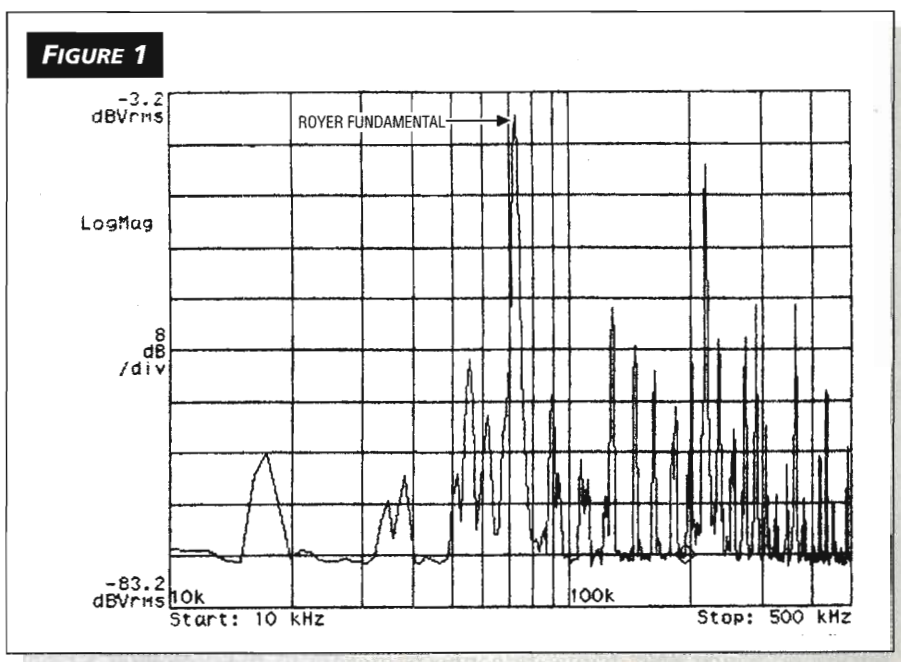
**Obtaining reliable efficiency data for CCFL circuits presents difficult measurement problems. The accuracy required in the high-frequency ac measurements is uncomfortably close to the state of the art.**

Drivers for cold-cathode fluorescent lamps (CCFLs) are intriguing devices (**Reference 1**). They must produce fairly high-voltage (hundreds of volts rms), quasi-sinusoidal, adjustable, regulated ac voltages, usually at tens or hundreds of kilohertz. The drivers must operate from low-voltage, often unregulated dc sources. Most CCFL drivers deliver modest amounts of power—usually <1W, but must do so with high efficiency (~90%). Moreover, the operating conditions that produce the maximum electrical efficiency ($P_{OUT}/P_{IN}$) don't always produce the best optoelectrical efficiency (light out/$P_{IN}$). As a result, when developing CCFL drivers, and even when designing IC drivers into assembled products, achieving optimal performance requires making many challenging measurements. Understanding how to properly make these measurements is useful, even if you aren't designing or using CCFL drivers. If your job involves applying measurement technology, or if you are merely interested in electrical measurements, there's a good chance you can find other applications for CCFL-circuit techniques.

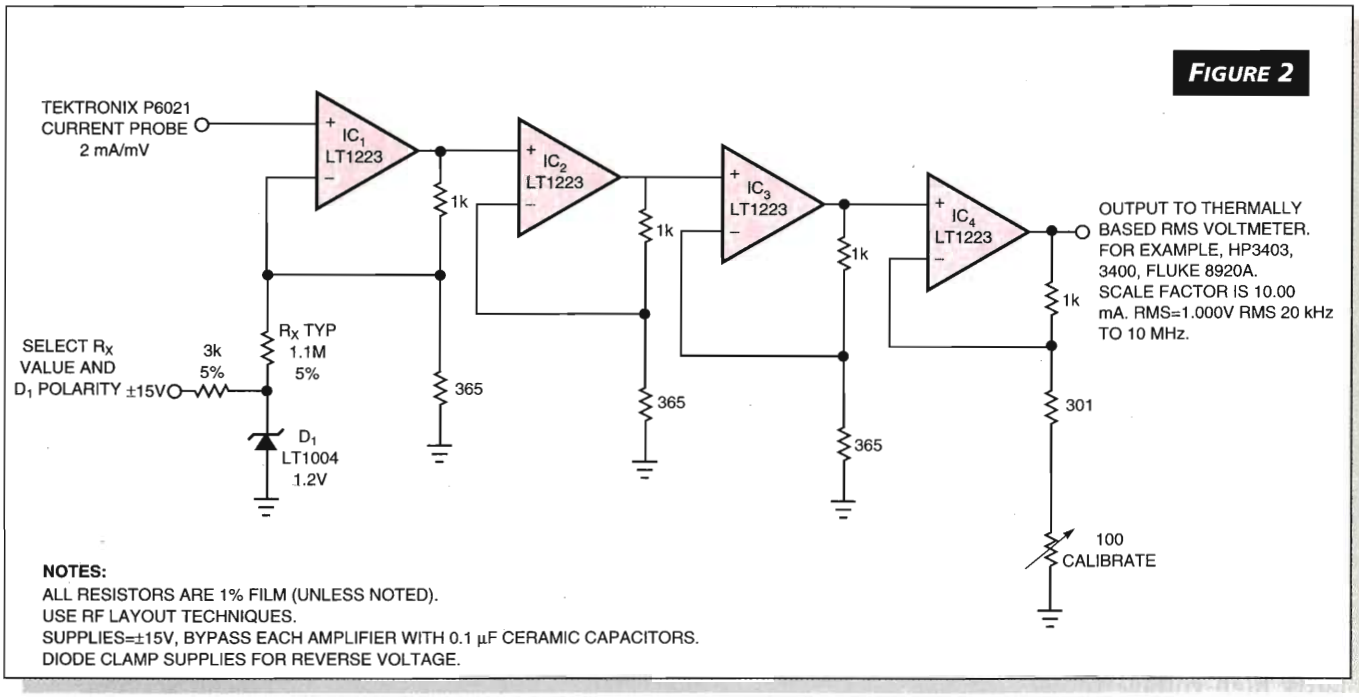
Establishing and maintaining accurate wideband ac measurements is a textbook example of a situation that requires careful attention to measurement. The combination of high-frequency, harmonic-laden waveforms and high voltage makes obtaining meaningful results difficult. Careful selection, understanding, and use of test instrumentation is crucial. You must think clearly to avoid unpleasant surprises.

The lamp's current and voltage waveforms contain energy over a wide frequency range. Most of this energy is concentrated at the inverter's fundamental frequency and immediate harmonics. However, for 1% measurement uncertainty, you must accurately capture energy content out to 10 MHz. **Figure 1**, a spectrum analysis of lamp current, shows significant energy at 500 kHz. Diminished, but sig-

**FIGURE 1**




**A spectral plot of lamp current shows significant energy to 500 kHz.**




**This precision clip-on current probe for CCFL measurements maintains 1% inaccuracy from 20 kHz to 10 MHz.**

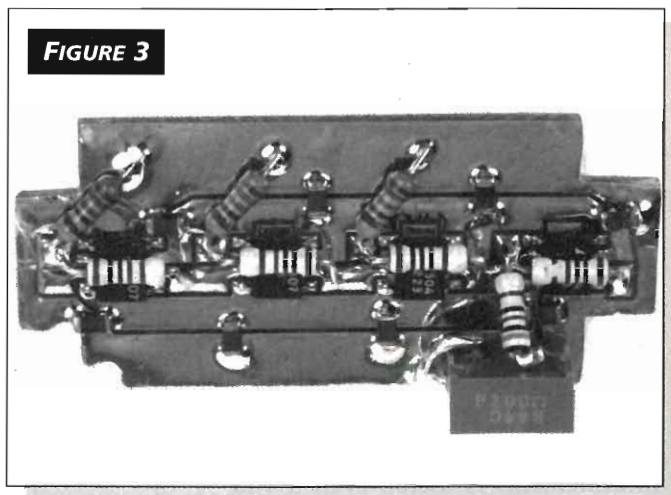
nificant, content is still apparent, however. This data suggests that the monitoring instrumentation must maintain high accuracy over wide bandwidth.

Accurate determination of rms operating current is important for electrical- and emissivity-efficiency computations and for ensuring long lamp life. Additionally, you may want to perform current measurements in the presence of high common-mode voltage (>1000V rms). The ability to make such measurements allows investigation and quantification of display- and wiring-induced losses, regardless of their origins in the lamp-drive circuitry.

### Current-probe circuitry

**Figure 2**'s circuit meets these measurement requirements. The **figure** shows a precision amplifier conditioning the output of a commercially available clip-on current probe. This configuration provides 1% measurement accuracy to 10 MHz. The clip-on probe is convenient even in the presence of high common voltages. The current probe biases $IC_1$, which operates at a gain of about 3.75. The probe's low-output-impedance termination eliminates the need for impedance matching. Additional amplifiers provide distributed gain, maintaining wide bandwidth with an overall gain of about 200. The individual amplifiers avoid any possible crosstalk-based error that a monolithic quad amplifier might introduce. Selecting $D_1$ and $R_X$ and choosing $D_1$'s polarity trim the overall amplifier offset. The 100Ω trimmer sets the gain, fixing the scale factor.

The output drives a thermally based, wideband, rms voltmeter. In practice, the circuit is built into a 2.25×1×1-in. enclosure, which BNC hardware connects directly to the voltmeter. There is no cable. **Figure 3** details RF layout techniques used in the amplifier's construction. The result is a clip-on current probe with 1% accuracy over a 20-kHz to 10-MHz bandwidth. This tool is indispensable in any rigorously conducted backlight work.




**To achieve the performance levels indicated in the text, the current-probe-amplifier layout uses RF techniques.**

**Figure 4**'s circuit, a current calibrator, permits calibration of the probe and amplifier. $IC_1$ and $IC_2$ form a Wein-bridge oscillator. $IC_4$ and $IC_5$ rectify the oscillator output; $IC_3$ compares the rectified output to a dc reference. $IC_3$'s output controls $Q_1$, closing an amplitude-stabilization loop. The amplitude-stabilized voltage terminates in a 100Ω, 0.1% resistor to provide a precise 10.00-mA, 60-kHz current through the series-current loop. Adjusting the nominally 15-kΩ resistor

## TABLE 1—CHARACTERISTICS OF SOME WIDEBAND HIGH-VOLTAGE PROBES

| TEKTRONIX PROBE TYPE | ATTENUATION FACTOR | ACCURACY | INPUT RESISTANCE | INPUT CAPACITANCE | RISE TIME | BAND-WIDTH | MAXIMUM VOLTAGE | DERATED ABOVE | DERATED TO AT FREQUENCY | COMPENSATION RANGE | ASSUMED TERMINATION RESISTANCE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| P6007 | 100X | 3% | 10M | 2.2pF | 14ns | 25MHz | 1.5kV | 200kHz | $700V_{RMS}$ at 10MHz | 15pF to 55pF | 1M |
| P6009 | 100X | 3% | 10M | 2.5pF | 2.9ns | 120MHz | 1.5kV | 200kHz | $450V_{RMS}$ at 40MHz | 15pF to 47pF | 1M |
| P6013A | 1000X | Adjustable | 100M | 3pF | 7ns | 50MHz | 12kV | 100kHz | $800V_{RMS}$ at 20MHz | 12pF to 60pF | 1M |
| P6015 | 1000X | Adjustable | 100M | 3pF | 4.7ns | 75MHz | 20kV | 100kHz | $2000V_{RMS}$ at 20MHz | 12pF to 47pF | 1M |

for exactly 1.000V rms across the 100Ω resistor trims the output.

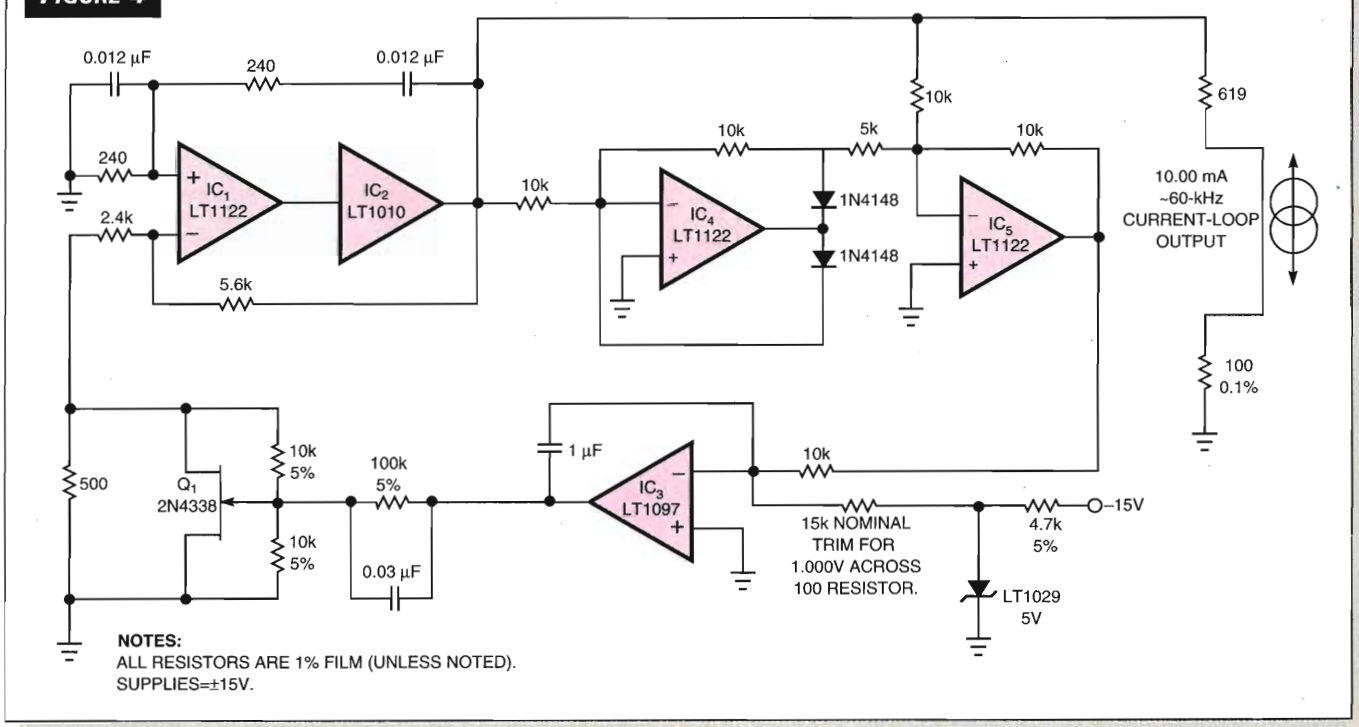
Over one year, this current probe has shown 0.2% baseline instability with 1% absolute error. The sole maintenance requirements for preserving accuracy are to keep the current-probe jaws clean and to avoid rough or abrupt handling of the probe.

### Voltage probes for grounded-lamp circuits

The high-voltage measurement across the lamp is demanding on the probe. The simplest case is measuring grounded-lamp circuits, in which the waveform fundamental is at 20 to 100 kHz, with harmonics into the megahertz region. This activity occurs at peak voltages in the kilovolt range. The probe must have a high-fidelity response under these conditions. Additionally, the probe should have low input capacitance to avoid loading effects that would corrupt the measurement. The design and construction of such a probe requires significant attention. **Table 1** lists some recommended probes and characteristics. Almost all standard oscilloscope probes fail if you try to use them for this measurement.

Attempting to circumvent the probe requirement by resistively dividing the lamp voltage also creates problems. Large-value resistors often have significant voltage coefficients, and the resistors' shunt capacitance is high and uncertain.

FIGURE 4




**This current calibrator forces an accurate and stable 10.00 mA rms at 60 kHz through the output-current loop.**

Therefore, avoid simple voltage dividers. Similarly, most high-voltage probes intended for dc measurement introduce large errors because of ac effects. The Tektronix P6013A and P6015 work well; the devices' 100-MΩ resistance and small capacitance introduce low loading errors. The penalty for their 1000× attenuation is reduced output, but the recommended voltmeters accommodate the small signals.

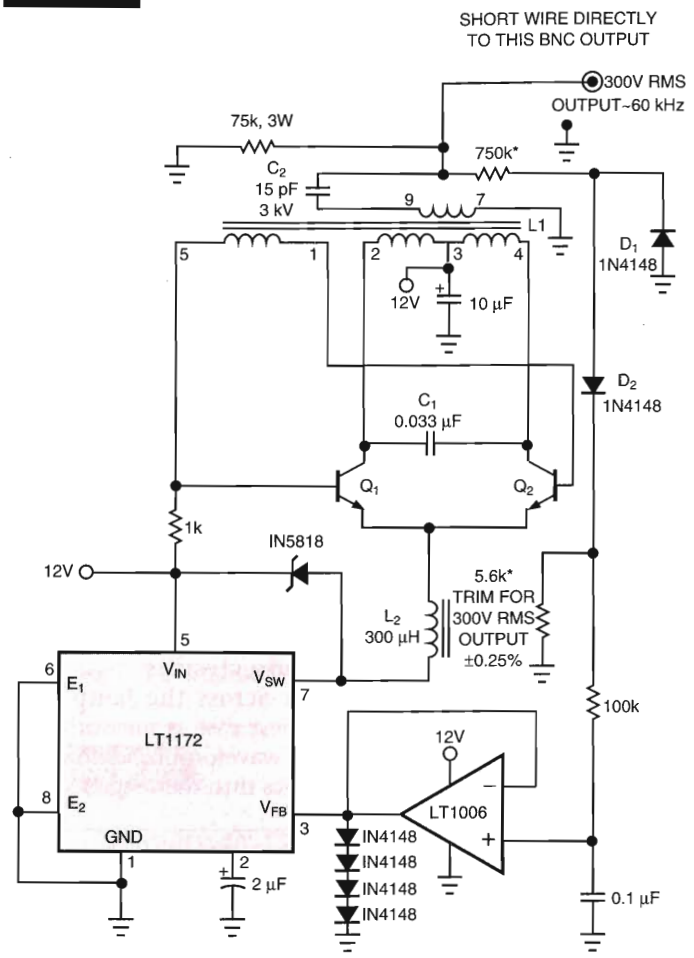
All of the recommended probes are designed to work into an oscilloscope input. Such inputs are almost always 1 MΩ paralleled by (typically) 10 to 22 pF. The recommended voltmeters have significantly different input characteristics. **Table 2** shows higher input resistances and a range of capacitances. Because of this difference, the probe compensation must accommodate the voltmeter's input characteristics. Normally, you can easily determine and adjust the optimum compensation point by observing the probe output on an oscilloscope. Apply a known-amplitude square wave, such as that from the oscilloscope calibrator, and adjust the probe for correct response.

Using the probe with the voltmeter presents an unknown impedance mismatch and raises the problem of determining when compensation is correct. The impedance mismatch occurs at low and high frequencies. To correct the low-frequency effect, place an appropriate-value resistor in shunt with the probe's output. For a 10-MΩ voltmeter input, a 1.1-MΩ resistor is suitable. Maintaining a coaxial environment, requires you to build this resistor into the smallest possible BNC-equipped enclosure. Do not use cable connections; place the enclosure directly between the probe output and the voltmeter input to minimize stray capacitance. This arrangement compensates the low-frequency impedance mismatch.

Correcting the high-frequency mismatch is more involved. Problems result from the wide range of voltmeter input capacitances combined with effects of the added shunt resistor. Knowing where to set the high-frequency probe-compensation adjustment is confusing. One solution is to feed a known-value rms signal to the probe-voltmeter combination and adjust the compensation for a proper reading. **Figure 5** shows a way to generate a known rms voltage. This scheme uses a standard backlight circuit reconfigured to produce a constant-voltage output. The op amp permits low R-C loading of the 5.6-kΩ feedback termination without introducing bias-current error. You can series- or parallel-trim the 5.6-kΩ value to obtain a 300V output. Stray parasitic capacitance in the feedback network affects the output voltage. Because of this effect, you should rigidly fix all feedback-associated nodes and components and build the entire circuit into a small metal box. This construction prevents any significant change in the parasitic-element values. The result is a known 300V-rms output.

Now, adjust the probe's compensation for a 300V voltmeter indication using the shortest possible connection to the calibrator box (for example, a BNC-to-probe adapter). This procedure, combined with the added resistor, completes the probe-to-voltmeter impedance match. If you alter the probe compensation (for example, for proper response on an oscilloscope) the voltmeter's reading becomes erroneous. Therefore, you may want to hide the probe when you aren't using it. It is good practice to verify the calibrator-box output before and after every set of efficiency measurements. Do this by using BNC adapters to directly connect the cali-

**FIGURE 5**




**NOTES:**
$C_1$ = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB.
WIMA FKP2, MDP-20 (GERMAN) OR PANASONIC ECH-U RECOMMENDED.
$L_1$ = SUMIDA 6345-020 OR COILTRONICS CTX110092-1
PIN NUMBERS SHOWN FOR COILTRONICS UNIT.
$L_2$ = COILTRONICS CTX300-4.
$Q_1$, $Q_2$ = ZETEX ZT849 OR ZDT1048.
* = 1% FILM RESISTOR (75-kΩ RESISTORS IN SERIES).

**This high-voltage rms calibrator is a voltage-output version of a CCFL driver circuit.**

brator box to the rms voltmeter. Set the voltmeter to the 1000V range.

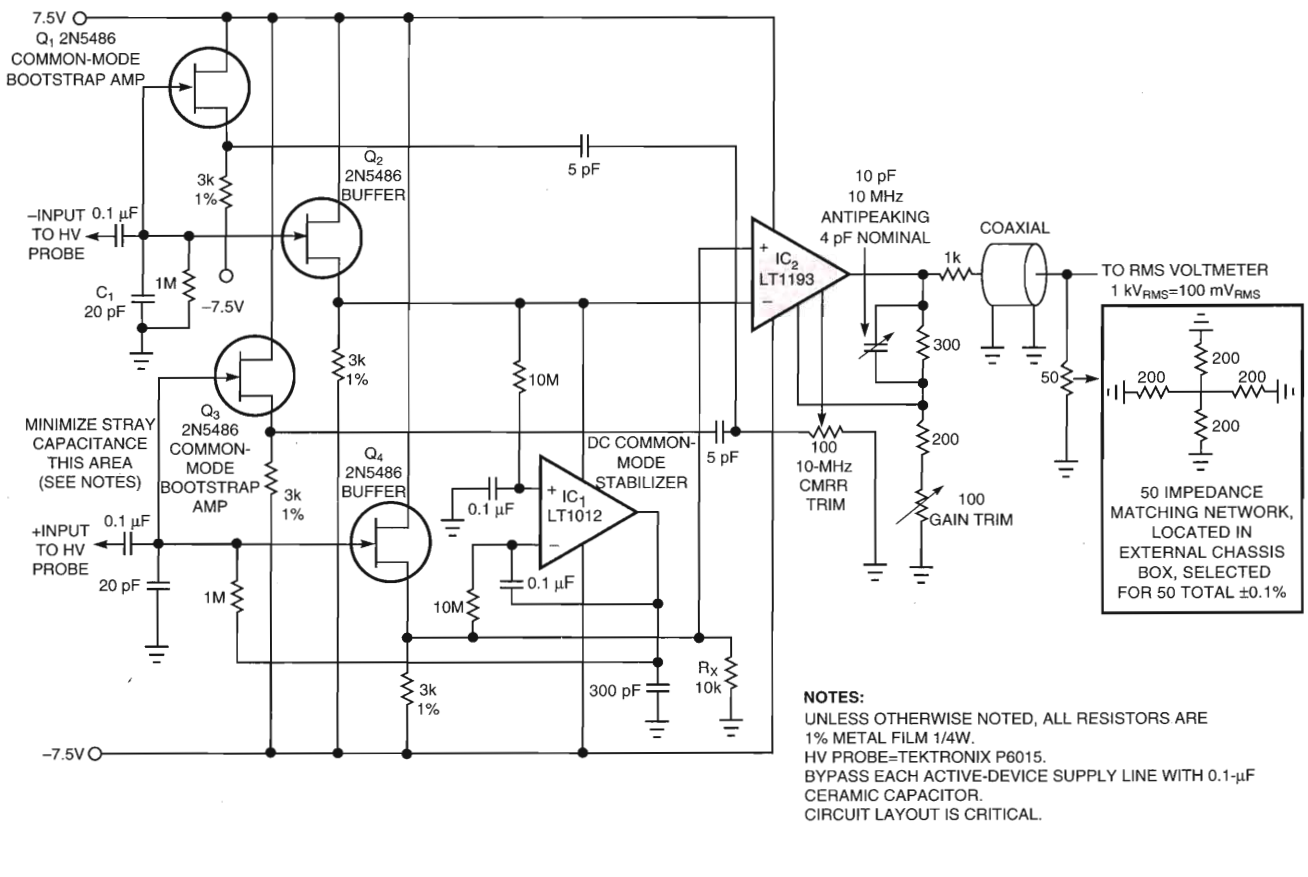
### Voltage probes for floating-lamp circuits

Measuring voltages in floating-lamp circuits requires a nearly heroic effort. Floating-lamp measurement involves all the difficulties of the grounded case but also needs a fully differential input, because the lamp floats freely from ground. You must not only properly compensate the two probes, but also match and calibrate them within 1%. Additionally, to check calibration, you need a fully floating source instead of **Figure 5**'s simple single-ended setup.

## TABLE 2—CHARACTERISTICS OF SOME THERMAL RMS VOLTMETERS

| MANUFACTURER AND MODEL | FULL SCALE RANGES | ACCURACY AT 1MHz | ACCURACY AT 100kHz | INPUT RESISTANCE AND CAPACITANCE | MAXIMUM BANDWIDTH | CREST FACTOR |
|---|---|---|---|---|---|---|
| Hewlett-Packard 3400 Meter Display | 1mV to 300V, 12 Ranges | 1% | 1% | 0.001V to 0.3V Range = 10M and < 50pF, 1V to 300V Range = 10M and < 20pF | 10MHz | 10:1 At Full Scale, 100:1 At 0.1 Scale |
| Hewlett-Packard 3403C Digital Display | 10mV to 1000V, 6 Ranges | 0.5% | 0.2% | 10mV and 100mV Range = 20M and 20pF ±10%, 1V to 1000V Range = 10M and 24pF ±10% | 100MHz | 10:1 At Full Scale, 100:1 At 0.1 Scale |
| Fluke 8920A Digital Display | 2mV to 700V, 7 Ranges | 0.7% | 0.5% | 10M and < 30pF | 20MHz | 7:1 At Full Scale, 70:1 At 0.1 Scale |

**FIGURE 6**




**NOTES:**
UNLESS OTHERWISE NOTED, ALL RESISTORS ARE 1% METAL FILM 1/4W.
HV PROBE=TEKTRONIX P6015.
BYPASS EACH ACTIVE-DEVICE SUPPLY LINE WITH 0.1-µF CERAMIC CAPACITOR.
CIRCUIT LAYOUT IS CRITICAL.

**This precision wideband differential probe amplifier permits floating lamp-voltage measurements. Source followers combine with impedance-matching networks to unload the probes. $IC_2$ provides differential to single-ended conversion.**

## CCFL-DRIVE-CIRCUIT MEASUREMENTS

**Figure 6**'s differential amplifier converts the differential output of the high-voltage probes to a single-ended signal for driving an rms voltmeter. If the probe compensation and calibration are correct, the amplifier introduces <1% error in 10-MHz bandwidth. Both probe inputs feed source followers ($Q_1$ through $Q_4$) via R-C networks that provide proper probe termination. $Q_2$ and $Q_4$ bias differential-amplifier $IC_2$, which runs at a gain of ~2. $IC_1$ controls the FET dc and low-frequency differential drift. $IC_1$ measures a band-limited version of $IC_2$'s inputs and biases $Q_4$'s gate-termination resistor. This arrangement forces $Q_4$ and $Q_2$ to equal source voltages. This control loop eliminates dc and low-frequency error resulting from FET mismatches. Although you might want to use a monolithic dual FET, such devices cause excessive high-frequency errors.

$Q_1$ and $Q_3$ also follow the probe output and feed a small, frequency-dependent, summed signal to $IC_2$'s auxiliary input. This signal corrects for the high-frequency common-mode-rejection limitations of $IC_2$'s main inputs. $IC_2$'s output drives the rms voltmeter via a 20:1 divider. The divider combines with $IC_2$'s gain-bandwidth characteristics to give <1% error to 10 MHz at the voltmeter input.

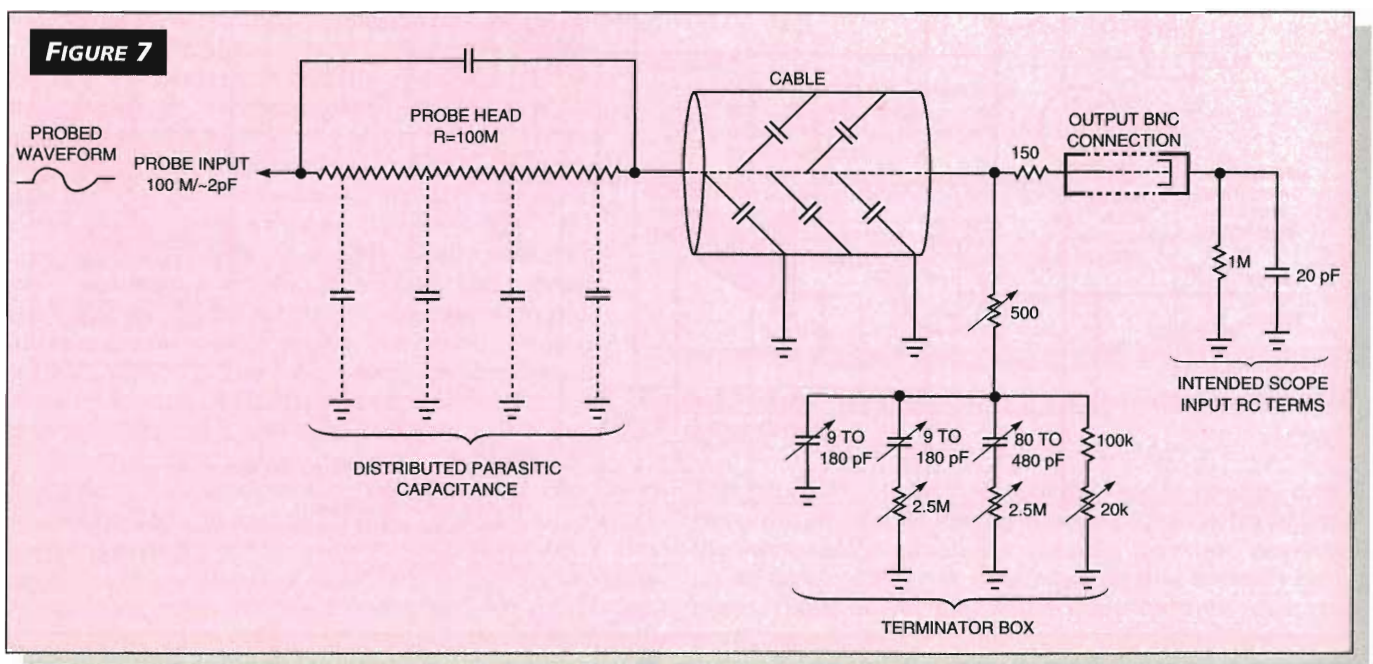
To calibrate the amplifier, tie both inputs together and select $R_X$ (shown at $Q_4$), so that $IC_1$'s output is near zero. You may have to place $R_X$ at $Q_2$ to make this trim. Next, drive the shorted inputs with a 1V, 10-MHz sine wave. Adjust the 10-MHz CMRR trim for a minimum rms voltmeter reading, which should be below 1 mV. Finally, lift the positive input from ground, apply 1V rms at 60 kHz, and set $IC_2$'s gain trim for a 100-mV voltmeter reading. As a check, grounding the positive input and driving the negative input with the 60-kHz signal should produce an identical meter reading. Further, known differential inputs at any frequency from 10 kHz to 10 MHz should produce corresponding calibrated and stable rms-voltmeter readings within 1%. You can correct readings outside this figure at the highest frequencies by adjusting the 10-MHz antipeaking trim. This adjustment completes the amplifier calibration.

The high-voltage probes must be properly frequency-compensated to give calibrated results with the amplifier. The R-C values at the amplifier inputs approximate the termination impedance for which the probe is designed. You must, however, precisely frequency-compensate individual probes to achieve the required accuracy. The probe characteristics make this exercise quite demanding.

### Probing for answers

**Figure 7** is an approximate schematic of the Tektronix P6015 high-voltage probe. A physically large, 100-MΩ resistor occupies the probe head. Although the resistor has repeatable wideband characteristics, it suffers from distributed parasitic capacitances. These distributed capacitances combine with similar cable losses, presenting a distorted version of the probed waveform to the terminator box. When properly adjusted, the terminator box impedance-vs-frequency characteristic corrects the distorted information, presenting the proper waveform at the output. The probe's 1000× attenuation factor and high impedance provide a safe, minimally invasive measure of the input waveform.

The large number of parasitic elements associated with the probe head and cable result in a complex, multiple-time-constant response characteristic. Faithful wideband response requires the terminator box components to separately compensate for each of these time constants. There-



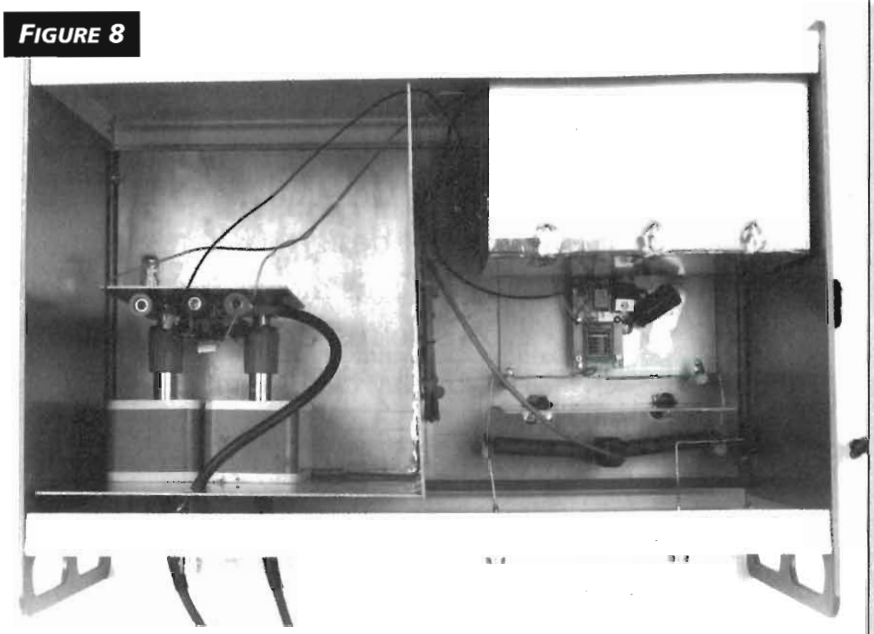

**Because of numerous distributed parasitic capacitances, the Tektronix P6015 high-voltage probe includes interactive trims.**

## CCFL-DRIVE-CIRCUIT MEASUREMENTS

fore, you must make no fewer than seven adjustments to compensate the probe to any particular instrument input. These trims are interactive, requiring a repetitive sequence before the probe is fully compensated. The probe manual describes the trimming sequence, using the intended oscilloscope display as the output. In this application, the ultimate output is from an rms voltmeter connected via the just-described differential amplifier. The meter display complicates determining the probe's proper compensation point but does not make the adjustment impossible.

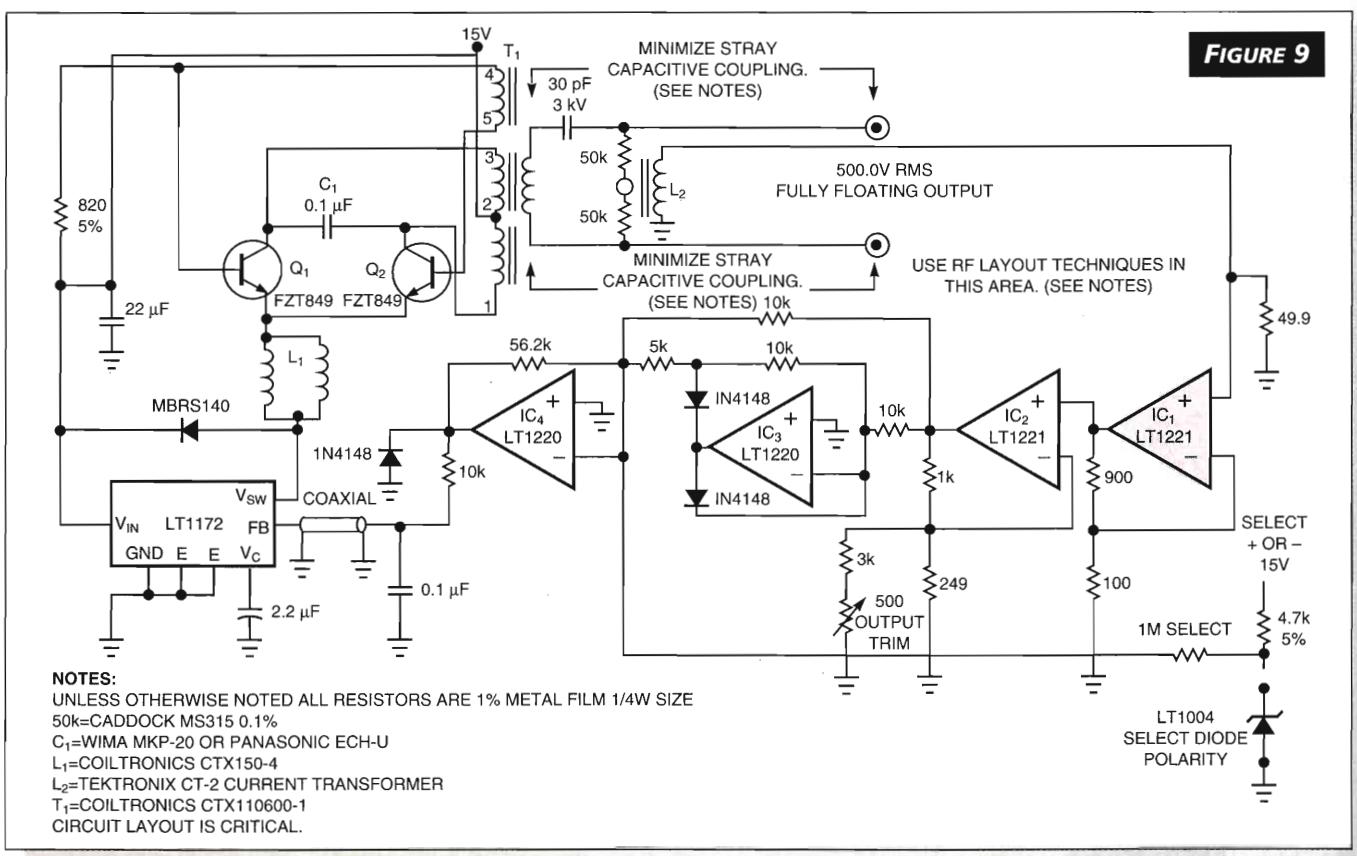
To compensate the probes, connect them directly to the calibrated differential amplifier (see **Figure 8**) and ground the probe associated with the negative input. Drive the positive-input probe with a 100V, 100-kHz square wave that has a clean 10-nsec edge with minimal aberrations following the transition. (Suitable pulse generators include the HP 214A and Tek-

**FIGURE 8**



**This interior view of the probe/calibrator shows, at the left, the differential amplifier, which mates directly with the probes. The calibrator is on the right. The current transformer is between the load resistors.**

**FIGURE 9**




**In this calibrator, the current transformer provides a floating output while maintaining tight loop control. Amplifiers provide gain to the inverter circuit's feedback node.**

## CCFL-DRIVE-CIRCUIT MEASUREMENTS

tronix 106.) The absolute amplitude of the waveform is unimportant. Use an oscilloscope and a properly compensated probe to monitor two points: the input square wave and $IC_2$'s output in the differential amplifier. Perform the compensation procedure described in the Tektronix P6015 manual until both waveforms have identical shapes. When you reach this state, repeat this procedure with the negative-input probe driven and the positive-input probe grounded. This sequence brings the probe's interactive adjustments reasonably close to the optimum points.

To complete the calibration, connect the 50Ω precision termination (see **Figure 6**) and the rms voltmeter to the differential amplifier's output. Ground the negative-input probe and drive the positive probe with a known-amplitude high-voltage waveform of about 60 kHz, such as that from **Figure 7**'s calibrator.

Perform very slight readjustments of this probe's compensation trims to get the voltmeter's reading to agree with the calibrated input. (Account for scaling differences; ignore the voltmeter's range and decimal-point indications.) To make this adjustment, use the trim or trims that have the greatest influence; you should have to make only slight adjustments.

Upon completing this step, repeat the procedure using the 100V, 100-kHz square wave, verifying input/output-waveform edge fidelity. If waveform fidelity has degraded, retrim and try again. You may have to repeat the procedure several times to achieve the required accuracy with both waveforms. Repeat this procedure for the negative-probe adjustment with the positive probe grounded.

Next, short both probes together and drive them with the 100V, 100-kHz square wave. Ideally, the rms voltmeter should read zero. In practice, it should indicate well below 1% of input. You can adjust the differential amplifier's 10-MHz CMRR trim (**Figure 6**) to minimize the voltmeter reading. Then, with the probes still shorted, apply a swept 20-kHz-to-10-MHz sine wave with the highest amplitude available. Monitor $IC_2$'s output with an rms voltmeter, ensuring that the output never rises above 1% of the input amplitude. (You have now made 14 interactive adjustments.)

Finally, apply the highest available-known amplitude, swept 20-kHz-to-10-MHz signal to each probe with the other probe grounded. Verify that the rms voltmeter indicates correct and flat gain over the entire swept-frequency range for each case.

If your measurements do not meet any condition described in the preceding list, you must repeat the entire calibration sequence. At this point, this calibration is, at long last, complete.

### Differential-probe calibrator

A calibrator with a fully floating, differential output allows periodic operational checking of the differential probe's accuracy. You build this calibrator into the same enclosure as the differential probe.

**Figure 9** is a schematic of the calibrator. The circuit is a highly modified form of the basic backlight power supply. In this circuit, $T_1$'s output drives two precision resistors which are well-specified for high-frequency, high-voltage operation. $L_2$, a wideband current transformer, monitors the resistor's current. $L_2$'s placement between the resistors combines with $T_1$'s floating drive to minimize the effects of $L_2$'s parasitic capacitance. Although $L_2$ has parasitic capacitance, the capacitance is bootstrapped to essentially 0V, negating its effect. $IC_1$ and $IC_2$ amplify $L_2$'s secondary output. $IC_3$ and $IC_4$ act as a precision rectifier. The 10-kΩ/0.1-μF filter smooths $IC_4$'s output and closes a loop at the LT1172's feedback pin. As do other CCFL circuits, the LT1172 sets $T_1$'s output by controlling the drive to the magnetic multivibrator (usually called a Royer circuit, after its inventor, GH Royer).

To calibrate this circuit, ground the LT1172's $V_C$ pin, open one of the connections to $T_1$'s secondary winding, and select the LT1004's polarity and associated resistor value for 0V at $IC_4$'s output. Next, put a 5.00-mA, 60-kHz current through $L_2$. (You can use the output of the circuit in **Figure 8**, rescaled for 5.00 mA.) Measure $IC_4$'s smoothed output (the LT1172's feedback pin), and adjust the output trim for 1.23V. Next, reconnect $T_2$'s secondary, remove the current-calibrator connection and unground the LT1172 $V_C$ pin. The result is 500V rms at the calibrator's differential output. You can check this with the differential probe. Reversing the probe connections should have no effect; the readings should agree within 1%.

The differential probe and floating-output calibrator require almost fanatical attention to layout to achieve the performance levels noted. The wideband amplifier sections utilize RF layout techniques that **Reference 2** documents reasonably well. **Figures 8 and 9** detail practical construction considerations related to parasitic capacitance. EDN

## References

1. Williams, Jim, *A Fourth Generation of LCD-Backlight Technology,* Linear Technology Corp, Application Note 65, October 1995.

2. Williams, Jim, *High-speed amplifier techniques,* Linear Technology Corporation, Application Note 47, August 1991.

## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp, Milpitas, CA, specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology, Cambridge, MA. A former student at Wayne State University, Detroit, Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

# 0.02% V/F converter consumes only 26 μA

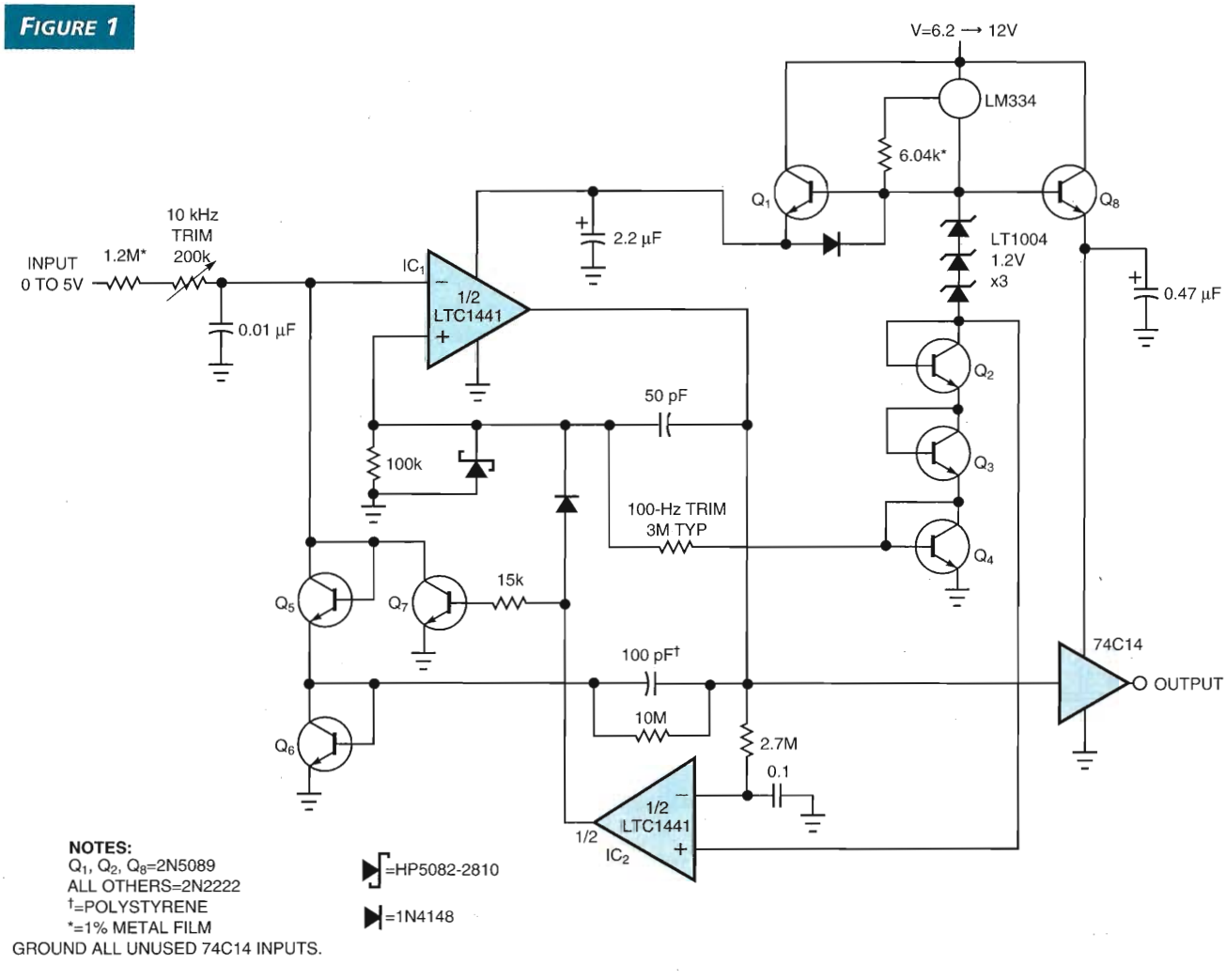
JIM WILLIAMS, LINEAR TECHNOLOGY, MILPITAS, CA

**Figure 1** shows a voltage-to-frequency (V/F) converter that produces a 0- to 10-kHz output for an input range of 0 to 5V. Linearity of the converter is 0.02%, and gain drift is 60 ppm/°C. The maximum current consumption is only 26 μA, 100 times lower than currently available units. To understand the circuit's operation, assume that the voltage at $IC_1$'s negative input is lower than the voltage at its positive input ($IC_2$'s output is low). The input difference results in a positive-going ramp at $IC_1$'s input (**Figure 2**, trace **A**).

$IC_1$'s output is high, allowing current to flow from the emitter of $Q_1$, through $IC_1$'s output stage, to the 100-pF capacitor. The 2.2-μF capacitor provides high-frequency bypassing, maintaining low impedance at the emitter of $Q_1$. The diode-connected transistor, $Q_6$, provides a path to ground. The voltage to which the 100-pF capacitor charges is a function of $Q_1$'s emitter voltage and the drop in $Q_6$. $IC_1$'s purely ohmic CMOS output contributes no voltage error. When the ramp at $IC_1$'s negative input goes high enough, $IC_1$'s output switches low (trace **B**) and the inverter switches high (trace **C**).

The switching action pulls current from $IC_1$'s negative-input capacitor via the $Q_5$ route (trace **D**). This current removal resets $IC_1$'s negative-input ramp to a potential slightly below ground. The 50-pF capacitor furnishes positive ac feedback to $IC_1$'s positive input (trace **E**), ensuring that $IC_1$'s output remains negative long enough for a com-

**FIGURE 1**




**This totally fat-free voltage-to-frequency converter manages to maintain 0.02% linearity on a diet of only 26 μA.**

# Chopped amplifier exacts only 5 μA

*JIM WILLIAMS, LINEAR TECHNOLOGY CORP, MILPITAS, CA*

The chopped amplifier in **Figure 1** combines low supply current of 5.5 μA with high accuracy. The offset voltage is 5 μV with a drift of 0.05 μV/°C. The gain exceeds $10^8$, which affords high accuracy, even at large closed-loop gains.

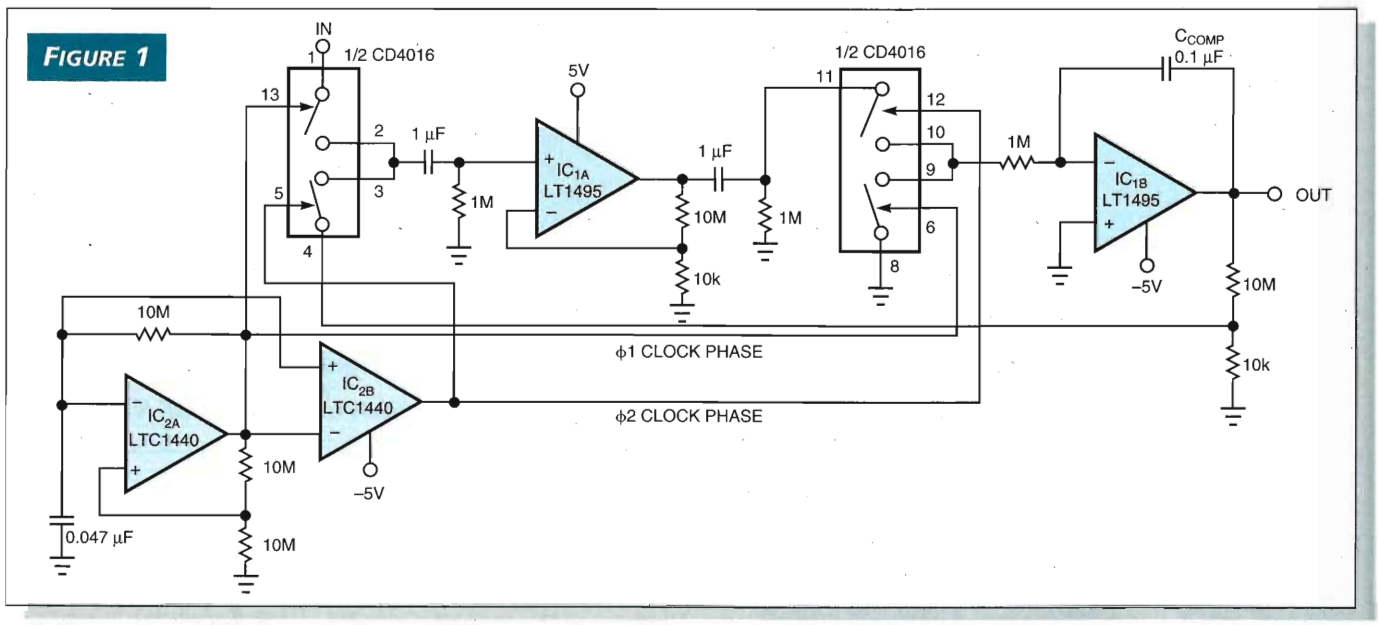
Micropower comparators $IC_{2A}$ and $IC_{2B}$ form a biphase 5-Hz clock. This clock drives the input-related switches, causing an amplitude-modulated version of the dc input to appear at $IC_{1A}$'s input. AC-coupled $IC_{1A}$ has a gain of 1000, and its output drives a switched demodulator that's similar to the modulator.

The demodulator output, a reconstructed, dc-amplified version of the circuit's input, drives a dc-gain stage, $IC_{1B}$. $IC_{1B}$'s output feeds back through gain-setting resistors to the input modulator, closing the feedback loop around the entire amplifier. The ratio of the feedback resistors, which in this case is 1000, sets the configuration's dc gain.

The circuit's internal ac coupling prevents $IC_1$'s dc characteristics from influencing overall dc performance, which results in the extremely low offset drift. The high open-loop gain permits 10-ppm gain accuracy at a closed-loop gain of 1000.

The desired micropower operation and $IC_1$'s bandwidth dictate the 5-Hz clock rate, so the resultant overall bandwidth is low. Full-power bandwidth is 0.05 Hz with a slew rate of approximately 1V/sec. Clock-related noise is about 5 μV. You can reduce this noise by increasing $C_{COMP}$, but increasing $C_{COMP}$ proportionally reduces the bandwidth. (DI #2031) EDN

**To Vote For This Design, Circle No. 318**




**This chopped amplifier features low supply current, low offset voltage and drift, and high accuracy.**

# Layout and probing techniques ensure low-noise performance

JIM WILLIAMS, LINEAR TECHNOLOGY CORP

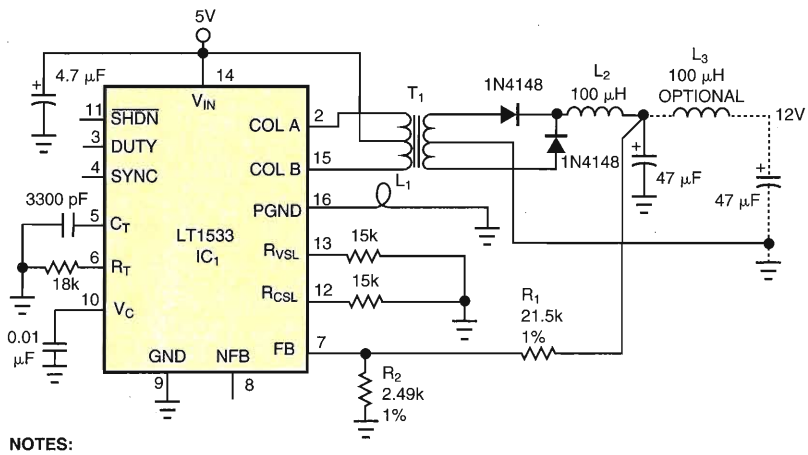
**A cavalier attitude regarding a low-noise design is a direct route to disappointment. Achieving and maintaining the low-noise potential requires judicious layout, probing, and connection techniques.**

When you think of low noise, switching regulators do not typically come to mind, but this situation is changing. A switching-regulator design can achieve low-noise performance of 100 µV (**Reference 1**). However, this low-noise switching-regulator design or any low-noise circuit doesn't achieve low-noise performance in a vacuum. You want the circuit to exhibit low noise in the real world on a real pc board with real connections to the circuit it powers and to the instruments that measure performance. Proper techniques for breadboarding, for pc-board layout, for probing, and for making valid connections are necessary to ensure the lowest possible noise.

**FIGURE 1**

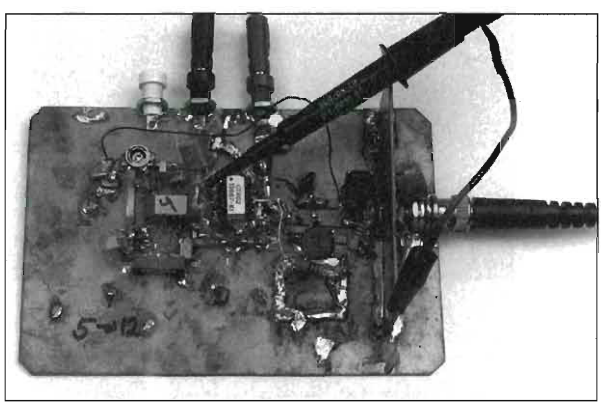
**To maintain low noise levels for the switching-regulator design (a), the breadboard (b) uses single-point ground returns. The ground plane carries no current, and the plane connects only the input common at the entry point to the board (middle banana jack). The trigger probe's ground lead can cause ground-loop-induced artifacts, which introduce serious measurement error, to appear in the display (c).**

(a)

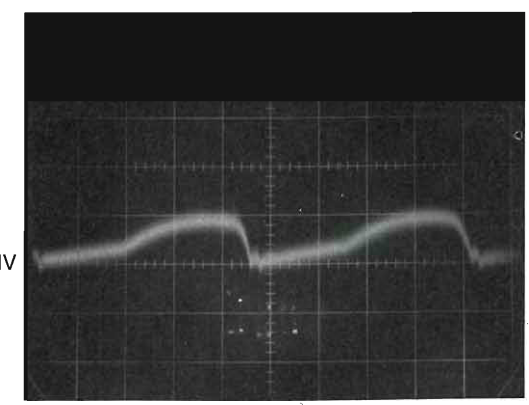



**NOTES:**
$T_1$: CTX02-13665-X1 (COILTRONICS INC, BOCA RATON, FL).
$L_1$: B-07T (COILCRAFT INC, CARY, IL), 22-nH TRACE INDUCTANCE, FERRITE BEAD (FERRONICS INC, FAIRPORT, NY) WITH ONE OR TWO TURNS OF WIRE OR FIVE TURNS OF #28 WIRE.
$L_2$, $L_3$: CTX100-3 (COILTRONICS).

(b)



(c)

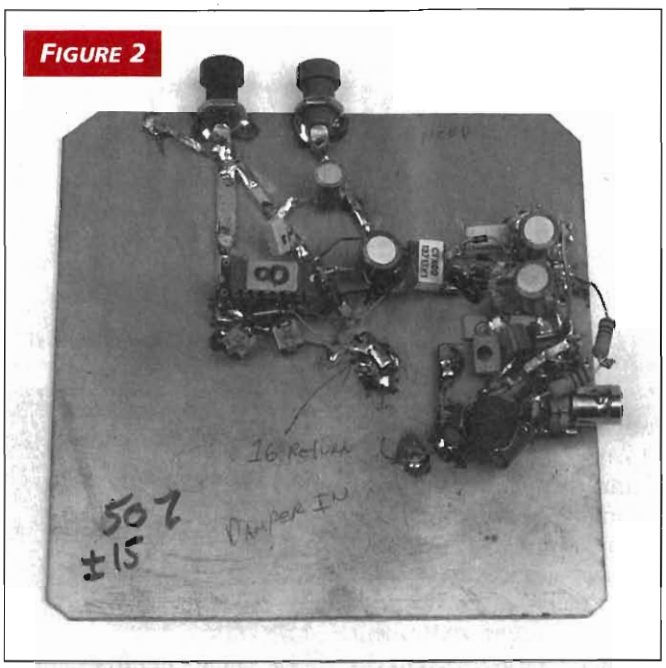


## LOW-NOISE LAYOUT, PROBING TECHNIQUES

The low harmonic content of an inherently low-noise switching regulator allows its noise performance to be less layout-sensitive than other switching regulators (**Figure 1a**). However, some prudence is in order. As in all things, a cavalier attitude is a direct route to disappointment. Obtaining the absolute lowest noise figure requires care, but you can readily achieve performance lower than 500 μV.

In general, you obtain the lowest noise by preventing the mixing of ground currents in the return path. An indiscriminate disposition of ground currents into a bus or ground plane causes such mixing, raising the observed output noise. The LT1533's restricted edge rates mitigate corrupted ground-path-induced problems, but the best noise performance occurs in a single-point ground scheme. Single-point return schemes may be impractical in production pc boards. In such cases, provide the lowest possible impedance path to the power entry point from the inductor associated with the LT1533's power ground pin (Pin 16). Locate the output-component ground returns as close as possible to the circuit load point. Minimize return-current mixing between input and output sections by restricting such mixing to the smallest possible common conductive area.

**FIGURE 2**




**A floating-output version of the basic switching regulator necessitates some minor layout changes. A separate planed area (center right) maintains low impedance between output-related return paths.**

### Control ground connections

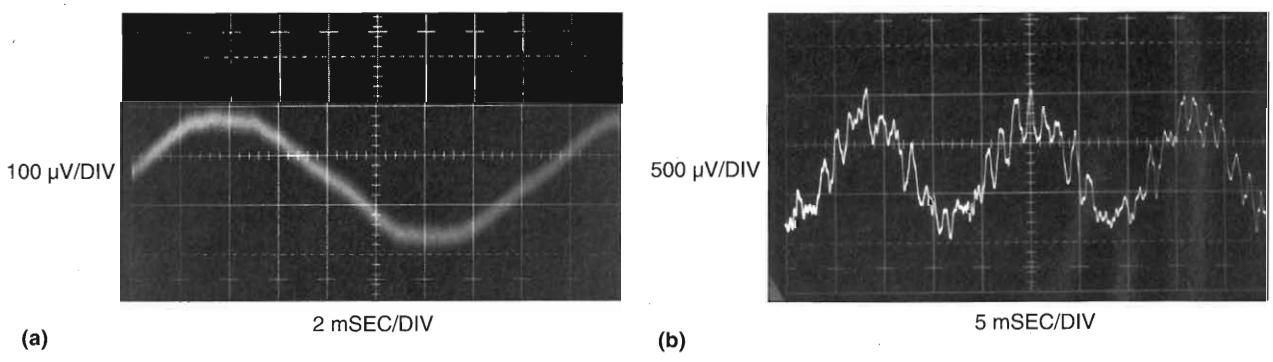
The layout of the low-noise breadboard of the switching-regulator circuit in **Figure 1** makes it fast and easy to modify in keeping with a breadboard's purpose. Single-point returns arrive separately from the output area (right side) and Pin 16 of the LT1533 IC (center left). The ground plane carries no current. The dummy load resistors do not terminate at the plane but return to the transformer's center tap. The center tap and plane separately tie into the ground system at the power-input common jack.

Layout considerations for the floating-output circuit in **Reference 1** are similar to those in **Figure 1a**, although the floating output mandates a few changes (**Figure 2**). The output load (right side, above the BNC connector) returns directly to the transformer secondary, which floats from input and plane ground potential. The main ground plane ties to the input common at the power entry port (left banana jack). The layout refers the floating-output potentials to a separate, smaller planed area (lower right), which ties to the transformer secondary center tap.

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. The low-level, wideband measurements demand care in routing signals to test instrumentation.

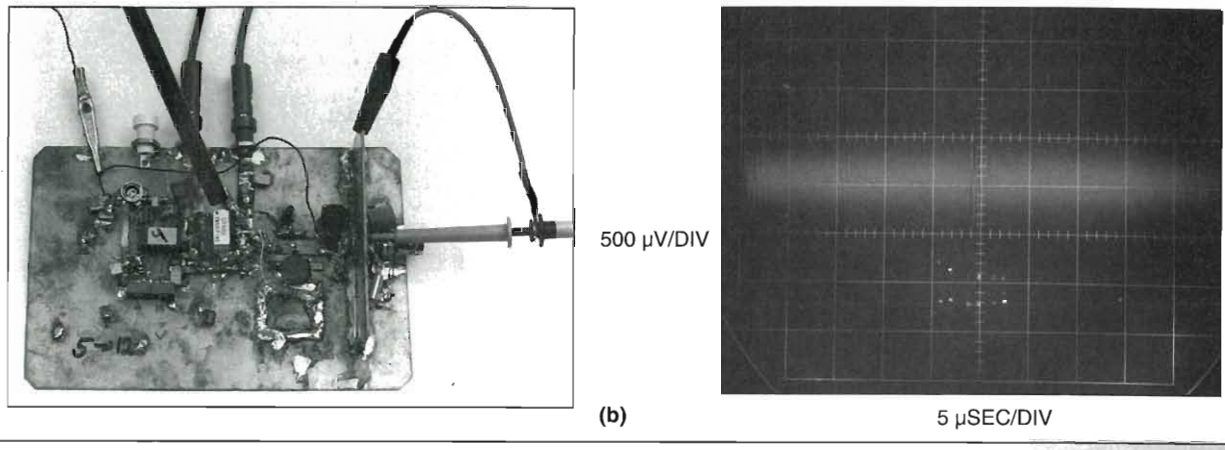
Ground loops and 60-Hz pickup are common problems. **Figure 3a** shows the effects of a ground loop between pieces of line-powered test equipment. Small current flow between the test equipment's nominally grounded chassis creates 60-

**FIGURE 3**



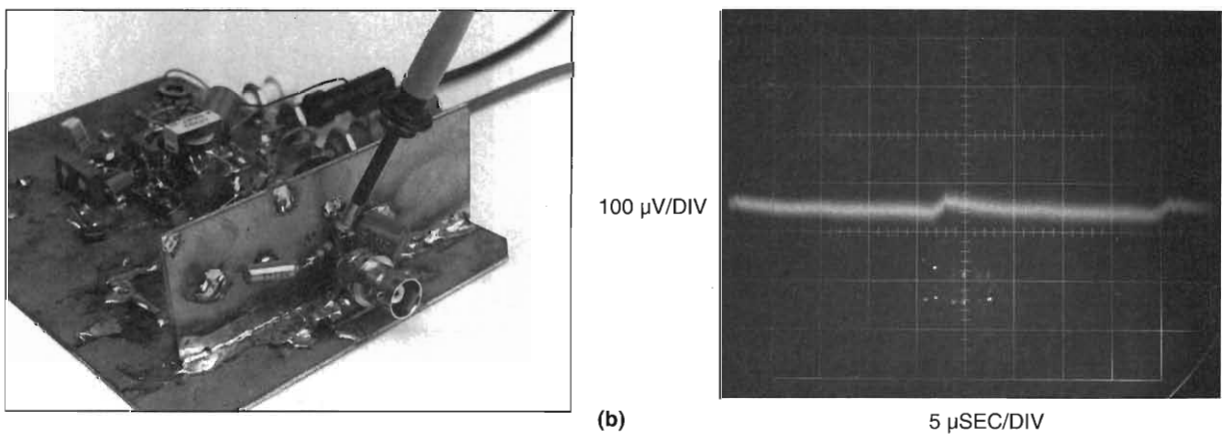

**A ground loop between pieces of test equipment induces 60-Hz display modulation (a). Excessive probe length at the feedback node causes 60-Hz pickup (b).**

FIGURE 4




**A floating trigger probe eliminates ground loops, but the output probe's ground lead (upper right) violates coaxial signal transmission (a). The result is excessive display noise (b).**

FIGURE 5




**A better probing technique uses a probe with a tip grounding attachment to approximate a coaxial connection (a). Reduced noise results, although some corruption is still evident (b).**

Hz modulation in the measured circuit output. You can avoid this problem by grounding all line-powered test equipment at the same outlet strip or by otherwise ensuring that all chassis are at the same ground potential. Similarly, you must avoid any test arrangement that permits circuit current flow in chassis interconnects. **Figure 3b** also shows 60-Hz modulation of the noise measurement. In this case, a 4-in. voltmeter probe at the feedback input is the culprit. Minimize the number of test connections to the circuit, and keep leads short.

### Avoid poor probing techniques

A short ground strap affixed to a scope probe connects to a point that provides a trigger signal for the oscilloscope (**Figure 1b**). The oscilloscope monitors circuit output noise via the coaxial cable. A ground loop on the board between the probe ground strap and the ground-referred cable shield causes apparent excessive ripple in the display (**Figure 1c**). Minimize the number of test connections to the circuit, and avoid ground loops.

You can replace the coaxial cable that transmits the circuit's output noise to the amplifier oscilloscope with a probe (**Figure 4a**); a short ground strap acts as the probe's return. This case eliminates the error-inducing trigger-channel probe of the previous case. Instead, a noninvasive isolated probe triggers the scope. The probe makes no galvanic connection to the circuit, which eliminates any possibility of a ground loop. Unfortunately, the breakup of the coaxial signal environment causes excessive display noise (**Figure 4b**). The probe's ground strap violates coaxial transmission, and RF noise corrupts the signal. To avoid the felony of violating coaxial signal transmission, maintain coaxial connec-

## LOW-NOISE LAYOUT, PROBING TECHNIQUES

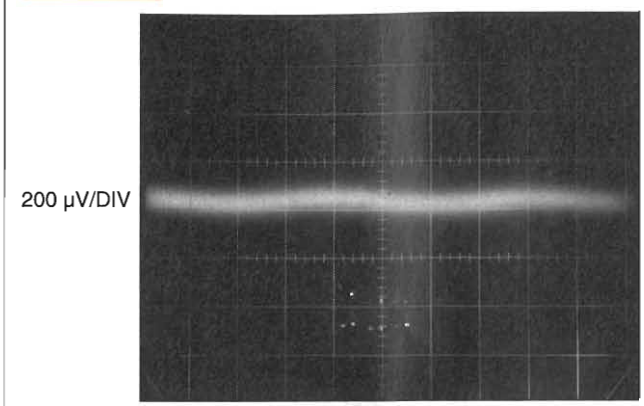
tions in the noise-signal-monitoring path.

The probe connection in **Figure 5a** also violates coaxial signal flow but to a less offensive extent—a misdemeanor. This probing setup eliminates the probe's ground strap and replaces it with a tip grounding attachment. The result (**Figure 5b**) is much better than that in **Figure 4b**, although signal corruption is still evident. Again, maintain coaxial connections in the noise-signal-monitoring path.

### Maintain coaxial connections

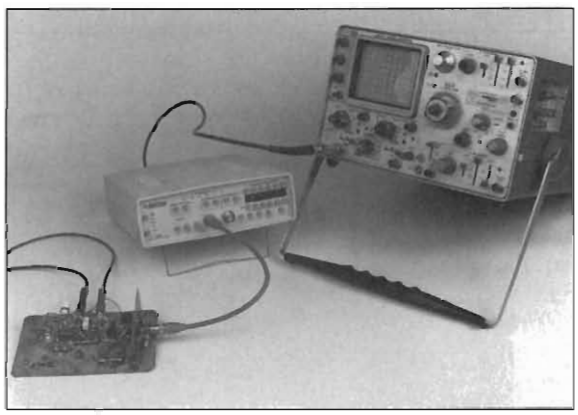
In theory, using a coaxial cable to transmit the noise signal to the amplifier-oscilloscope combination affords the highest integrity cable-signal transmission (**Figure 6a**). **Figure 6b**'s trace shows this theory to be true: The aberrations and excessive noise in **Figure 6a** have disappeared. The

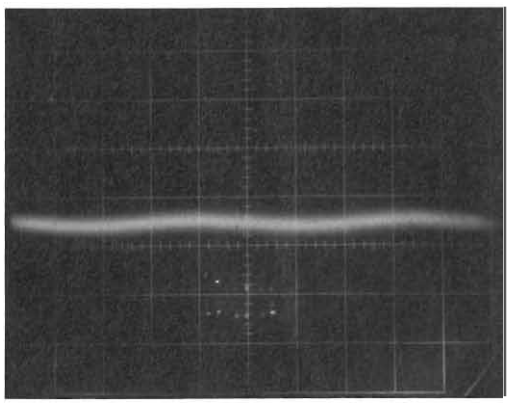
FIGURE 8




**A voltmeter lead attached to the regulator's output introduces RF pickup, multiplying the apparent noise floor.**

FIGURE 6

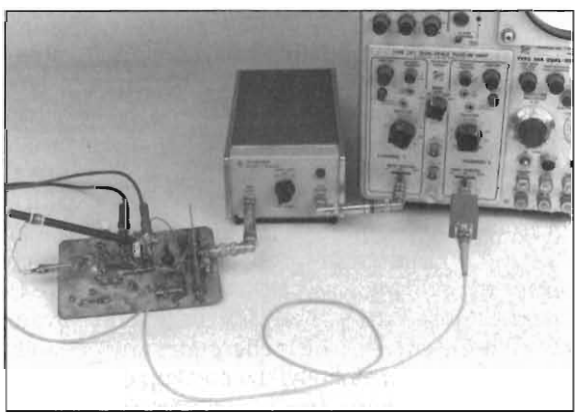

(a)

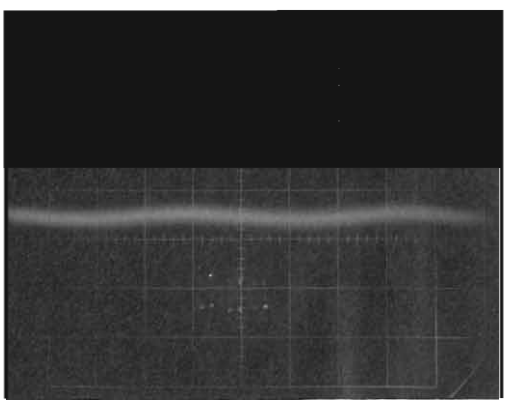


(b)

**Coaxial connections throughout the test setup (a) theoretically afford signal transmission with the highest fidelity, and real measurements agree with this theory (b). The switching residuals are faint outlines in the amplifier noise.**

FIGURE 7


(a)



(b)

**A direct connection to the test equipment (a) eliminates any possible cable-termination parasitics (b), providing signal transmission identical to that in the cable termination approach of Figure 6b.**

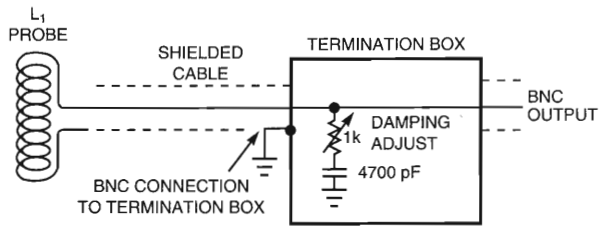
## LOW-NOISE LAYOUT, PROBING TECHNIQUES

switching residuals are now faintly outlined in the amplifier noise floor. Once again, maintain coaxial connections in the noise-signal-monitoring path.

One way to verify that no cable-based errors exist is to eliminate all cables between the breadboard, amplifier, and oscilloscope (**Figure 7a**). The result (**Figure 7b**) is indistinguishable from that of **Figure 6b**, indicating no cable-introduced infidelity. When results seem optimal, design an experiment to test them. Whether results of this experiment are as expected or poor, design another experiment to test them.

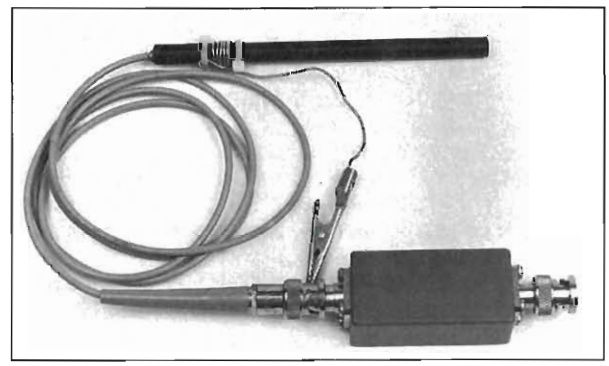
In theory, attaching a voltmeter lead to the regulator's output should introduce no noise. However, an increased noise reading under this condition contradicts the theory (**Figure 8**). The regulator's output impedance, albeit low, is not zero, especially as the frequency scales up. The RF noise that the test lead injects works against the finite-output impedance to produce the 200-μV noise in the **figure**. If you must connect a voltmeter to the output during testing, provide the connection through a 10-kΩ to 10-μF filter. This network eliminates the problem and introduces minimal

**FIGURE 9**




NOTE: $L_1$: JW MILLER #100267.

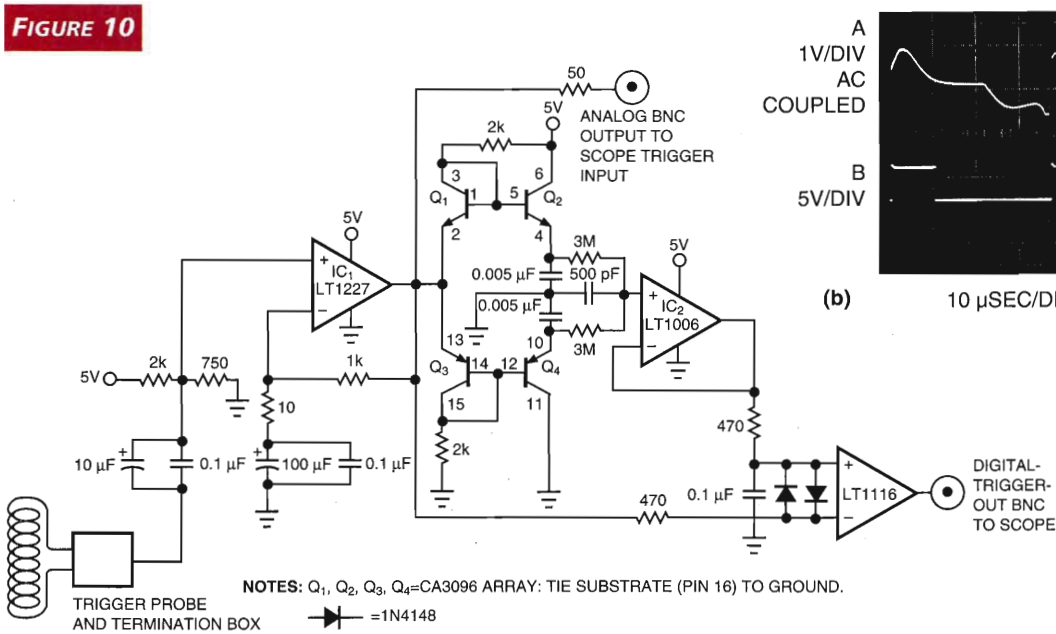
(a)



(b)

**A simple trigger probe (a, b) eliminates board-level ground loops. The components in the termination box provide damping for $L_1$'s ringing response.**

**FIGURE 10**




NOTES: $Q_1$, $Q_2$, $Q_3$, $Q_4$=CA3096 ARRAY: TIE SUBSTRATE (PIN 16) TO GROUND.
=1N4148

(a)




(b) 10 μSEC/DIV (UNCALIBRATED)

**A trigger-probe amplifier (a) is useful when small magnetic fields are unable to reliably trigger the oscilloscope. This design has both an analog (b, Trace A) and digital output (b, Trace B) and maintains the digital output over 50-to-1 probe-signal variations.**

error in the monitoring DVM. Minimize the number of test-lead connections to the circuit while checking noise. Prevent test leads from injecting RF into the test circuit.

### Use an isolated trigger probe

The isolated trigger probe in **Figure 4** is simply an RF choke terminated against ringing (**Figure 9**). The choke picks up a residual radiated field, generating an isolated trigger signal. This arrangement furnishes a scope-trigger signal essentially without measurement corruption. For good results, adjust the termination for minimum ringing while preserving the highest possible amplitude output. Light compensatory damping produces a signal with high-amplitude ringing, which causes poor scope triggering. Proper adjustment results in a more favorable output, characterized by minimal ringing and well-defined edges.

The field around the switching magnetic components is small and may be inadequate for reliably triggering some oscilloscopes. In such cases, a trigger-probe amplifier is useful (**Figure 10a**). This amplifier uses an adaptive triggering scheme to compensate for variations in probe-output amplitude. A stable 5V trigger output is maintained over a 50-to-1 probe-output range.

$IC_1$, operating at a gain of 100, provides wideband ac gain. The output of this ×100 stage (**Figure 10b, Trace A**) biases a two-way peak detector, comprising $Q_1$ through $Q_4$. $Q_2$'s emitter capacitor stores the maximum peak, and $Q_4$'s emitter capacitor retains the minimum excursion. The dc value of the midpoint of $IC_1$'s output signal appears at the junction of the 500-pF capacitor and the 3-MΩ resistors. This point always sits midway between the signal's excursions, regardless of absolute amplitude.

$IC_2$ buffers this signal-adaptive voltage to set the trigger voltage at the LT1116's positive input. $IC_1$'s output directly biases the LT1116's negative input. Signal-amplitude variations of greater than 50-to-1 do not affect the LT1116's output, which is the circuit's trigger output (**Figure 10b, Trace B**). EDN

## Reference

1. "Switching-regulator design lowers noise to 100 μV," *EDN*, Dec 4, 1997, pg 151.

## Author's biography

*Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

By Jim Williams, Linear Technology

**ACCURATELY MEASURING THE SETTLING TIME OF A 16-BIT DAC AND ITS OUTPUT AMPLIFIER IS AN ART FORM. ONE MEASUREMENT TECHNIQUE BORROWS FROM THE DESIGN OF A CLASSIC SAMPLING OSCILLOSCOPE AND PROVIDES RELIABLE RESULTS. THREE OTHER MEASUREMENT APPROACHES PRODUCE RESULTS THAT CLOSELY AGREE WITH EACH OTHER.**

# Measuring 16-bit settling times: the art of timely accuracy

INSTRUMENTATION, WAVEFORM GENERATION, data acquisition, feedback-control systems, and other applications are beginning to make use of 16-bit data converters, specifically 16-bit DACs. By providing 16-bit performance at a lower cost than previous modular and hybrid technologies, new ICs make 16-bit DACs a practical design alternative. With the increasing use of these high-resolution devices comes an increasing need for techniques that accurately and reliably measure performance.

A DAC's dc specifications are relatively easy to verify; the measurement techniques are well-understood, although they are often tedious. The ac specifications, however, require more sophisticated approaches to produce reliable information. In particular, the settling time of a DAC and its output amplifier is extraordinarily difficult to determine to 16-bit resolution.

DAC settling time is the elapsed time from the input-code application until the output arrives at and remains within a specified error band around the final value. Manufacturers usually specify the settling time for a full-scale 10V transition. DAC settling time has three distinct components: During delay time, which is very small and almost entirely due to propagation delay through the DAC and output amplifier, there is no output movement; during slew time, the output amplifier moves at its highest possible speed toward the final value; and during ring time, the amplifier recovers from slewing and ceases movement within some defined error band (**Figure 1**). Normally, there is a trade-off between slew and ring time. Fast-slewing amplifiers generally have extended ring times, which complicate amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs that degrade dc error terms (see **sidebar** "Practical considerations for DAC-amplifier compensation").

It is difficult to measure to 16-bit (≈0.0015%) accuracy regardless of the speed of what you are measuring. Dynamic measurement to 16-bit resolution is particularly challenging, and even more so if you use specialized components (see **sidebar** "Measuring the settling time of chopper-stabilized amplifiers"). A reliable 16-bit settling-time measurement requires exceptional care in your experimental technique. Accurate 16-bit results require careful attention to breadboarding, layout, and connection techniques. Wideband 100-μV-resolution measurements do not tolerate a cavalier laboratory attitude (**Reference 1**).

## COMMON APPROACH OVERDRIVES OSCILLOSCOPE

A common circuit that you use to measure DAC settling time employs the "false-sum-node" technique (**Figure 2**). The resistors and DAC amplifier form a

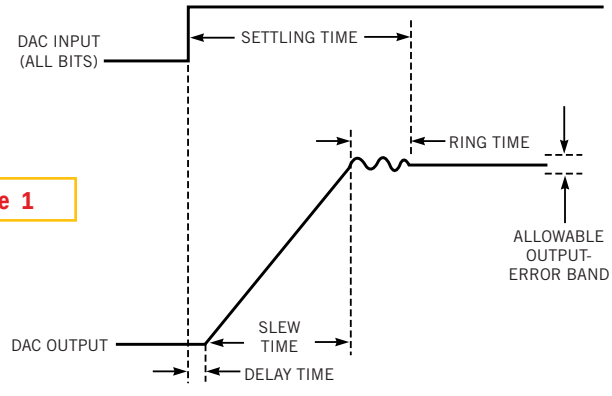



Figure 1

**DAC-settling-time components include delay, slew, and ring times. Fast amplifiers reduce slew time, although longer ring time usually results.**

bridge-type network. Assuming ideal resistors, the amplifier output steps to the value of $V_{IN}$ when the DAC inputs move to all ones. During the slew time, the diodes bound the settle node, which limits the voltage excursion. When settling occurs, the oscilloscope probe's voltage should be zero. The resistor divider's attenuation means that the probe's output equals one-half of the actual settled voltage.

In theory, this circuit allows you to observe the settling to small amplitudes. In practice, this circuit does not reliably produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, ac loading of the resistor junction influences the observed settling waveforms. A 10-pF probe alleviates this problem, but its 10× attenuation sacrifices oscilloscope gain. 1× probes are unsuitable because of their excessive input capacitance. An active 1× FET probe works, but another issue remains. The clamp diodes at the settle node reduce swing during amplifier slew time and thereby prevent excessive oscilloscope overdrive. Unfortunately, overdrive-recovery characteristics vary among oscilloscopes, and vendors do not usually specify these characteristics (see **sidebar** "Evaluating oscilloscope-overdrive performance"). The Schottky diodes' 400-mV drop means that the oscilloscope may see an unacceptable overload and display questionable results.

At 10-bit resolution—10 mV at the DAC output or 5 mV at the oscilloscope—the oscilloscope typically undergoes a 2× overdrive at 50 mV/div, and the desired 5-mV baseline is barely discernible. At 12-bit or higher resolution, making a valid measurement using the circuit in **Figure 2** is hopeless. Increasing oscilloscope gain increases the measurement's vulnerability to overdrive-induced errors. At 16 bits, there is no chance of measurement integrity. Thus, measuring a 16-bit settling time requires a high-gain oscilloscope that is

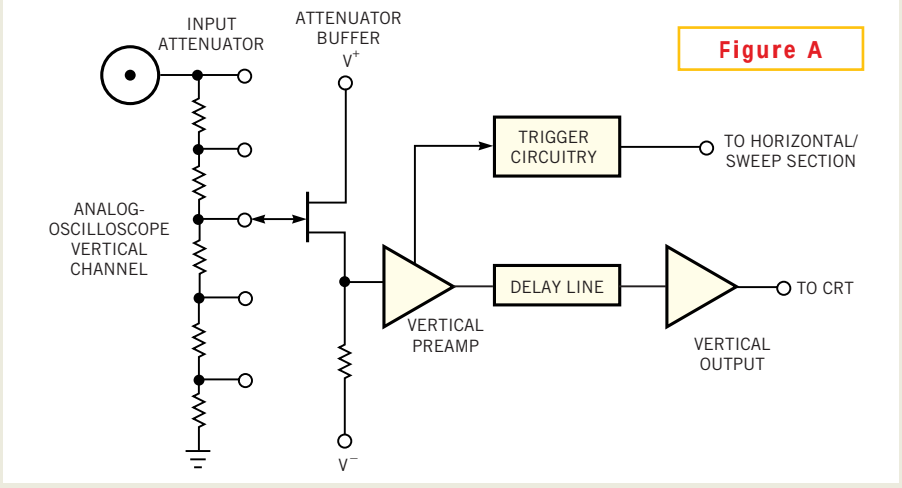
## EVALUATING OSCILLOSCOPE-OVERDRIVE PERFORMANCE

The design of most of the settling-time circuits in this article attempts to provide the monitoring oscilloscope with little or no overdrive. Oscilloscope recovery from overdrive is a gray area that manufacturers almost never specify. One settling-time-measurement method requires overdriving the oscilloscope. In this case, the oscilloscope must supply an accurate waveform after the measurement circuit drives the display off screen.

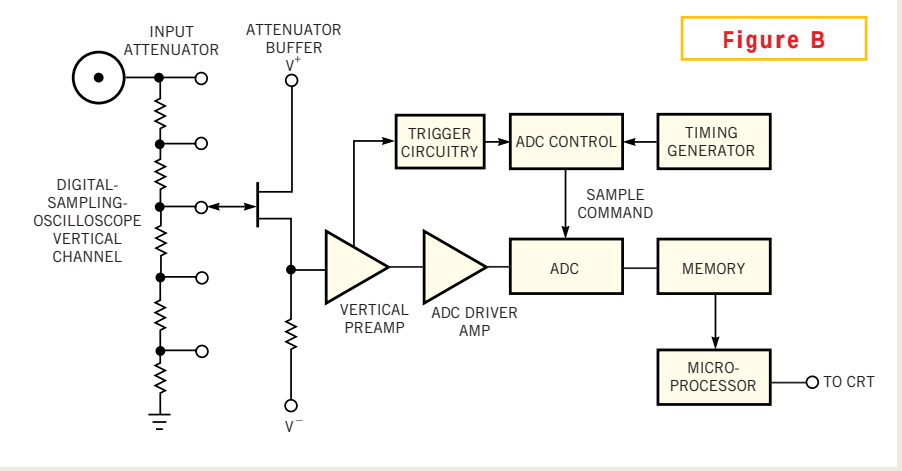
The answer to how long you must wait after an overdrive before taking the display seriously is quite complex. Factors involved in determining this duration include the degree of overdrive, its duty cycle, and its magnitude in time and amplitude.

Response to overdrive varies widely among oscilloscopes. For example, the recovery time for a 100× overload at 0.005V/div may be very different from the recovery time at 0.1V/div. The recovery characteristic may also vary with waveform shape, dc content, and repetition rate. With so many variables, you must cautiously approach measurements that involve oscilloscope overdrive.

To determine why most oscilloscopes have trouble recovering from overdrive, study the vertical paths of the three basic oscilloscopes: analog, digital, and classic sampling oscilloscopes. Analog and digital scopes are susceptible to overdrive; the classic




**When you overdrive an analog oscilloscope, the attenuator buffer, preamp, and vertical output amplifier can saturate. Full recovery can take a surprisingly long time.**




**The linear front end of a digital sampling oscilloscope can saturate in the same way an analog scope does, causing similar overdrive-recovery problems.**

somehow immune to overdrive. You can address the gain issue with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

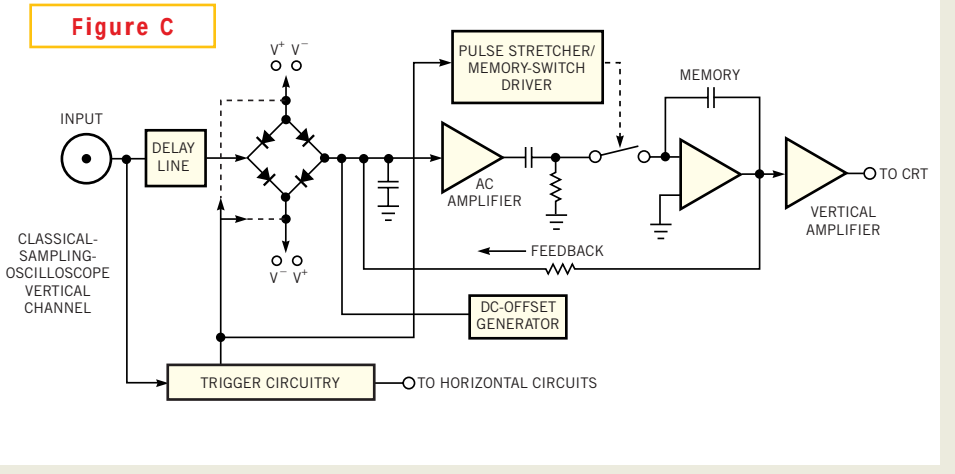
The only oscilloscope technology that offers inherent overdrive immunity is the classic sampling scope. Do not confuse this scope with modern-era digital sampling scopes, which have overdrive restrictions. Unfortunately, vendors no longer manufacture these classic instruments, but you can still find them on the secondary market. It is possible, however, to construct a circuit that borrows the overload advantages of classic-sampling-scope technology. Additionally, you can endow the circuit with features that are particularly suitable for measuring 16-bit-DAC settling times.

## A PRACTICAL SETTLING-TIME MEASUREMENT

A block diagram of a 16-bit-DAC settling-time-measurement circuit (**Figure 3**) shares some attributes with the circuit in **Figure 2**. The same pulse that controls the DAC also triggers a delayed-pulse generator, which consists of independently variable delay and pulse-generator blocks. The output of this generator determines the state of a diode-bridge switch. You adjust the delayed-pulse generator's timing so that the switch does not close until settling is nearly complete. The circuit samples both the amplitude and the time of the incoming waveform. This scheme never subjects the oscilloscope to overdrive; no off-screen activity ever occurs. Before applying the input step to the oscilloscope, the circuit inserts a time-correction delay to compensate for the propagation delay of the settling-time-measurement path.

The diode-bridge switch is the key to the measurement. Borrowed from classic-sampling-oscilloscope circuitry, this switch connects the preamplified oscilloscope to the settle point. The diode bridge's inherent balance eliminates charge-injection-

Figure C




**The classic sampling oscilloscope is inherently immune to overload because the instrument samples the input *before* providing any gain.**

sampling scope is the only architecture that is inherently immune to overdrive.

An analog oscilloscope is a real-time, continuous linear system (**Figure A**). The input drives an attenuator, and a wideband buffer unloads the attenuator output. The vertical preamp provides gain and drives the trigger pickoff, delay line, and vertical output amplifier. The attenuator and delay line are passive elements and require little comment.

The buffer, preamp, and vertical output amplifier are complex, linear gain blocks, each with dynamic operating-range restrictions. Additionally, inherent circuit balance, low-frequency stabilization paths, or both can set each block's operating point. Overdriving the input can cause one or more of these stages to saturate, forcing internal nodes and components to abnormal operating points and temperatures. When the overload ceases, full recovery of the electronic and thermal time constants may take a surprisingly long time.

The digital sampling oscilloscope eliminates the vertical output amplifier but has an attenuator buffer and amplifiers ahead of the A/D converter (**Figure B**). The digital scope is also susceptible to overdrive-recovery problems.

## INSTRUMENT HAS INHERENT IMMUNITY

The classic sampling oscilloscope is unique; the nature of its operation makes it inherently immune to overload (**Figure C**). The classic scope samples the input before taking any gain. Unlike **Figure B**'s digital sampling scope, the input is fully passive to the sampling point. Additionally, the output feeds back to the sampling bridge, which maintains its operating point over a range of inputs. The dynamic swing available to maintain the bridge output is large and easily accommodates a range of oscilloscope inputs.

For all of these reasons, the amplifiers in the classic scope see no overload (even at 1000× overdrives) and exhibit no recovery problems. You can derive additional immunity from the instrument's relatively slow sample rate; even if you overload these amplifiers, they have plenty of time to recover between samples.

The designers of classic sampling scopes capitalized on the scope's overdrive immunity by including variable dc-offset generators to bias the feedback loop. These generators permit you to offset a large input so that you can accurately observe small amplitude activity on top of the signal. This feature is ideal for settling-time measurements. Unfortunately, manufacturers no longer produce classic sampling oscilloscopes; if you have one, take care of it.

Don't despair if you don't have access to a classic sampling scope. Although analog and digital oscilloscopes are susceptible to overdrive, many tolerate some degree of overdrive abuse. A simple test indicates when and if overdrive deleteriously affects the oscilloscope. See **Reference A** for more information.

## REFERENCE

A. Williams, Jim, "High-speed amplifier techniques," Application Note 47, Linear Technology Corp, 1991.

based errors in the output, making the bridge far superior to other electronic switches. Any other high-speed-switch technology contributes excessive output spikes caused by charge-based feedthrough. A FET switch is unsuitable because its gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt the oscilloscope display, inducing overload and defeating the switch's purpose.

The diode bridge's balance combines with matched, low-capacitance monolithic diodes and complementary high-speed switching to yield a cleanly switched output. The scheme also controls the temperature of the monolithic-diode bridge to provide a bridge offset error of less than 10 μV, which stabilizes the measurement baseline. Uncommitted diodes in the monolithic array implement the temperature control.

A more detailed view of the bridge circuitry reveals how the bridge diodes cancel each other's temperature coefficients (**Figure 4**). Unstabilized bridge drift is about 100 μV/°C, and the temperature control reduces residual drift to a few microvolts per degrees Celsius. To achieve temperature control, one diode acts as a sensor. Another diode, running in reverse breakdown ($V_Z \approx 7V$), serves as the heater. The control amplifier, which compares the sensor diode's voltage with a voltage at the amplifier's negative terminal, drives the heater diode to stabilize the temperature of the array.

The circuit achieves dc balance by trimming the bridge's on-current for zero offset voltage between the input and output. Two ac trims are necessary: The ac-balance trim corrects for diode and layout capacitive imbalances, and the skew-compensation trim corrects timing asymmetry in the nominally complementary bridge drive. These ac trims compensate small dynamic imbalances that could result in parasitic bridge outputs.

### DETAILED CIRCUIT INCLUDES SAMPLING BRIDGE

The detailed schematic of the 16-bit-DAC settling-time-measurement circuit closely follows the block diagram (**Figure 5**). The input pulse simultaneously switches all of the DAC bits; the pulse also routes

## PRACTICAL CONSIDERATIONS FOR DAC-AMPLIFIER COMPENSATION

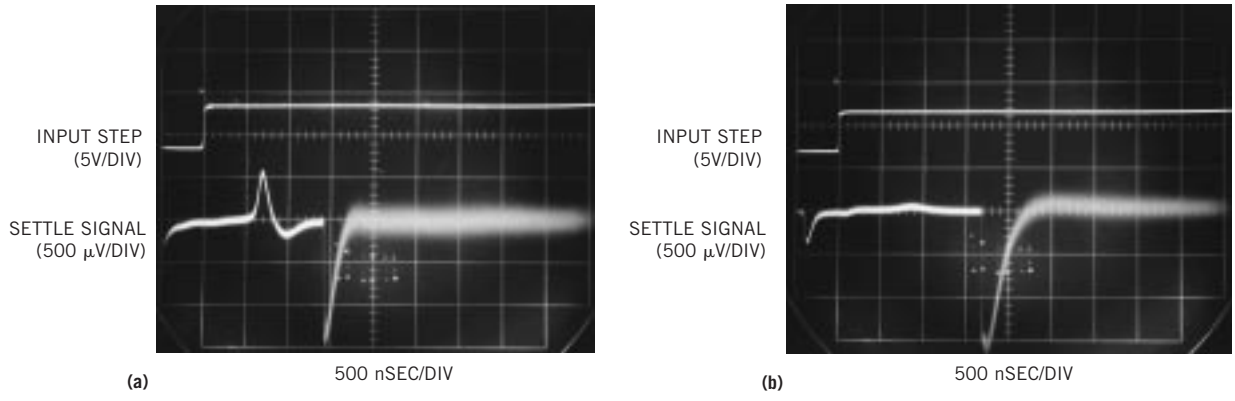
There are a number of practical considerations when compensating the DAC-amplifier pair to get the fastest settling time. As this article discusses, settling-time components include delay, slew, and ring times. Delay is due to the propagation time through the DAC amplifier and is a small term. The amplifier's maximum speed sets the slew time. Ring time is the time during which the amplifier recovers from slewing and ceases movement within some defined error band.

Once you choose a DAC-amplifier pair, only the ring time is readily adjustable. Because slew time is usually the dominant lag, it is tempting to select the amplifier with the fastest available slew time to obtain the best settling. Unfortunately, fast-slewing amplifiers usually have extended ring times, negating their brute-force speed advantage. Invariably, the penalty for raw speed is prolonged ringing, which you can damp using only large compensation capacitors. This compensation works, but it results in protracted settling times.

The key to good settling times is to choose an amplifier with the right balance of slew-rate and recovery characteristics and to compensate the amplifier properly. Achieving this design goal is harder than it sounds because you can neither predict nor extrapolate an amplifier's settling time from any combination of data-sheet specifications. You must measure the settling time in the intended configuration.

In the case of a DAC and its amplifier, a number of terms combine to influence settling time. These terms include amplifier slew rate and ac dynamics, DAC output resistance and capacitance, and the compensation capacitor. These terms interact in a complex manner, making predictions hazardous. Take notice, Spice aficionados: If you eliminate the DAC's parasitic elements and replace them with a pure resistive source, amplifier settling time is still not readily predictable. The DAC's output-

**Figure A**



to the oscilloscope via a delay-compensation network. This delay network, comprising CMOS inverters and an adjustable RC network, compensates the oscilloscope's input-step signal for the 12-nsec delay through the circuit's measurement path (**Reference 1**).

The circuit uses the 3-kΩ resistor ratio set to algebraically sum the opposing DAC amplifier, and it uses LT1236 reference currents to produce a 0V reading when the circuit settles. The LT1236 also furnishes the DAC's reference, making the measurement ratiometric. $IC_1$ unloads the clamped settle node and drives the sampling bridge. The additional clamp diodes at $IC_1$'s output prevent abnormal $IC_1$ outputs from damaging the diode array, which can happen because of a lost supply or supply-sequencing anomalies. (I became unfit for human companionship when I discovered this mishap. Replacing the sampling bridge was a lengthy and highly emotionally charged task that required an exhaustive breadboarding exercise. See **Reference 1.**) $IC_3$ and associated components provide temperature control for the sampling diode bridge by comparing the forward drop of the diode at pin 12 of the array with a stable potential derived from the −5V regulator. The diode at pin 14 serves as a chip heater. These pin connections provide the best temperature-control performance.

The input pulse also triggers the 74-HC123 one shot, which produces a delayed pulse that sets the diode bridge on time. The 20-kΩ potentiometer sets the delay, and the 5-kΩ potentiometer sets the pulse width. If you appropriately set the delay, the oscilloscope does not see any input until settling is nearly complete, eliminating overdrive to the scope. You need to adjust the sample-window width so that you can observe all remaining settling activity. In this way, the oscilloscope's output is reliable, and you can observe meaningful data. $Q_1$ through $Q_4$ shift the level of the one shot's output to provide the bridge with a complementary switching drive. The switching transistors ($Q_1$ and $Q_2$) are UHF types; they permit true differential bridge switching with less than 1 nsec of time skew.

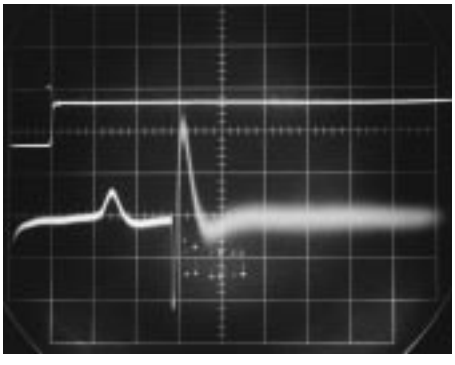
impedance terms make this difficult problem even more messy.

The only way to deal with these problems is to use the feedback compensation capacitor, $C_F$. $C_F$ rolls off amplifier gain at the frequency that permits the best dynamic response. Normally, the DAC's current output unloads directly into the amplifier's summing junction, placing the DAC's parasitic capacitance between ground and the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to "hunt" and ring around the final value before settling. Different DACs have different output-capacitance values. CMOS DACs have the highest output capacitance, typically 100 pF. This value varies with code.

You can achieve the best settling results by selecting the compensation capacitor to functionally compensate for all of the mentioned parasitics. **Figure Aa** shows results for an optimally selected feedback capacitor. The amplifier comes cleanly out of slew and settles quickly.

In **Figure Ab**, the feedback capacitor is too large. Settling is smooth, although overdamped, and a 600-nsec penalty results. **Figure Ac**'s feedback capacitor is too small, causing a somewhat underdamped response and resulting in excessive ring-time excursions. In both cases, settling time increases from 1.7 to 2.3 μsec.

When you individually trim the feedback capacitor for optimal response, the DAC, amplifier, and compensation-capacitor tolerances are irrelevant. If you don't use individual trimming, you must consider these tolerances when determining the feedback capacitor's production value. DAC capacitance and resistance, as well as the feedback capacitor's value, affect the ring time. The relationship is nonlinear, although some guidelines are possible. The DAC-impedance terms can vary by ±50%, and the feedback capacitor is typically a ±5% component. Additionally, the data sheet states that amplifier slew rate has a significant tolerance. To obtain a production feedback-capacitor value, determine the optimum value by individually trimming components on the production-board layout. (Board-layout parasitic capacitance counts, too.) Then, factor in the worst-case percentage values for DAC-impedance terms, slew rate, and feedback-capacitor tolerance. Add these values to the trimmed capacitor's measured value to obtain the production value. This budgeting is perhaps unduly pessimistic, but it will keep you out of trouble. (Summing the rms error may be a defensible compromise, but this method's potential problems become clear when you are sitting in an airliner that is landing in a snowstorm.)




**An optimal value of $C_F$ compensates for all DAC parasitics and results in the fastest settling time of 1.7 μsec (a). Increasing the capacitor's value produces an overdamped response with no ringing, but settling time increases to 2.3 μsec (b). An undersized capacitor produces an underdamped response with additional ringing that also results in a longer settling time of 2.3 μsec (c).**

The residue amplifier ($IC_2$) monitors the bridge's output, provides gain, and drives the oscilloscope. **Figure 6** shows circuit waveforms. When the sample gate goes low, the bridge switches cleanly, and you can easily observe the last 1.5 mV of slew. Ring time is also clearly visible, and the amplifier settles nicely to its final value. When the sample gate goes high, the bridge switches off, with only 600 μV of feedthrough. The 100-μV peak before bridge switching (at ≈3.5 vertical divisions) is evidence of feedthrough from $IC_1$'s output, but the circuit controls this feedthrough to keep all activity on screen. No off-screen activity occurs at any time; the circuit never subjects the oscilloscope to overdrive.

The circuit requires trimming to achieve this level of performance. Grounding $Q_5$'s base before applying power sets the bridge's temperature-control point. Next, apply power and measure $IC_3$'s positive input with respect to the −5V rail. Select the resistor at $IC_3$'s negative input, which is nominally 1.5 kΩ, for a voltage at $IC_3$'s negative input that is 57 mV less than the positive input's value. As before, adjust $IC_3$'s nega-

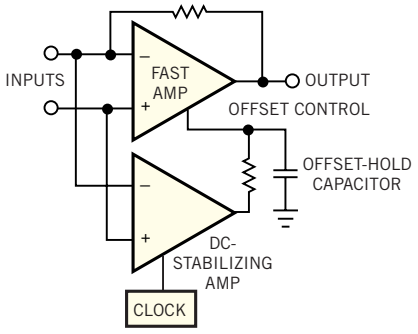
## MEASURING THE SETTLING TIME OF CHOPPER-STABILIZED AMPLIFIERS

Determining the settling time of chopper-stabilized amplifiers is a special case and requires some understanding of how these amplifiers work. **Figure A** is a simplified block diagram of the LTC1150 CMOS chopper-stabilized amplifier, which actually includes two amplifiers. The "fast amp" processes input signals directly to the output. This amplifier is relatively quick, but it has poor dc-offset characteristics. A second, clocked amplifier periodically samples the offset of the fast channel and maintains an offset-hold capacitor at whatever value is necessary to correct the fast amplifier's offset errors. The circuit clocks the dc-stabilizing amplifier so that it operates (internally) as an ac amplifier, eliminating its dc terms as an error source. The clock chops the stabilizing amplifier at about 500 Hz, providing the hold-capacitor-offset control with updates every 2 msec.

The settling time of this composite amplifier is a function of the response of the fast and stabilizing paths. **Figure Ba** shows short-term settling of the amplifier. Damping is reasonable, and the 10-μsec settling time and profile appear typical. **Figure Bb** reveals an unpleasant surprise. If the DAC's slew-time interval coincides with the amplifier's sampling cycle, serious error results. In **Figure Bb**, the horizontal scale is slow. Initially, the amplifier quickly settles (settling is visible in the second vertical-division region), but it generates a huge error 200 μsec later, when the internal clock applies an offset correction. Successive clock cycles progressively chop the error into the noise, but a complete recovery takes 7 msec.

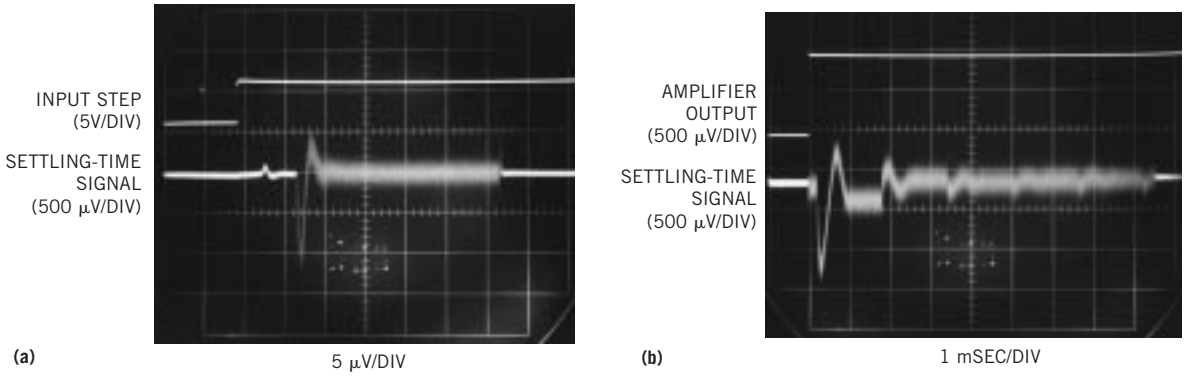
The error occurs because the amplifier samples its offset when its input signal is well outside its bandpass. This set of events causes the stabilizing amplifier to acquire erroneous offset information. When the amplifier applies the "correction," a huge output error results. Admittedly, this error is a worst-case scenario; it can happen only if the DAC's slew-time interval coincides with the amplifier's internal clock cycle—but it can happen.

Figure A




**An LTC1150 CMOS chopper-stabilized amplifier comprises a fast amp, which processes signals directly to the output, and a dc-stabilizing amp, which periodically samples the offset of the fast amp and maintains its output-hold capacitor at a value that minimizes offset errors.**

Figure B




**The short-term settling profile of the chopper-stabilized amplifier seems typical at approximately 10 μsec (a). Unfortunately, slowing the horizontal sweep reveals a monstrous tailing error, which occurs when the amplifier's clocked operation coincides with DAC slewing (b).**

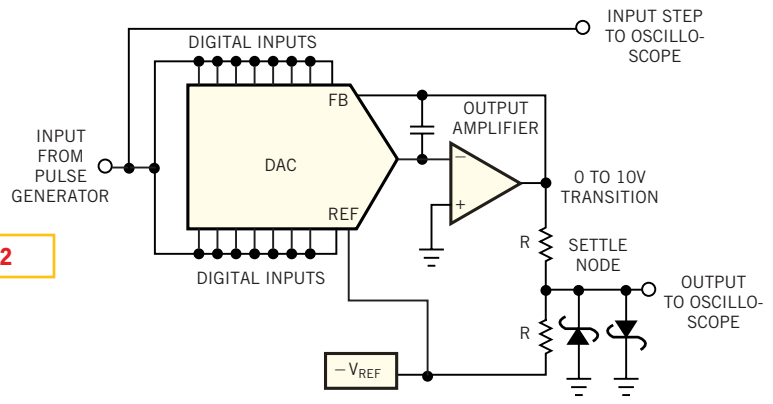
tive input with respect to −5V. Remove ground from $Q_5$'s base, and the circuit will control the sampling bridge to about 55°C according to the following equation:

$$25\ C\ (ROOM) + \frac{57\ mV}{1.9\ mV/\ C\ (DIODE\ DROP)} = 25\ C + 30\ C\ (RISE) = 55\ C.$$

You set the dc and ac bridge trims—baseline zero, ac balance, and skew compensation—when the temperature control is functional. To make these adjustments, disable the DAC and its amplifier by disconnecting the input pulse from the DAC, setting all DAC inputs low, and shorting the settle node directly to the ground plane. When the switching-related activity is on-screen and the offset error reduces to an unreadable level, the circuit is ready to use. You can remove ground from the settle node and restore the input-pulse connection to the DAC.

Beware that without proper trimming, ac and dc errors are present at the output of $IC_2$'s residue amplifier. The sample gate's transitions cause large, off-screen residue-amplifier swings, and the amplifier output shows significant dc-offset error during the sampling interval. Adjusting the ac-balance and skew-compensation potentiometers minimizes the switching-induced transients.

Figure 2




**A popular summing scheme for DAC-settling-time measurements provides misleading results because a 16-bit measurement causes greater than 200× oscilloscope overdrive, and the scope displays meaningless information.**

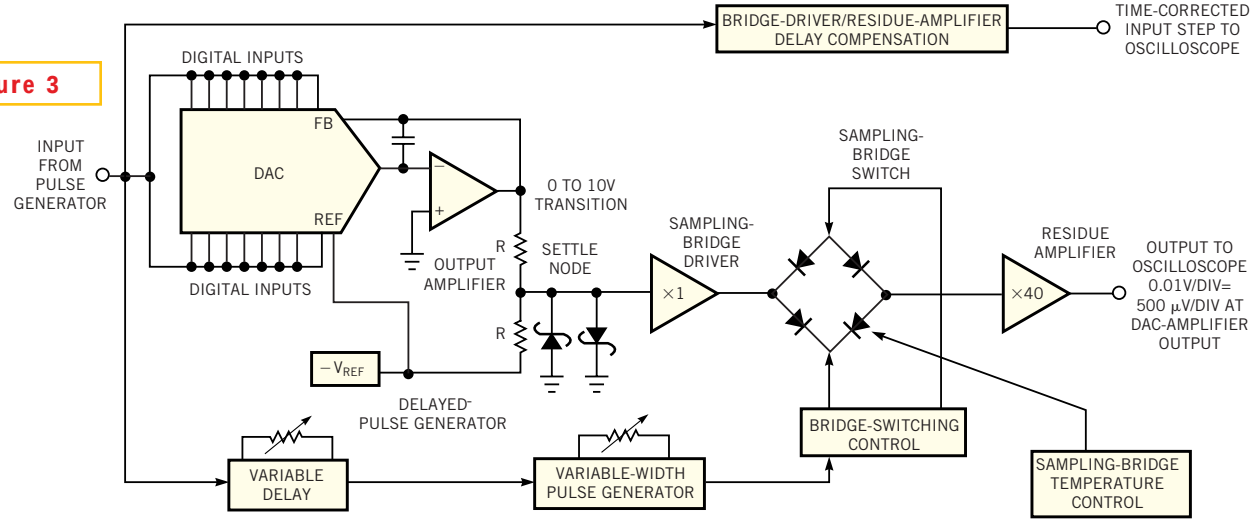
## SET SAMPLING WINDOW AND COMPENSATION

**Figure 7** underscores the importance of proper sampling-window positioning in time. In **Figure 7a**, the sample gate's delay initiates the sample window too early, and the residue amplifier's output overdrives the oscilloscope when sampling commences. **Figure 7b** displays optimal conditions, with all amplifier residue well within the screen boundaries.

In general, it is good practice to "walk" the sampling window until the last millivolt or so of the amplifier's slew time so that you can observe the onset of ring time. The sampling-based approach provides this capability, which is a powerful measurement tool. Additionally, remember that slower amplifiers may require extended delay times, extended sampling-window times, or both. These extended times may necessitate larger capacitor values in the 74H123 one-shot timing networks.

The DAC-amplifier pair requires frequency compensation to achieve the best possible settling time. The DAC has appreciable output capacitance, which complicates amplifier response and makes careful compensation-capacitor selection even more important (see **sidebar** "Practical considerations for DAC-amplifier compensation"). Light compensation permits very fast slew times but causes excessive ringing amplitude over a protracted time, which increases the total settling time. Severe ringing can feed through during a portion of the sample-gate off period, although no overdrive results. A large-value compensation capacitor eliminates all ringing but slows the amplifier and further increases settling time. A carefully chosen compensation capacitor results in tightly controlled damping.

Figure 3



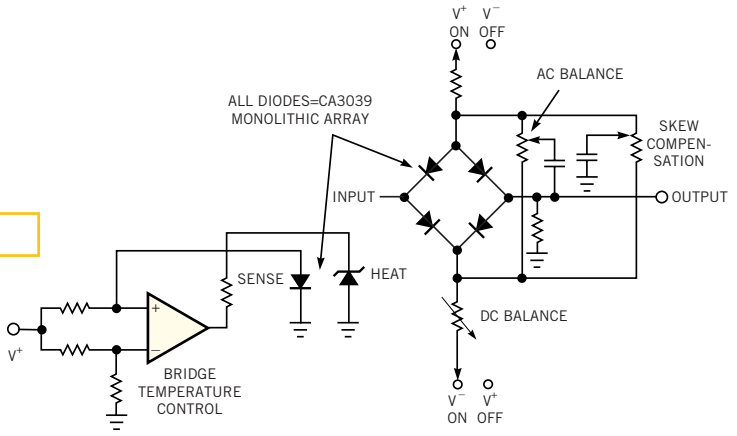

**A diode-bridge-switch scheme minimizes switching feedthrough, which prevents the residue amplifier from overdriving the oscilloscope. Temperature control maintains a 10-µV switch-offset baseline.**

## ALTERNATIVE METHODS VERIFY RESULTS

Based on the above results, the sampling-based settling-time circuit appears to be a useful measurement option, but how can you be sure? A good way to verify **Figure 5**'s method is to make the same measurement using alternative methods and see if you get the same results.

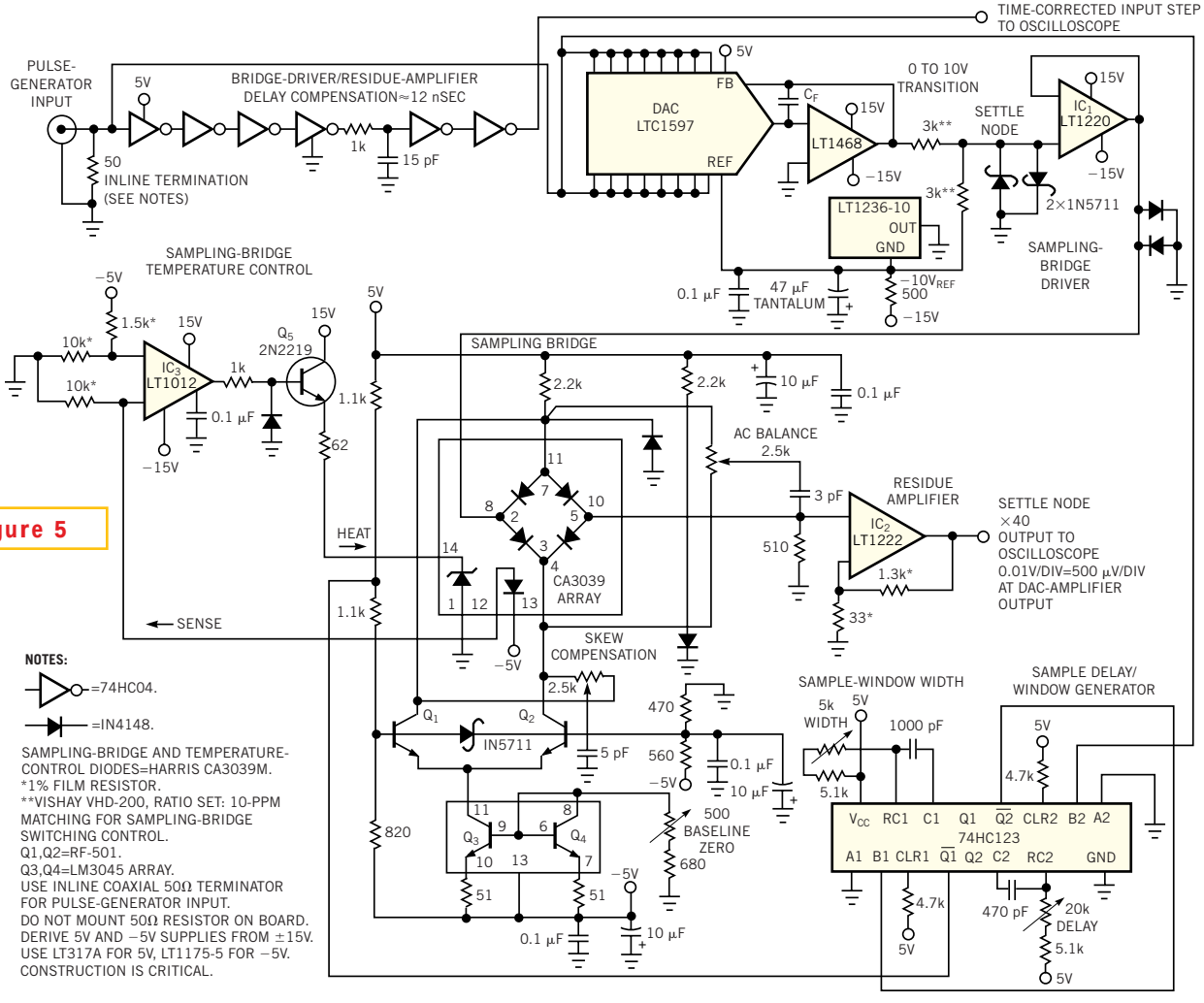
Recall from **Figure 2** that the Schottky-diode-bounded settle node forces a 400-mV overdrive to the oscilloscope, rendering all measurements useless. Now, consider the result if the diodes return to bias voltages that are slightly lower than the diode drops. Theoretically, this setup has the same effect as ground-referred diodes with an inherently lower forward drop, which greatly reduces oscilloscope overdrive. In practice, diode V-I characteristics

Figure 4




**A more detailed schematic of the diode-bridge switch includes adjustments for ac balance, dc balance, and switch-drive timing skew. Two uncommitted diodes in the diode array provide the sense and heat temperature controls.**

Figure 5




**A detailed schematic of the DAC-setting-time-measurement circuit includes the DAC and its output amplifier, the temperature-controlled diode-bridge switch, time-correction circuitry for the input step to the oscilloscope, and a delayed-pulse generator for proper positioning of the sample window.**

and temperature effects limit achievable performance to uninteresting levels. Clamping reduction is minimal, and diode forward leakage, which occurs when the settle node reaches zero, causes signal amplitude errors. Although this approach is impractical, it hints at a more useful method.

### METHOD I: BOOTSTRAPPED CLAMP

One approach returns the diodes to amplifier-generated voltages bootstrapped from the settle node's input signal (**Figure 8**). This method maintains the diode bias at the optimum point with respect to the settle-node signal. During DAC-amplifier slew, the settle-node signal is large, and the amplifiers supply a resultant large bias to the diodes, forcing the desired small clamp voltage. When the DAC-amplifier comes out of slew, the settle-node signal nearly approaches zero, the clamp amplifiers supply almost no diode bias, and the oscilloscope monitors the uncorrupted settle-node output. Adjustable amplifier gains permit optimal setting of positive and negative bound limits. This scheme offers the possibility of minimizing oscilloscope overdrive and preserving signal-path integrity.

The circuit in **Figure 9** adapts the bootstrapped clamp to **Figure 6**'s settling-time test circuit. The clamp circuit, comprising $IC_3$ and $IC_4$, is nearly identical to **Figure 8**'s circuit. The settle node feeds the residue amplifier ($IC_1$ and $IC_2$), which drives the bootstrapped clamp. $IC_1$ and $IC_2$ supply a nonsaturating gain of 80 to the clamp, which permits a 500-μV/div oscilloscope scale factor with respect to the DAC-amplifier output. As before, the circuit time corrects the input pulse for signal-path delays. Additionally, FET probes at the outputs ensure overall delay matching. The bootstrapped clamp's output impedance mandates a FET probe. A second FET probe can monitor the input step but only to maintain channel-delay matching.

### METHOD II: SAMPLING OSCILLOSCOPE

As previously discussed, classic sampling oscilloscopes are inherently immune to overdrive, so why not use this feature and attempt to measure settling time using a simple diode clamp? The circuit in **Figure 10** is identical to that in **Figure 9**, except that a simple diode clamp replaces the bootstrapped clamp. These conditions heavily overdrive the sampling scope—a Tektronix (www.tek.com) type 661 with 4S1 vertical and 5T3 timing plug-ins—which is ostensibly immune to the overdrive insult.

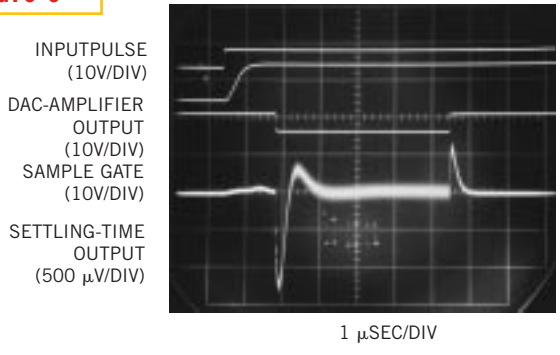
### METHOD III—DIFFERENTIAL AMPLIFIER

In theory, a differential amplifier that has one input biased at the expected settled voltage can measure settling time to 16-bit resolution. In practice, this measurement is extraordinarily demanding for a differential amplifier. The amplifier's overload-recovery characteristics must be pristine. In fact, no commercially produced differential-amplifier or -oscilloscope plug-in meets this requirement. However, a recently introduced instrument, the differential amplifier type 1855 from Preamble Instruments (www.preamble.com), which is not fully specified at these levels, appears to have superb overload-recovery performance (**Figure 11**). An internal adjustable reference biases the amplifier's negative input to the expected settled voltage. The differential amplifier's clamped output operates at a gain of 10 and drives $IC_1$ and $IC_2$. Together, $IC_1$ and $IC_2$ produce a bounded, nonsaturating gain of 40. This circuit cannot overdrive the monitoring oscilloscope, which operates at 0.2V/div (500 μV/div at the DAC amplifier).

### SUMMARIZE THE RESULTS

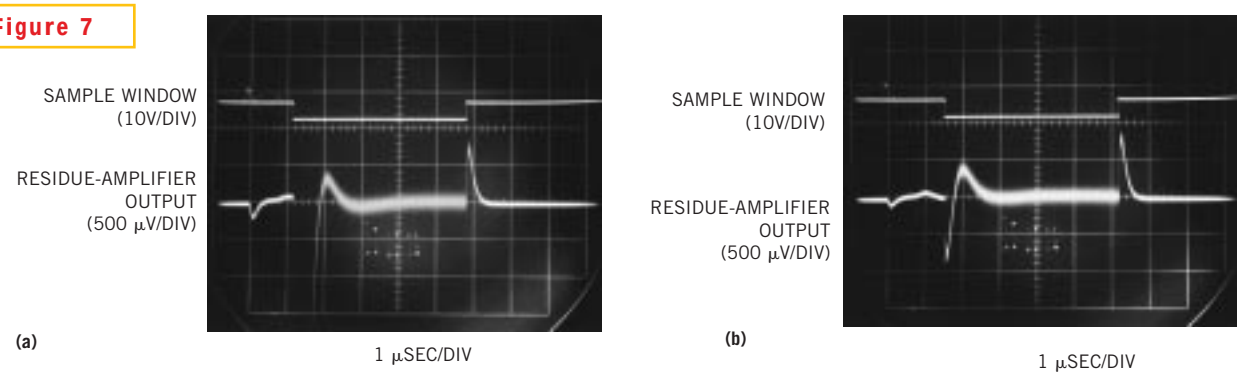
The simplest way to summarize the results of these four measurement techniques is by visual comparison. **Figure 12** displays the settling times of all four circuits. If all four ap-

**Figure 6**




**With proper trimming and proper positioning of the sample gate's window, the settling-time measurement is 1.7 μsec.**

**Figure 7**



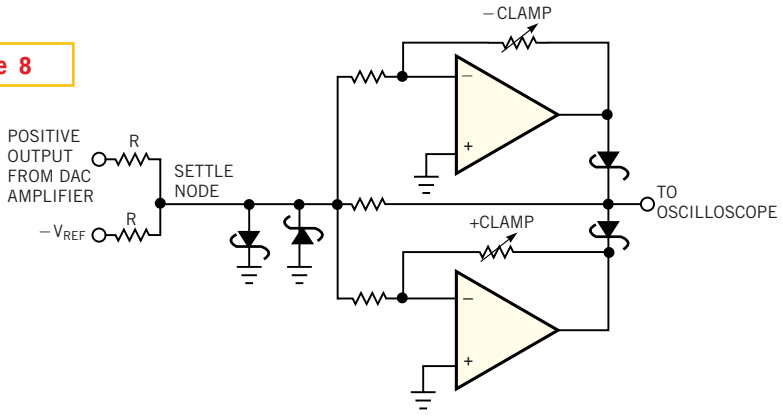

**Properly positioning the sampling window in time is critical. Inadequate sample-gate delay overdrives the oscilloscope and results in off-screen activity (a). The optimal delay time positions the sampling window so that all output settling information is well within the screen's boundaries (b).**

proaches represent good measurement techniques and if you properly construct each circuit, the results should be identical. If the results are identical, they have a high probability of being valid. Remember that the construction details are critical.

Examination of the four scope photos in **Figure 12** shows identical 1.7-µsec settling times and settling-waveform signatures. The shape of the settling waveform is identical in all four photos. In each photo, the top trace is the time-corrected input step, and the bottom trace is the settle signal. In the bootstrapped-clamp circuit, the oscilloscope undergoes about a 2.5× overdrive, although the settling signal appears undistorted (**Figure 12b**). Despite a brutal overdrive of the classic sampling scope, the scope appears to respond cleanly, giving a plausible settle-signal presentation (**Figure 12c**). For the differential-amplifier circuit, the settle signal comes smoothly out of bound, entering the amplified linear region between the third and fourth vertical divisions (**Figure 12d**). The settling signature appears reasonable, and complete settling occurs just beyond the fourth vertical division. This kind of agreement makes the measured results highly credible. It also provides you with the confidence to characterize a variety of amplifiers.

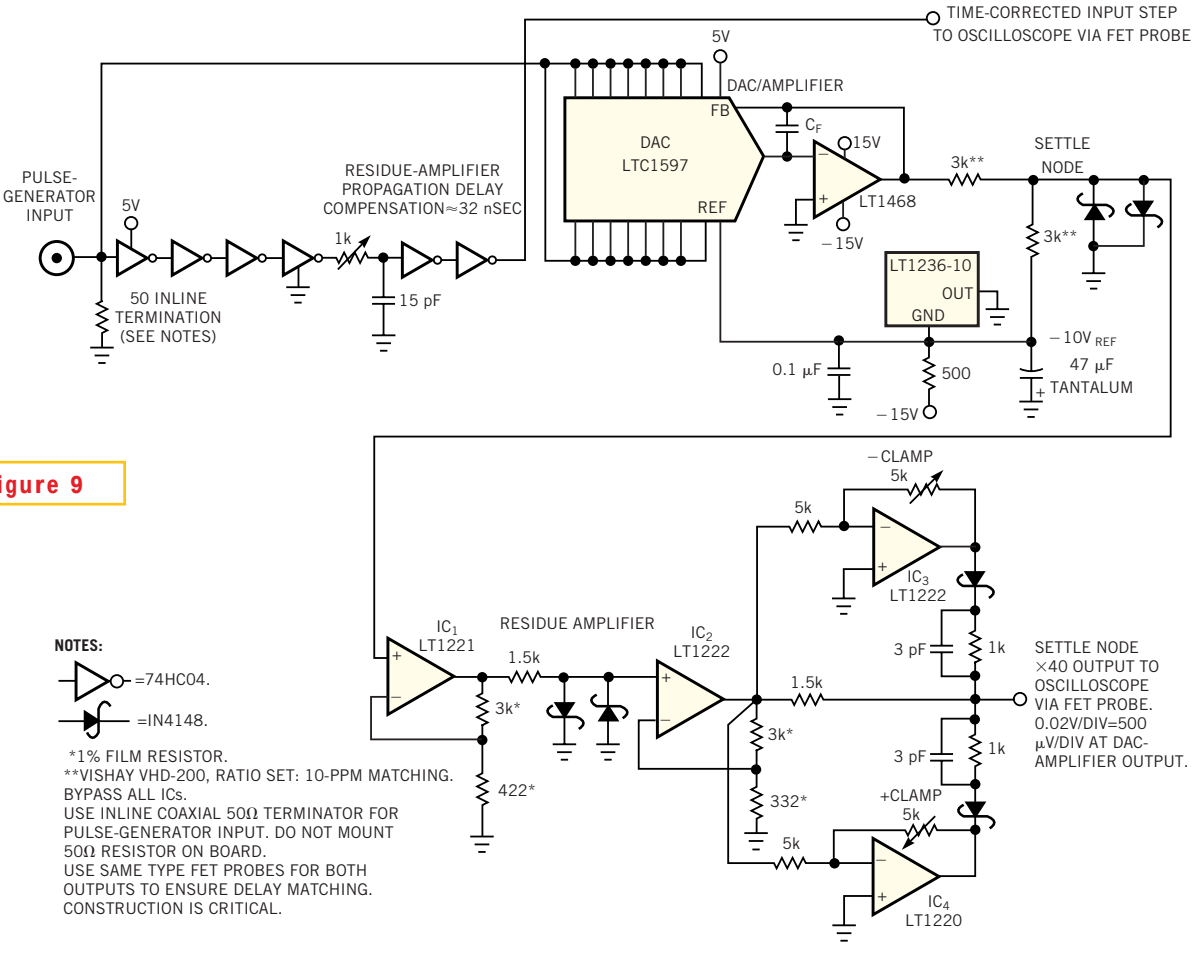
When discussing DAC settling time, you

Figure 8




**A bootstrapped clamp biases the diodes from the settle-node input signal to minimize the effects of V-I characteristics and temperature.**

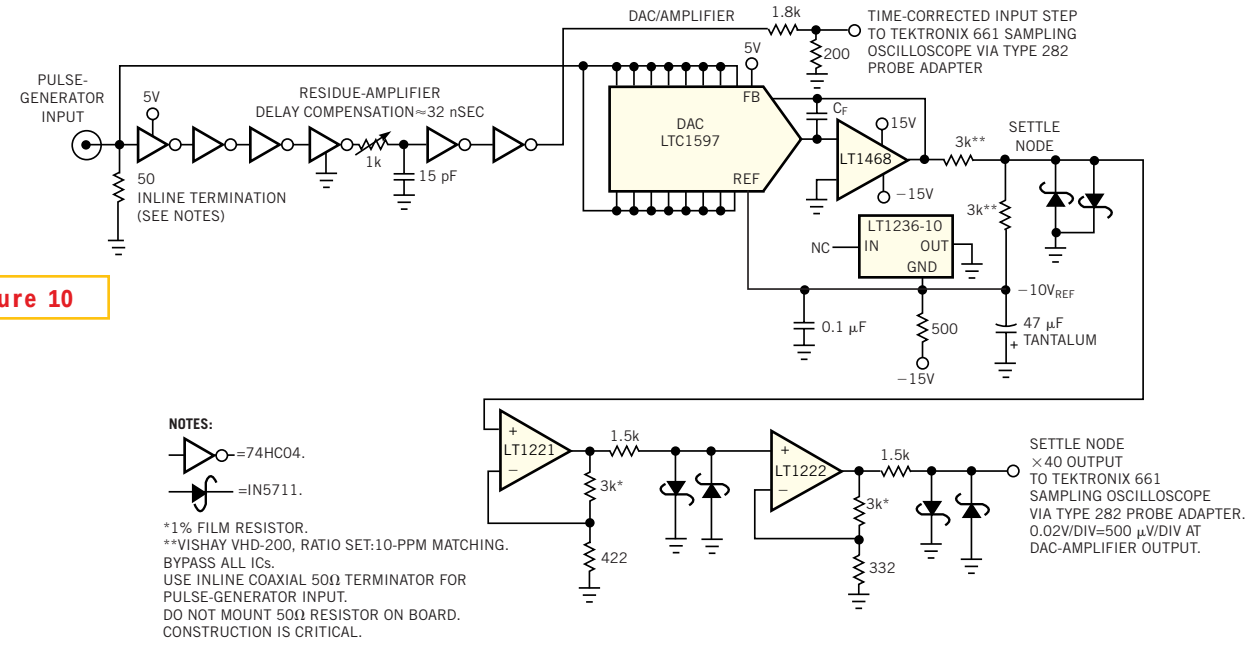
Figure 9




**A bootstrapped-clamp-based settling-time-measurement circuit results in a substantially lower oscilloscope overdrive than you get with the conventional diode clamp, but the oscilloscope must still tolerate ≈2.5× screen overdrive.**

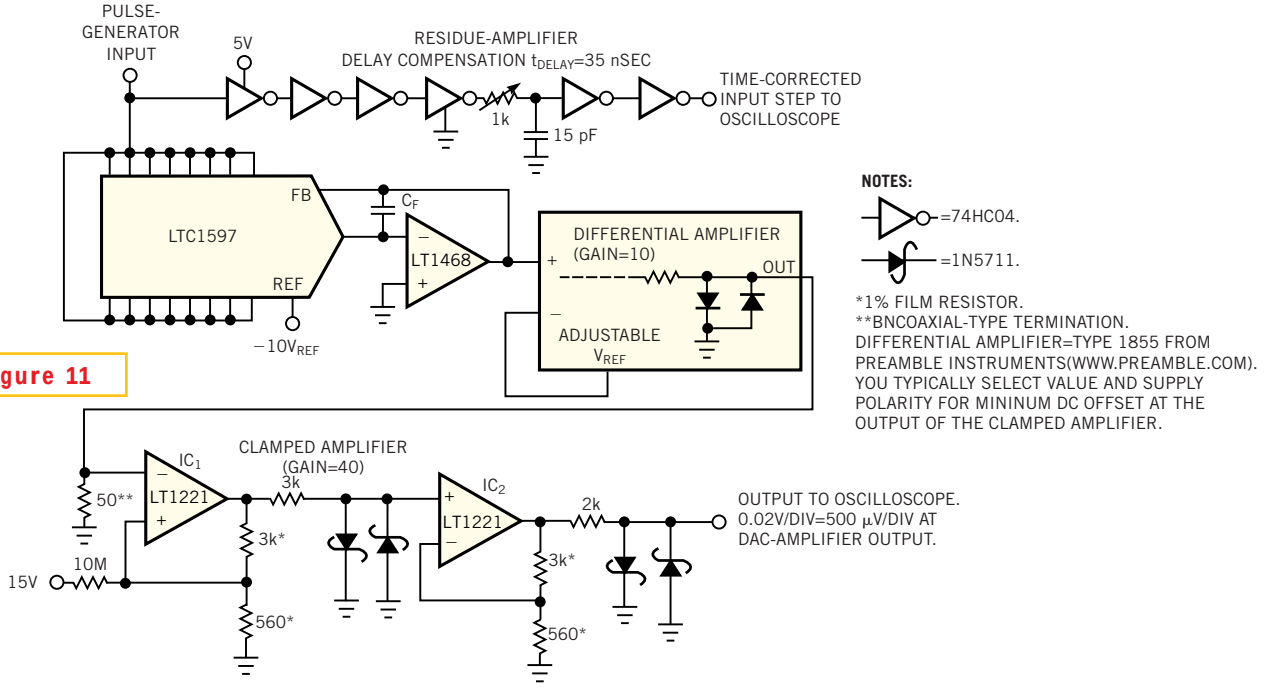
cannot isolate the DAC from its output amplifier; the DAC-amplifier combination is crucial to obtaining the performance you desire. However, beware of oversimplifying this complex topic. A suitable amplifier for your application may not be accurate to 16 bits over temperature or, in some cases, even at 25°C. Many applications, such as ac signal processing, servo loops, and waveform generation, are insensitive to dc-offset error. Therefore, amplifiers that are not accurate to 16 bits may still be worthy candidates. Applications requiring dc accuracy to 16 bits (10V full-scale) must keep input errors at less than 15 nA and 152 µV

Figure 10



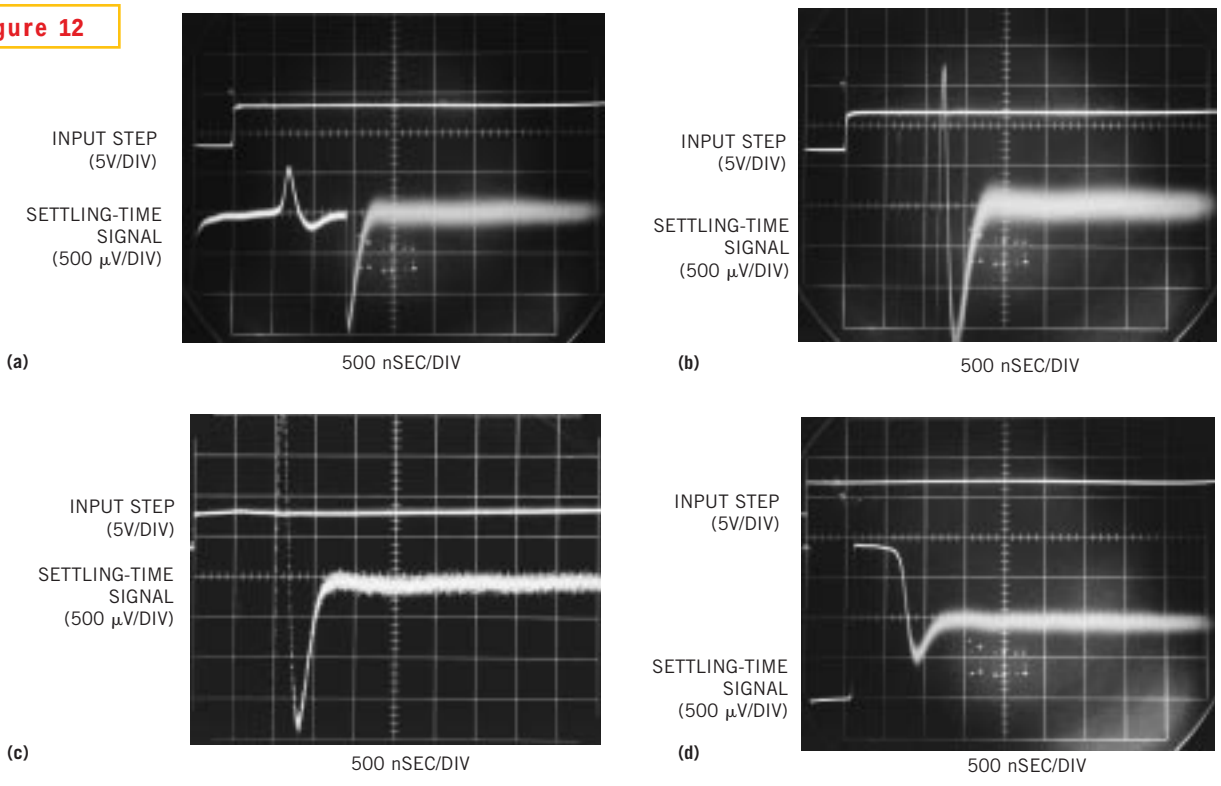

**A classic sampling oscilloscope's inherent overload immunity allows you to use a simple diode clamp in place of a bootstrapped clamp.**

Figure 11




**A differential amplifier with excellent input-overload recovery allows 16-bit settling-time measurements without overdriving the oscilloscope.**

Figure 12



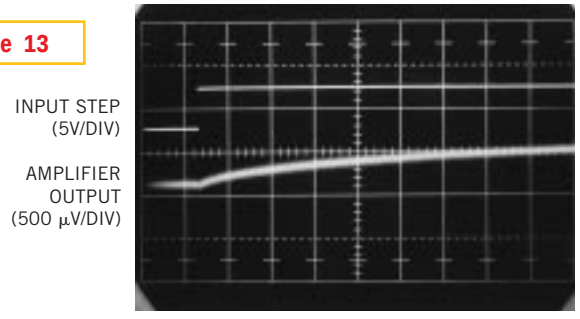

**Settling-time-measurement results of all four techniques–the original diode-bridge circuit (a), the bootstrapped-clamp method (b), the simple diode clamp with a classic sampling oscilloscope (c), and the differential-amplifier approach (d)–show identical 1.7-µsec settling times and identical settling-waveform signatures.**

to maintain performance. Amplifiers with 16-bit accuracy fall into two categories: amplifiers with absolute dc conformance at room temperature and amplifiers with absolute dc conformance over temperature.

All amplifiers have an inherent accuracy-versus-speed trade-off. Some very accurate amplifiers are relatively slow. Ask yourself two important questions: Do you really need 16 bits over temperature and how fast do you need to go? The circuit in **Figure 6** combines the LTC1597 DAC and the LT1468 amplifier for a blend of 16-bit accuracy and a 1.7-µsec settling time.

A final category of settling-time error is thermally based. Some poorly designed amplifiers exhibit a substantial "thermal tail" after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after the output appears settled. After checking settling at high speed, it is always a good idea to slow the oscilloscope sweep and look for thermal tails (**Figure 13**). The loaded amplifier slowly drifts 400 µV after apparent settling (note horizontal-sweep speed). Often, loading the amplifier's output accentuates the thermal tail's effect.

Figure 13




**A poorly designed amplifier can exhibit a "thermal tail," which is drift due to die heating, even after it appears that settling has occurred. In this case, loading the amplifier causes a thermal-tail error of 400 µV, or greater than 2.5 LSB.**

Reference

1. Williams, Jim, "Component and meas-urement advances ensure 16-bit DAC settling time," Application Note 74, Linear Technology Corp, 1998.

Acknowledgment

*George Feliz developed the bridge-switching scheme at Linear Technology Corp.*

Author's biography

*Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA, www.linear-tech.com), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

 *By Jim Williams, Linear Technology Corp*

**OBTAINING A RELIABLE SETTLING-TIME MEASUREMENT IS DIFFICULT AND REQUIRES A CAREFUL APPROACH AND AN EXPERIMENTAL TECHNIQUE. YOU CAN USE NEW CIRCUITS TO TEST THE 30-NSEC SETTLING TIME OF A PRECISION WIDEBAND AMPLIFIER.**

# Measuring precision-amplifier settling time

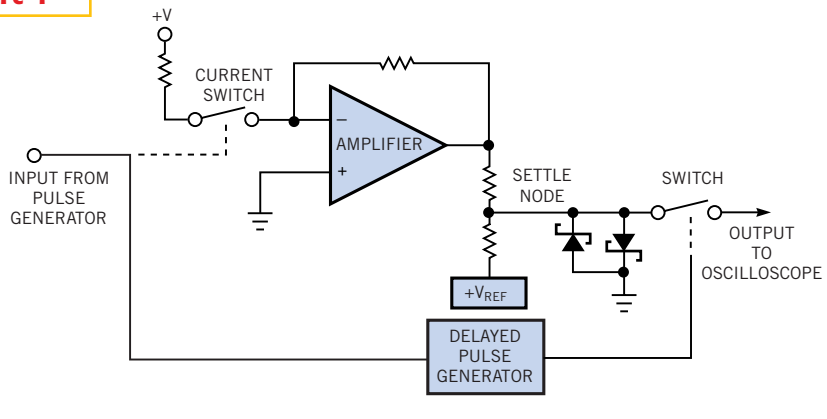
Countless applications, including instrumentation, waveform-generation, and data-acquisition systems, use wideband amplifiers. Some of the new amplifiers combine precision with high-speed operation. As with many other components, the dc specifications are relatively easy to verify. However, ac specifications and settling time require sophisticated measurement approaches. Obtaining a reliable nanosecond-region settling-time measurement is difficult and requires a careful approach and an experimental technique.

A previous article discussed the basics of settling-time measurements and the techniques for measuring the settling time of a 16-bit DAC together with its output amplifier (**Reference 1**). The techniques necessary to measure the settling time of an amplifier by itself are similar but have significant differences. For one, the circuit to measure only the amplifier settling time is 60 times faster than the 16-bit DAC measurement circuit. Also, the measurement is less precise: 0.1% versus 0.0015%.

High-speed settling time is difficult to measure because the most common circuit for measuring settling time, which uses the "false-sum-node" technique, suffers from many drawbacks. The circuit requires the input pulse to have a flat top within the required measurement limits, which are typically settling within 5 mV or less for a 5V step. No general-purpose pulse generator can hold output amplitude and noise within these limits. The generator's output causes aberrations to appear at the oscilloscope probe, and these aberrations are indistinguishable from amplifier-output movement. Thus, the results are unreliable.

The oscilloscope connection also presents problems. As probe capacitance rises, ac loading of the circuit's resistor junction influences observed set-

**Figure 1**




**The switch at the input gates a current step to the amplifier under test, making the circuit insensitive to pulse-generator aberrations. The output, or sampling, switch prevents the oscilloscope from monitoring the settle node until settling is nearly complete, thereby eliminating overdrive.**

tling waveforms. A 10-pF probe alleviates this problem, but this probe's 10× attenuation sacrifices oscilloscope gain; 1× probes are unsuitable because of their excessive input capacitance.

Finally, the 400-mV drop across the clamp diodes at the circuit's settle node can cause the oscilloscope to undergo an unacceptable overload, which brings the displayed results into question because the overdrive-recovery characteristics of oscilloscopes can vary widely.

Thus, measuring an amplifier's settling time requires a "flat-top" pulse generator and an oscilloscope that is somehow immune to overdrive. These issues are central to a wideband-amplifier settling-time measurement.

## SWITCH CURRENT, NOT VOLTAGE

You can avoid the flat-top pulse-generator requirement by switching current rather than voltage. It is easier to gate a quickly settling current into the amplifier's summing node than to control a voltage. This approach makes the input-pulse generator's job easier, although it still must have a rise time of 1 nsec or less to avoid measurement errors (see **sidebar** "Subnanosecond-rise-time pulse generators for the rich and poor").

The only oscilloscope technology that offers inherent overdrive immunity is the classic sampling scope, which you should not confuse with modern DSOs that have overdrive restrictions. Unfortunately, manufacturers no longer make these instruments, although some are still available on the secondary market. You can, however, construct a circuit that borrows the overload advantages of classic sampling-oscilloscope technology. Also, the circuit can include features for measuring settling times of around 1 nsec.

## MEASURE NANOSECOND-REGION SETTLING

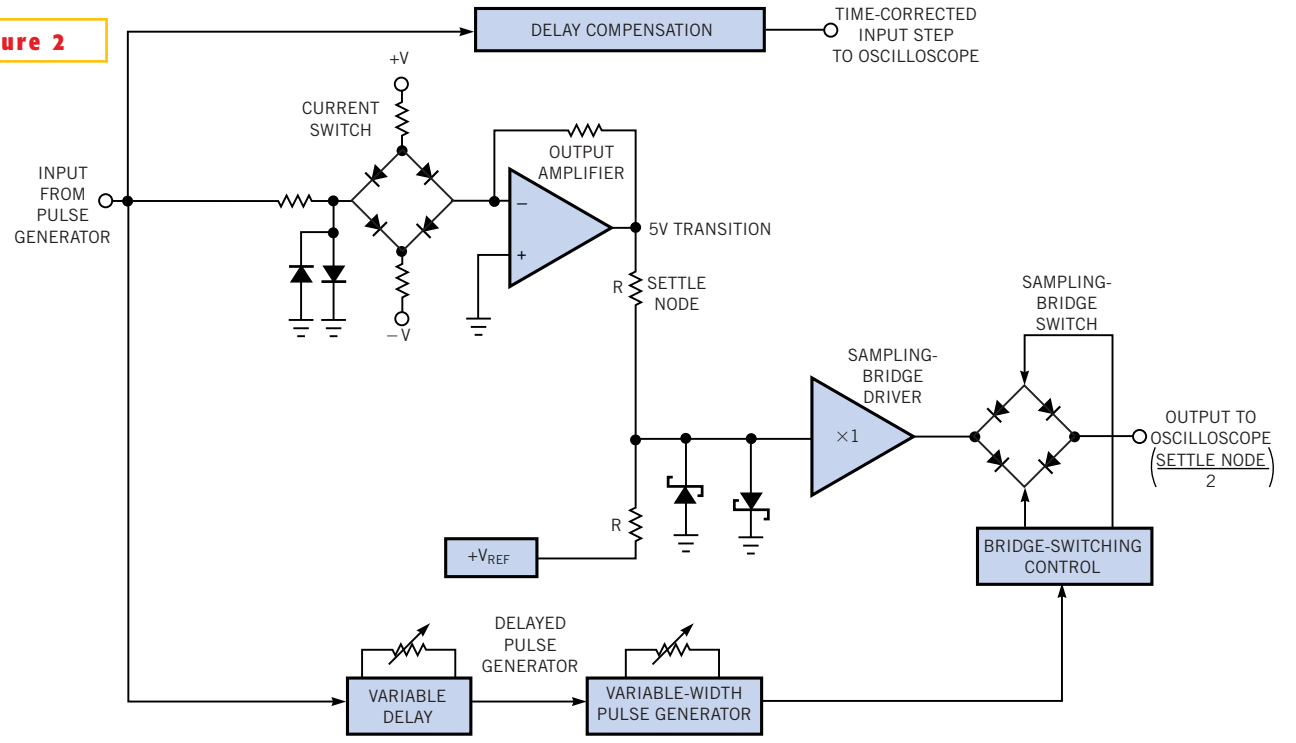
**Figure 1** is a conceptual diagram of a settling-time measurement circuit. This **figure** shares attributes with the false-sum-node circuit but has some additional features. The oscilloscope connects to the settle point through a switch, and the input pulse triggers a delayed pulse generator that determines the switch's state. The circuit sets the timing of the delayed pulse generator so that the switch does not close until settling is nearly complete. In this way, the circuit samples the time as well as the amplitude of the incoming waveform. The circuit never subjects the oscilloscope to overdrive, and no off-screen activity ever occurs. The oscilloscope displays only the tail end of amplifier settling.

The input pulse controls a switch at the amplifier's summing junction. This switch gates current to the amplifier through a voltage-driven resistor and eliminates the flat-top pulse-generator requirement, although the switch must be fast and devoid of drive artifacts.

**Figure 2** provides a more complete representation of the settling-time-measurement scheme. The delayed pulse generator now comprises a delay and a pulse generator, both independently variable. The input step to the oscilloscope undergoes delay compensation, which compensates for the propagation delay of the measurement path.

The most striking new aspects of the diagram are the diode-bridge switches. Borrowed from classic sampling-oscilloscope circuitry, these switches are key to the measurement. The inherent balance of a diode bridge eliminates charge-injection-based errors, and a diode bridge

**Figure 2**

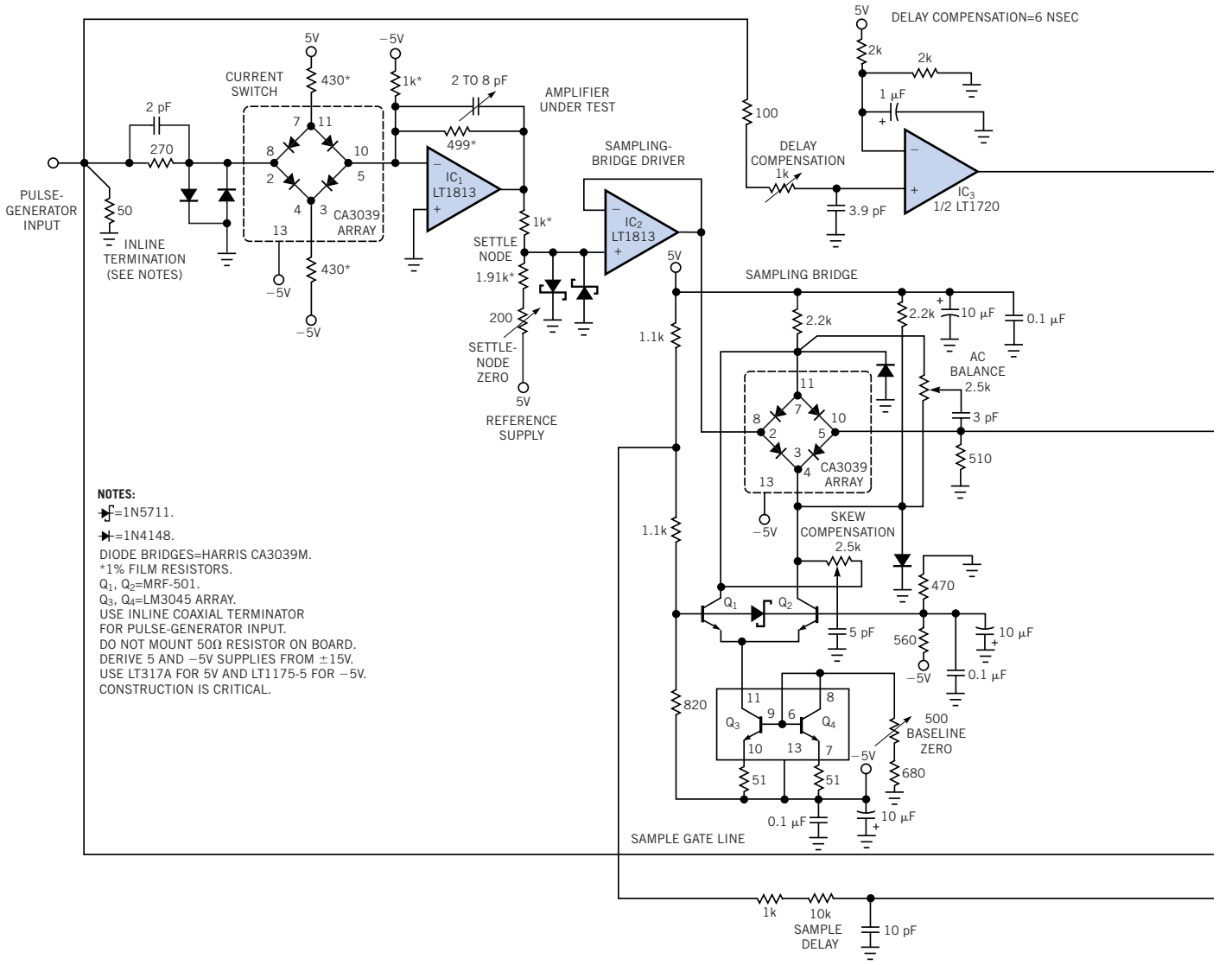



**Using diode bridges for the current and sampling-bridge switches eliminates charge-injection-based errors. Each bridge's balance, combined with matched, low-capacitance monolithic diodes and high-speed switching, yields clean switching.**

is superior to other electronic switches in this characteristic. Any other high-speed-switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are unsuitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt switching, defeating the switches' purpose.

The diode-bridge balance, combined with matched, low-capacitance monolithic diodes and high-speed switching, yields clean switching. The input-driven bridge quickly switches current into the amplifier's summing point, and settling occurs within a few nanoseconds. The diode clamp to ground at this bridge's input prevents excessive bridge-drive swings and ensures that input-pulse characteristics are irrelevant. The output, or sampling, bridge requires considerable attention to achieve the desired performance. The monolithic bridge diodes tend to cancel each other's temperature coefficient—drift is only about 100 µV/°C, but a dc balance is necessary to minimize offset. Trimming the bridge's on-current for zero I/O offset voltage provides dc balance. An ac-balance trim is necessary to correct for diode and layout capacitive imbalances, and a skew-compensation trim corrects for any timing asymmetry in the nominally complementary bridge drive. These ac

**Figure 3**




**This settling-time-measurement circuit closely follows the block diagram of Figure 2. Optimum performance requires attention to layout.**

trims compensate small dynamic imbalances, minimizing parasitic bridge outputs.

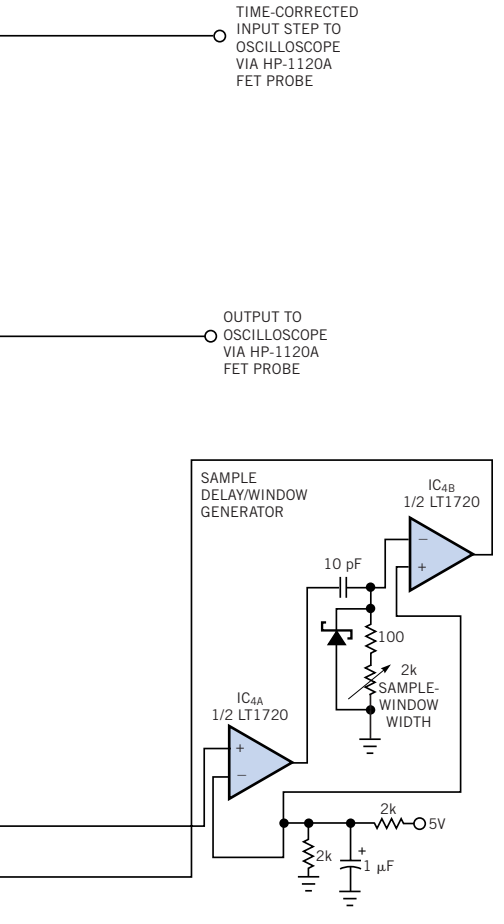
### DETAILED SETTLING-TIME CIRCUITRY

**Figure 3** details the settling-time measurement circuitry for $IC_1$, the LT1813 amplifier under test. The input pulse switches the input bridge and also routes to the oscilloscope via a delay-compensation network. The delay network, comprising a fast comparator, $IC_3$, will be approximately 1 nsec.

For the settling-time-measurement circuit, three delay measurements are of interest: the delay from the pulse generator to the amplifier under test, the delay from the amplifier under test to the settle node, and the delay from the amplifier under test to the output.

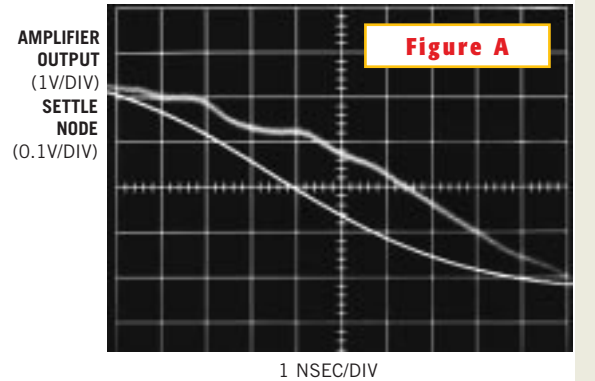
The delay from the pulse-generator input to the amplifier under test is approximately 800 psec. **Figure A** indicates 2.5 nsec from the amplifier under test to the settle node. **Figure B** indicates 5.2 nsec from the amplifier under test to the output. In **Figure A**'s measurement, the probes have a severe source-impedance mismatch. You can compensate for this mismatch by adding a series 500Ω resistor to the probe that monitors the amplifier under test. This provision approximately equalizes this probe's source impedance and negates the probe's input-capacitance term, which is approximately equal to 1 pF.

The measurements reveal a circuit I/O delay of 6 nsec, and you apply this correction by adjusting the 1-kΩ delay-compensation trim at the input to $IC_3$ in the settling-time-measurement circuit.

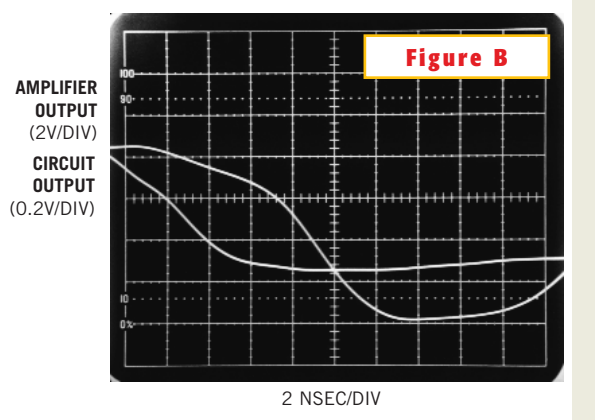



## MEASURING AND COMPENSATING SETTLING-CIRCUIT DELAY

The settling-time-measurement circuit uses an adjustable delay network to time-correct the input pulse for delays in the signal-processing path. Typically, these delays introduce errors of 20%, so an accurate correction is necessary. Setting the delay-compensation potentiometer involves observing the network's I/O delay and adjusting for the appropriate time interval. Determining the "appropriate" time interval is somewhat more complex and requires a wideband oscilloscope with FET probes. To ensure accuracy in the following delay measurements, you must verify the probe's time skew. Connect the probes to a subnanosecond pulse generator and verify the probe skew within 100 psec. Verifying the probe skew ensures small error for the delay measurements, which




**The delay from the amplifier-under-test output to the settle node is 2.5 nsec.**




**The delay from the amplifier-under-test output to the circuit's output is 5.2 nsec.**

and an adjustable RC network, compensates the oscilloscope's input step signal for the 6-nsec delay through the circuit's measurement path (see **sidebar** "Measuring and compensating settling-circuit delay"). The circuit compares $IC_1$'s output to the 5V reference via the summing resistors at the settle node. The 5V reference also furnishes the bridge's input current, making the measurement ratiometric. The −5V-reference supply pulls current from the summing point at $IC_1$'s inverting input, allowing the amplifier a 5V step from +2.5V to −2.5V. $IC_2$ unloads the clamped settle node and drives the sampling bridge.

The input pulse triggers the $IC_4$-based delayed pulse generator. This circuitry produces a delayed pulse whose width sets the on-time of the sampling bridge. The 10-kΩ sample-delay potentiometer controls delay time, and the 2-kΩ sample-window-width potentiometer controls pulse width. If you appropriately set the delay, the circuit provides no input to the oscilloscope until settling is nearly complete, eliminating overdrive. You adjust the sample-window width so that all remaining settling activity is observable. In this way, the oscilloscope's output is reliable, and you can take meaningful data. $Q_1$ through $Q_4$ level-shift the output of the delay generator to provide complementary switching drive to the bridge. The actual switching transistors, $Q_1$ and $Q_2$, are UHF types, permitting true differential bridge switching with less than 1 nsec of time skew.

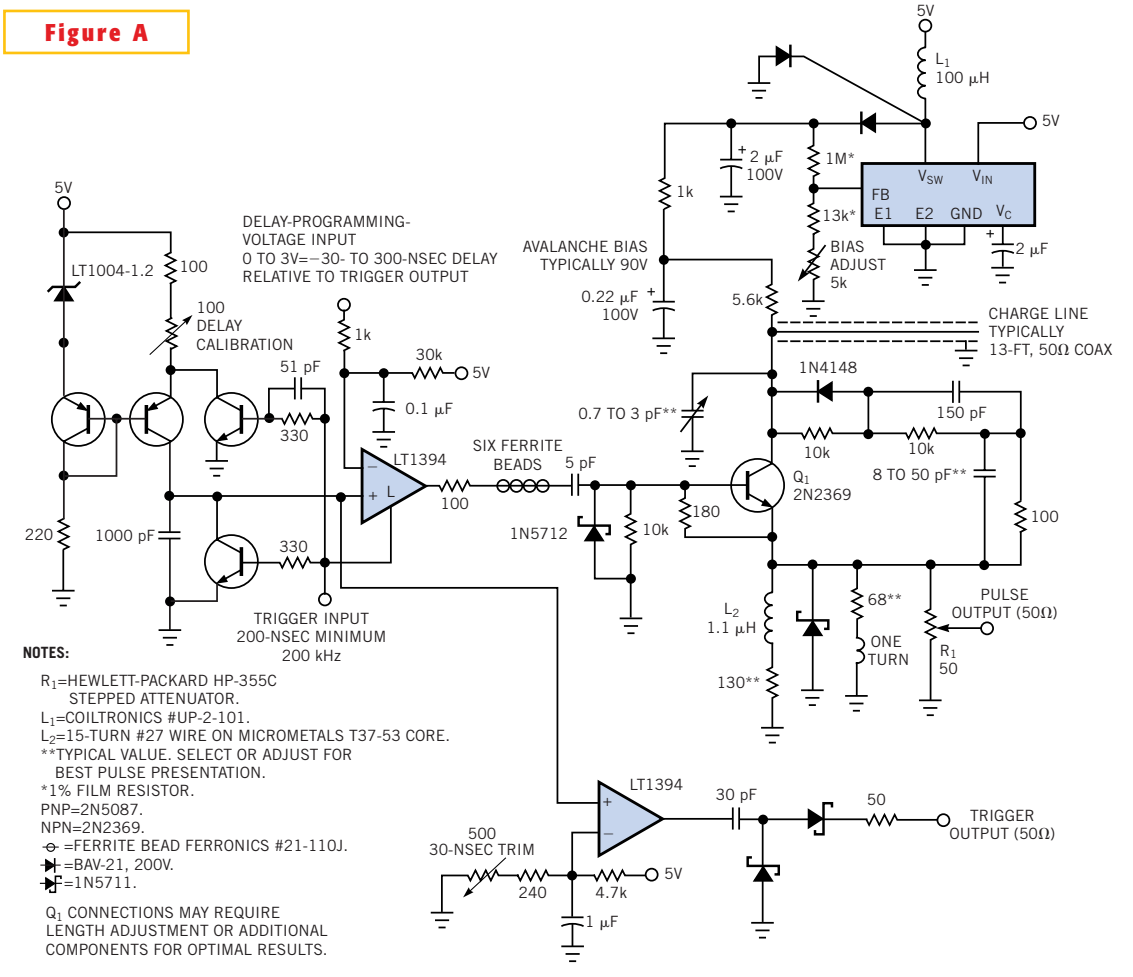
**Figure 4** shows circuit waveforms.

## SUBNANOSECOND-RISE-TIME PULSE GENERATORS FOR THE RICH AND POOR

The input diode bridge of the settling-time measurement circuit requires a subnanosecond-rise-time pulse to cleanly switch current to the amplifier under test. The ranks of pulse generators providing this capability are thin. Instruments with rise times of 1 nsec or less are rare, and costs are excessive. Current-production units can easily cost $10,000, and prices rise to-

Continue on pg 92

**Figure A**




**A programmable delay triggers this subnanosecond-rise-time pulse generator. The charge line at $Q_1$'s collector results in a 40-nsec output width.**

ward $30,000 depending on features. Substantially less expensive approaches are available for bench work and production testing.

The secondary market offers subnanosecond-rise-time pulse generators at attractive cost. The Hewlett-Packard HP-8082A transitions in less than 1 nsec, has a full complement of controls, and costs about $500. The HP-215A, long out of manufacture, has 800-psec edge times and is a clear bargain with a typical price lower than $50. This instrument also has a versatile trigger output, which permits continuous-time phase adjustment from before to after the main output. External trigger impedance, polarity, and sensitivity are also variable. The output, controlled by a stepped attenuator, puts 610V into 50Ω in 800 psec.

The Tektronix type 109 switches in 250 psec. Although amplitude is fully variable, charge lines are necessary to set pulse width. This reed-relay-based instrument has a fixed repetition rate of approximately 500 Hz and no external trigger facility, making it somewhat unwieldy to use. Price is typically $20. The Tektronix type 111 is more practical. Edge times are 500 psec, and the device has fully variable repetition rate and external trigger capabilities. The charge-line length sets the pulse width. Price is usually about $25.

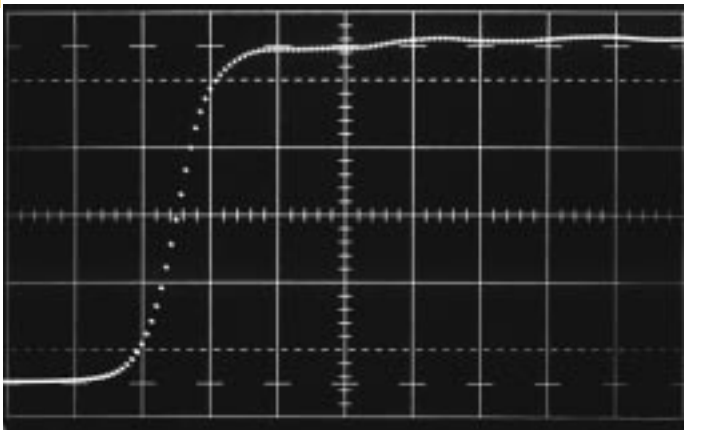
A potential problem with older instruments is availability. Residents of Silicon Valley tend toward inbred techno-provincialism. Citizens of other locales cannot simply go to a flea market, junk store, or garage sale and buy a subnanosecond pulse generator. **Figure A** shows a circuit that produces subnanosecond-rise-time pulses. The circuit's operation essentially duplicates the Tektronix type 111 pulse generator. Rise time is 500 psec, and pulse amplitude is fully adjustable. An external input determines repetition rate, and you can set the occurrence of the output pulse from before to after a trigger output.

This circuit uses an avalanche pulse generator, $Q_1$, to create extremely fast rise-time pulses. The transmission-line length at $Q_1$'s collector sets the pulse width, and a coaxial-cable charge line attaches to the collector. In this case, a 13-ft charge line produces a 40-nsec-wide output.

The picture in **Figure B**, taken with a 3.9-GHz bandpass oscilloscope (Tektronix 547 with 1S2 sampling plug-in) shows output-pulse purity and rise time. The rise time is 500 psec with minimal preshoot and pulse-top aberrations. The pulse's falling edge has similar characteristics.

This level of cleanliness requires considerable layout experimentation, particularly with $Q_1$'s emitter and collector lead lengths and associated components. Ground-plane-type construction with high-speed layout, connection, and termination techniques is essential for good results from this circuit. Additionally, small inductances or RC networks may be necessary between $Q_1$'s emitter and $R_1$ to get best pulse presentation.

**Figure B**




**The pulse-generator output shows a 500-psec rise time with minimal pulse-top aberrations.**

Trace A is the time-corrected input pulse, Trace B is the amplifier output, Trace C is the sample gate, and Trace D is the settling-time output. When the sample gate goes low (Trace C), the bridge switches cleanly, and the last 10 mV of slew is easily observable. Ring time is also clearly visible, and the amplifier settles nicely to final value. When the sample gate goes high, the bridge switches off with only millivolts of feedthrough. Note that no off-screen activity occurs; the oscilloscope is never subjected to overdrive.

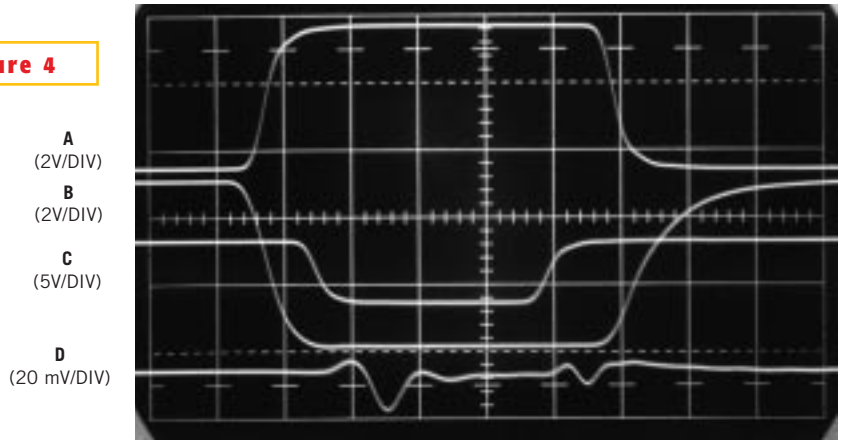
**Figure 5** expands vertical and horizontal scales so that settling detail is more visible. Note that this photo measures settling time from the onset of the time-corrected input pulse. Appropriate setting of the oscilloscope gain results in an amplitude measurement with respect to the amplifier, not the sampling bridge's output. This calibration eliminates the ambiguity that the ÷2 ratio of the summing resistors at the settle node introduces. Trace A is the time-corrected input pulse, and Trace B is the settling output. The last 20 mV of movement, which begins at the center-screen vertical marker, is easily observable, and the amplifier settles inside 5 mV (0.1%) in 30 nsec after the onset of the input step.

## PROPERLY SET TRIMS

As mentioned, the circuit requires dc and ac trimming to achieve this level of performance. Making these adjustments requires disabling the amplifier by disconnecting the input-current switch and

the 1-kΩ resistor at the amplifier and shorting the settle node directly to the ground plane (**Reference 2**). With the amplifier disabled and the settle node grounded, the output should theoretically always be zero, but this is not the case for an untrimmed bridge. Because the sample gate's transitions cause large signal swings, ac and dc errors are present. Additionally, the output shows significant dc-offset error during the sampling interval. Adjusting the ac-balance and skew-compensation trims minimizes the switching-induced transients. The baseline-zero trim adjusts the dc offset. Using these adjustments, you can minimize all switching-related activity and reduce offset error to unreadable levels. You can use the settle-node-zero trim to correct for any further differences between the presettling and postsettling baseline.

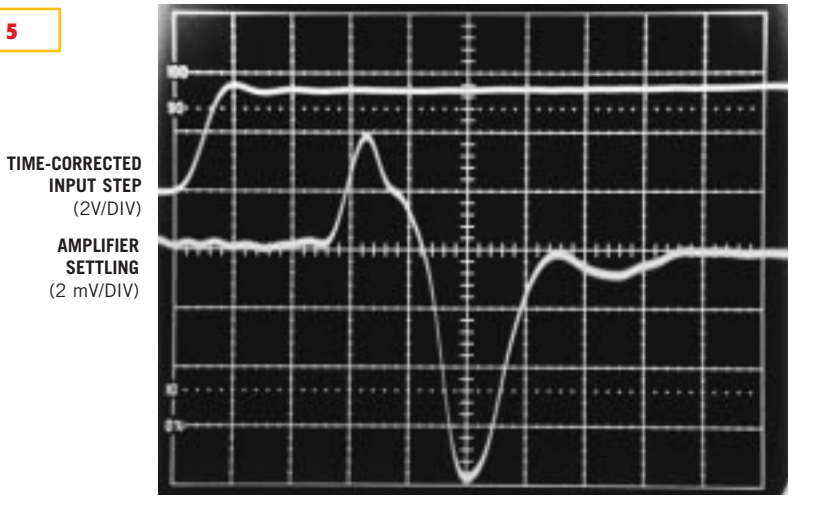
Figure 4




**Settling-time-circuit waveforms include the time-corrected input pulse (Trace A), the amplifier-under-test output (Trace B), the sample gate (Trace C), and the settling-time output (Trace D).**

Some other factors are important for the circuit to operate properly (**Reference 2**). First, you must properly position the sampling window in time. Initiating the sample window too early causes the measurement circuit's output to overdrive the oscilloscope when sampling commences. In general, it's good practice to "walk" the sampling window up to the last 10 mV or so of amplifier slewing so that the onset of ring time is observable. Second, the amplifier requires frequency compensation using the $C_{COMP}$ capacitor in **Figure 3** to get the best possible settling time. Light compensation permits fast slewing but causes excessive ringing amplitude over a long time. At the other extreme, a large value for $C_{COMP}$ eliminates all ringing but slows the amplifier so that settling stretches to 50 nsec. A carefully chosen capacitor value results in tightly controlled damping and a settling time of 30 nsec.

Figure 5




**Expanded vertical and horizontal scales show 30-nsec amplifier settling time to within 5 mV.**

Finally, achieving this level of performance depends on layout. The circuit's construction involves a number of subtleties and is crucial.□

## References

1. Williams, Jim, "Measuring 16-bit settling times: the art of timely accuracy," *EDN*, Nov 19, 1998, pg 159.

2. Williams, Jim, "30 nanosecond settling time measurement for a precision wideband amplifier," Application Note 79, Linear Technology Corp, 1999.

3. Williams, Jim, "Component and measurement advances ensure 16-bit DAC settling time," Application note 74, Linear Technology Corp, 1998.

## Author's Biography

*Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA, www.linear-tech.com), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

*Jim Williams, Linear Technology, and J Phillips and G Vaughn, CTS Wireless Components*

**PIEZOCERAMIC TRANSFORMERS HAVE MANY FEATURES, INCLUDING SMALL FORM FACTOR, THAT MAKE THEM INHERENTLY WELL-SUITED TO CCFL-BACKLIGHT INVERTERS.**

# A svelte beast cuts high voltage down to size

LCDs are in use everywhere, from PCs of all sizes to point-of-sale terminals to instruments, autos, and medical apparatus. LCDs use a cold-cathode fluorescent lamp (CCFL) as a light source to backlight the display. The CCFL requires a high-voltage ac supply for operation. Typically, more than 1000V rms are necessary to initiate lamp operation, with sustaining voltages of 200 to 800V ac.

To date, designers have used magnetic transformers in the high-voltage section of backlight "inverters," which convert a dc voltage to high-voltage ac. Designers have spent much effort on magnetic transformers for CCFL inverters, and much written material exists about these designs (**references 1**, **2**, and **3**).

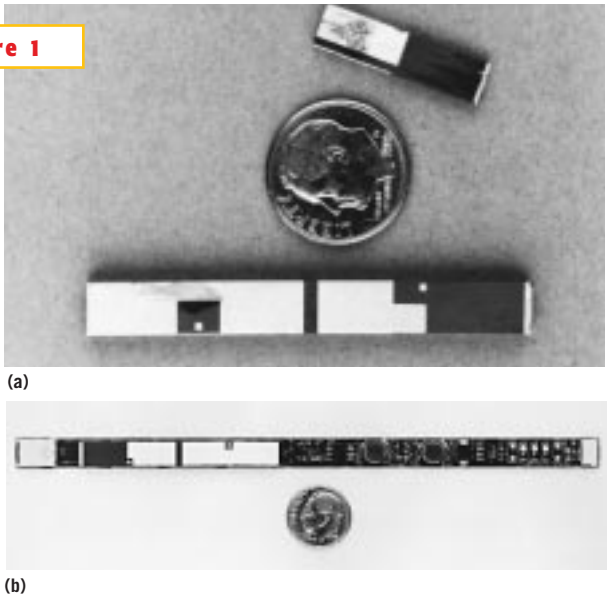
However, the piezoceramic (PZT, for the lead-zirconate-lead-titanate material it comprises) transformer, an arcane and little-known technology, now presents a new approach to this high-voltage generation (see "How it works," pg 54). PZT transformers have many compelling characteristics, including small size, safety, and the ability to work with different displays without recalibration. The size and width of these transformers provide an ideal form factor for constructing space-efficient CCFL-backlight inverters (**Figure 1**).

## MAGNETIC CCFL TRANSFORMERS

The PZT transformer is an important design alternative because magnetic-transformer-based approaches are running into difficulties as pc-board space shrinks. In particular, laptop computers with large-area screens have little room for the backlight-inverter board. In many cases, so little space is available that building the inverter function inside the LCD panel has become attractive although, to date, impractical. Thus, construction and high-voltage-breakdown characteristics of magnetic transformers present barriers to implementing them in these forthcoming space-intensive designs.

Additionally, as refined as magnetic technology is, other inverter problems associated with this technology exist, including the necessity to optimize and

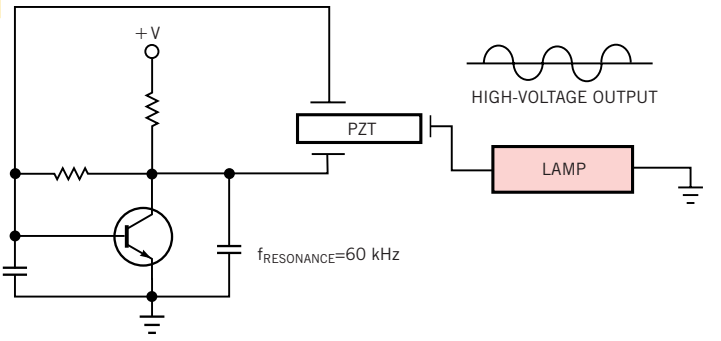
Figure 1




**Piezoceramic transformers—in this case, 1.5 (upper) and 10W (lower) devices—are much smaller and narrower than magnetic transformers (a). A complete LCD-backlight inverter fits onto a much thinner board (b).**

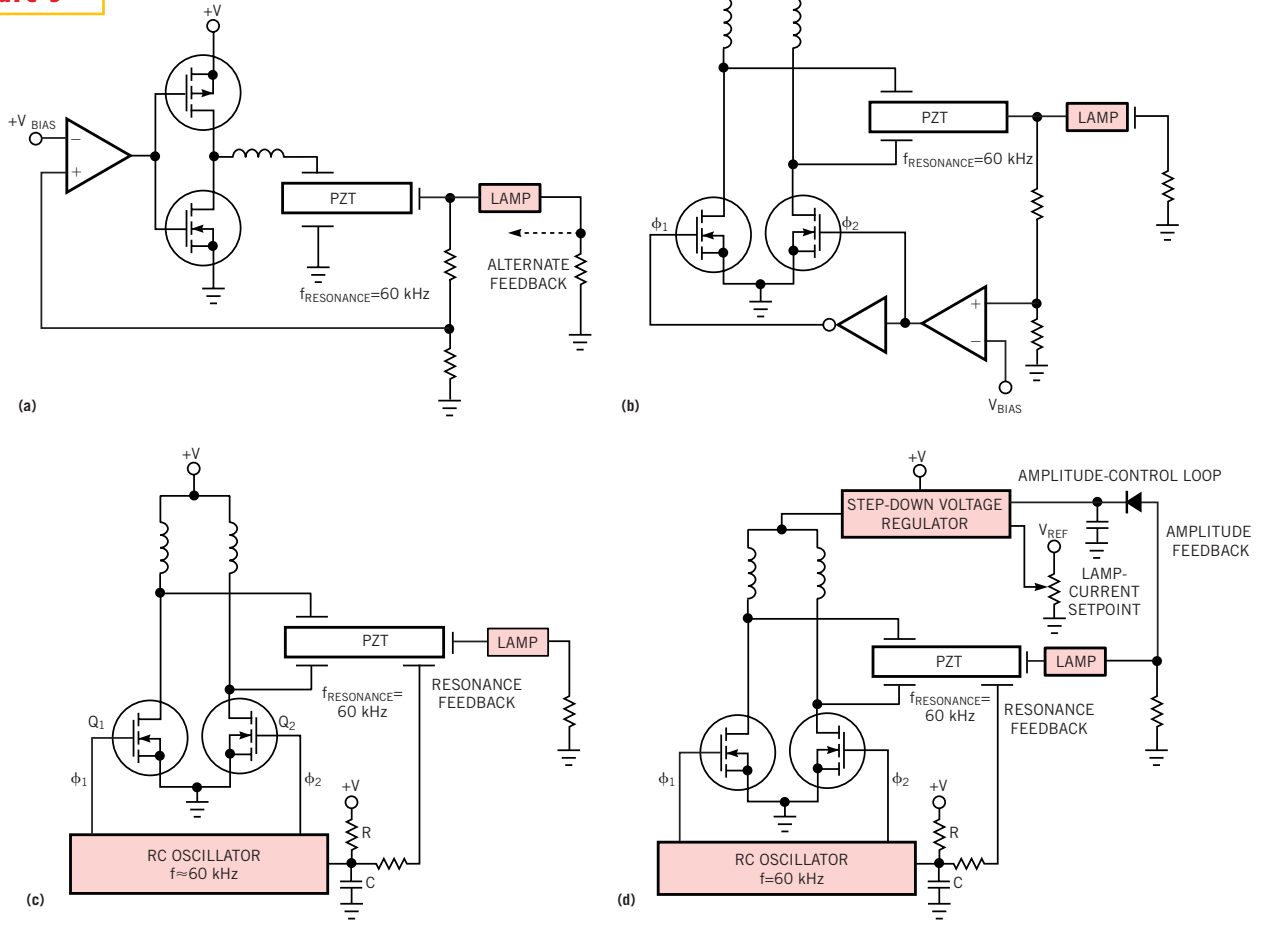
calibrate the inverter for best performance with a given display type. Practically, this requirement means that the manufacturer must adjust inverter parameters, via either hardware or software, to achieve optimum performance with a given display type. Commensurate adjustments in inverter characteristics must accompany changes in the display type. Another problem is fail-safe protection due to self-destructive transformer malfunctions. Finally, the magnetic field that conventional transformers provide can interfere with the operation of adjacent circuitry. With the exception of size, you can address all of these problems, but the solutions in-

**Figure 2**




**A Pierce-type circuit sustains resonance but cannot efficiently deliver power. The circuit also "mode-hops" due to the transformer's parasitic resonances.**

**Figure 3**




**A feedback-based oscillator has an efficient drive stage, but poorly defined transformer-phase characteristics cause spurious modes with line and load variations (a). A push-pull version of the circuit in (a) retains efficiency and permits simple all-n-channel drive. Poor phase characteristics still preclude stable loop operation (b). A feedback tap on the PZT transformer synchronizes the RC oscillator, providing stable phase characteristics (c). Adding an amplitude-control loop with current sensing stabilizes the lamp's intensity (d).**

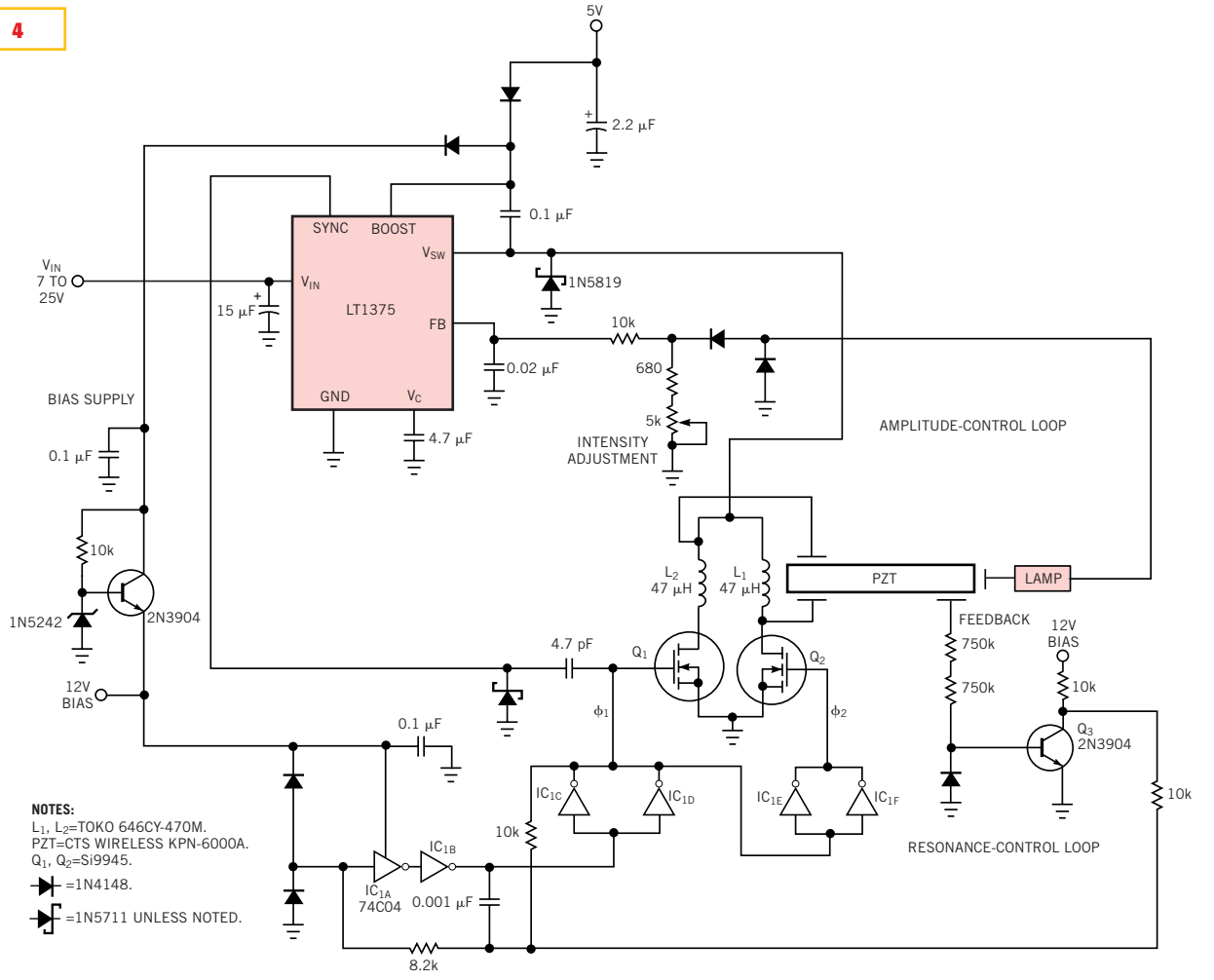
cur economic and circuit/system penalties, as **references 1**, **2**, and **3** discuss.

## PZT TRANSFORMERS CONVERT ENERGY

Like magnetic devices, PZT transformers are basically energy converters. A magnetic transformer operates by converting an electrical input to magnetic energy and then reconverting the magnetic energy back to an electrical output. A PZT transformer has an analogous operating mechanism: A PZT transformer converts an electrical input into mechanical energy and subsequently reconverts this mechanical energy back to an electrical output. The mechanical transport causes the PZT transformer to vibrate, similar to quartz-crystal operation, but at acoustic frequencies. The resonance associated with this acoustic activity is extraordinarily high; Q factors greater than 1000 are typical. This transformer action results from using properties of certain ceramic materials and structures. The physical configuration and number of layers in its construction set a PZT transformer's voltage gain. This structure is obviously different from a magnetic transformer, although some very rough magnetic analogs are turns ratio and core configuration. Also different, and central to any serious drive-scheme attempt, is that a PZT transformer has a large input capacitance, as opposed to a magnetic transformer's input inductance.

Piezoelectric-transformer technology is not new and currently exists in various products (**references 4**, **5**, and **6**). More familiar examples of piezoelectric devices are barbecue-grill igniters, for which a direct mechanical input to the PZT transformer produces an electrical discharge, and marine sonar transducers, for which an electrical input produces a pronounced sonic output. You can also find piezoelectric devices in speakers (tweeters), medical ultrasound transducers, mechanical actuators, and fans. Various designs have attempted to use piezoelectric-based backlight inverters, but previous transformer and circuit approaches could not provide power, efficiency, and wide dynamic range of operation. These designs had restricted transformer operating regions and complex and ill-performing electronic-con-

**Figure 4**




**The design in Figure 3d provides the basis for a complete PZT-based backlight inverter. The PZT transformer's resonant feedback synchronizes the RC oscillator via $Q_3$. The amplitude-control loop powers the transformer via the LT1375 switching regulator.**

trol schemes. Additionally, the PZT-transformer-mounting schemes enlarged the overall size, negating the size advantage.

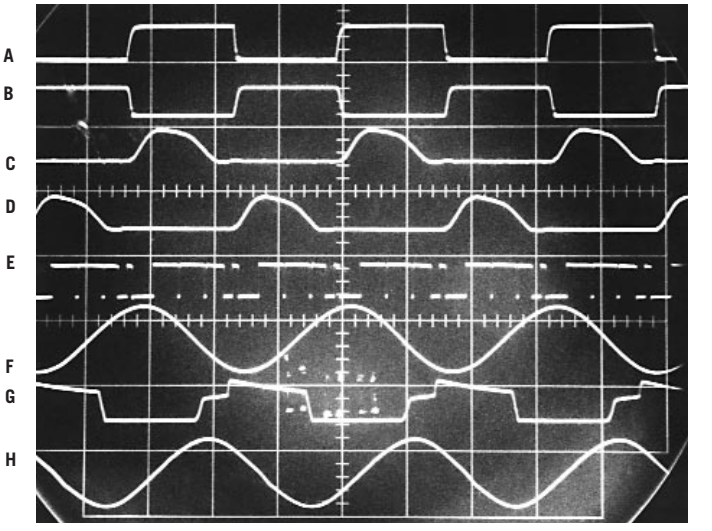
## DEVELOP A CONTROL SCHEME

Constructing a practical circuit requires a few design iterations. The circuit in **Figure 2** treats the PZT transformer like a quartz crystal, using it in a Pierce-type oscillator. Self-resonance occurs, and a sinusoidal ac high voltage drives the lamp. This circuit has a number of unpleasant features. Little power is available due to the circuit's high output impedance. Additionally, the PZT transformer has a number of other spurious modes besides its desired 60-kHz fundamental. Changes in drive level or load characteristics induce "mode-hopping," manifested by the transformer's resonance jumping to subharmonic or harmonic frequencies. Sometimes, several modes occur simultaneously. Operation in these modes results in low efficiency and instability. Practically, this circuit was never a serious candidate, only as an exploratory exercise. Its contribution is demonstrating that the PZT transformer's self-resonance is a potentially viable path.

The circuit in **Figure 3a**, a feedback oscillator, addresses the high-output-impedance problem with a totem-style pair. This circuit is partially successful, although efficient totem drive devoid of simultaneous conduction requires care. The mode-hopping problem persists, and, in this case, the long acoustic transit time through the transformer and the wideband-feedback path aggravates the problem. This acoustic transit time, or transit time at the speed of sound, produces enormous feedback phase error. Even worse, this phase error varies with line and load conditions. The alternate feedback in **Figure 3a** senses current as opposed to voltage. This scheme eliminates the voltage-divider-induced loading but does nothing to address the phase uncertainties and mode-hopping. A final problem, which is common to all resonant oscillators, concerns start-up. Gently tapping the transformer at the low-voltage end usually starts a reticent circuit, but this fact is hardly reassuring. The circuit in **Figure 3b** is similar but uses a ground-referred push-pull power stage, simplifying the drive scheme. This approach is a better one, but phase error and mode-hopping and start-up problems are as before.

The circuit in **Figure 3c** retains the

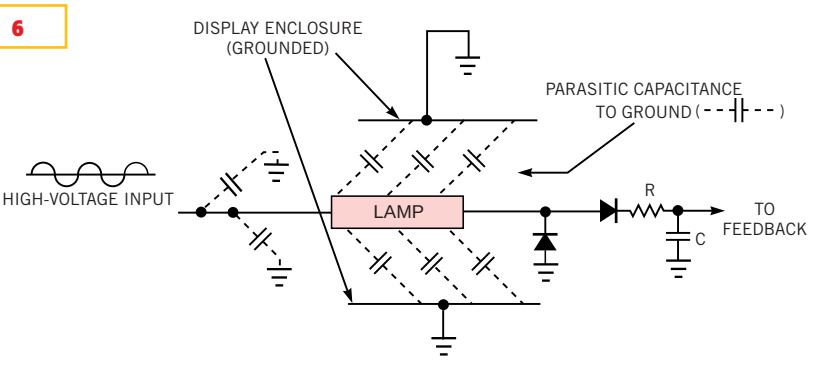
**Figure 5**




| TRACE | VERTICAL SCALE | DESCRIPTION |
|---|---|---|
| A | 20V/DIV | $Q_2$ GATE DRIVE |
| B | 20V/DIV | $Q_1$ GATE DRIVE |
| C | 50V/DIV | $Q_1$ DRAIN RESPONSE |
| D | 50V/DIV | $Q_2$ DRAIN RESPONSE |
| E | 20V/DIV | $L_1$-$L_2$ JUNCTION |
| F | 500V/DIV | PZT FEEDBACK TAP |
| G | 20V/DIV | $Q_3$ COLLECTOR |
| H | 2000V/DIV | PZT HIGH-VOLTAGE OUTPUT |

**Waveforms for the circuit in Figure 4 show the PZT's high-voltage output (Trace H). The PZT transformer acts as a mechanical filter, producing low-distortion sine waves.**

**Figure 6**




**All displays introduce some amount of parasitic capacitance between the lamp, its leads, and other electrically conductive elements.**

drive scheme and solves the remaining problems. Central to this circuit's operation is a new resonance-feedback terminal at the PZT transformer. This connection, precisely positioned on the transformer, provides constant-phase resonance information regardless of operating conditions. At power-up, the RC oscillator drives $Q_1$ and $Q_2$ at a frequency outside resonance. The transformer, excited off-resonance, at first responds inefficiently, although voltage-amplified resonant waveforms appear at the feedback and output terminals. The resonant information at the feedback terminal injection-locks the RC oscillator, pulling it to the transformer's resonance. At this point, the circuit supplies the transformer with on-resonance drive, and efficient operation commences. Note that this type of operation is the heart and soul of a bootstrapped startup circuit. The circuit maintains the feedback terminal's constant-phase characteristic over all line and load conditions, and the loop enforces resonance.

The circuit in **Figure 3d** retains the resonance loop and adds an amplitude-control loop to stabilize lamp intensity. The circuit feeds back sensed lamp current to a voltage regulator to control the transformer's drive power. The regulator's reference point is variable, permitting a lamp-intensity setting at any desired level. The amplitude and resonance loops operate simultaneously but fully independently of each other. This two-loop operation is the key to high-power, wide-range, and reliable control.

**Figure 4** is a detailed schematic of **Figure 3d**'s concept. The resonance loop comprises $Q_3$ and the CMOS-inverter-based oscillator. The amplitude loop centers on the LT1375 switching regulator. **Figure 5** shows circuit waveforms. Traces A and B show $Q_2$ and $Q_1$ gate drives, respectively, and traces C and D are the resultant $Q_1$ and $Q_2$ drain responses. The LT1375 step-down switching regulator, responding to the rectified and averaged lamp current, closes the amplitude loop by driving the $L_1$-$L_2$ junction (Trace E). The 4.7-μF capacitor at the $V_C$ pin stabilizes the loop. The PZT transformer's acoustic transport speed furnishes an almost-pure delay in the loop, making compensation an interesting exercise (see additional information for this article at www.ednmag.com). Note that the design in **Figure 4** includes no filtering; the raw LT1375 500-kHz PWM output directly drives the $L_1$-$L_2$-PZT network. This direct drive is permissible because the PZT transformer's Q factor is so high that it responds only at resonance, as the half-sine waves of traces C and D indicate.

The feedback tap (Trace F) supplies phase-coherent information and looks like a current source to $Q_3$ under all conditions (note Trace F's vertical-scale factor). The 750-kΩ resistors in series minimize parasitic capacitance at the transformer feedback terminal. $Q_3$'s col-

lector (Trace G) clamps this information to a lower voltage and injection-locks the CMOS-inverter-based oscillator, which closes the resonance loop. The oscillator ensures start-up, just as in **Figure 3c**, and effectively filters the already-narrowband resonant feedback, further ensuring resonance-loop fidelity under all conditions. Trace H is the PZT transformer's high-voltage output delivered to the lamp. This example uses a potentiometer to set the dimming, although simple current summing to the LT1375 feedback pin also allows electronic control (**Reference 1**).

## ADDITIONAL CONSIDERATIONS AND BENEFITS

As mentioned, the PZT transformer has other benefits besides size. One of these benefits is safety. A PZT transformer cannot fail due to output shorts or opens. Short circuits knock the PZT transformer off-resonance, and it simply stops, absorbing no energy. Open circuits do not cause arc-induced PZT failures because arcing between turns, as in a magnetic transformer, can't occur. However, it is always wise to sense and arrest an overvoltage condition. Despite their size, PZT transformers are capable of large outputs. With a 10V supply, an uncontrolled PZT transformer can easily produce 3000V rms. This ability mandates some form of overvoltage protection in a production circuit.

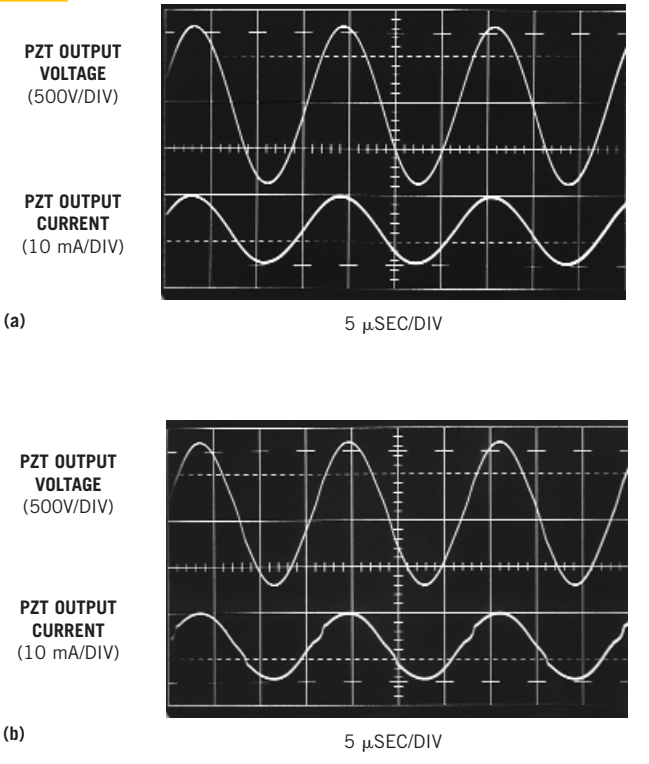
Another significant attribute is that the amplitude-control loop's scale factor is almost completely independent of load, including parasitic capacitance. The practical advantage is that you can use the same PZT-based inverter circuit with a range of displays with no recalibration of any kind. This feature is a distinct advantage over magnetically based inverters, which all require some form of scale-factor recalibration, either hardware- or software-based, when you change the display. Understanding this feature requires some study.

Almost all displays introduce some parasitic capacitance between the lamp, its leads, and electrically conductive elements within the display. Such elements may include the display enclosure, the lamp reflector, or both (**Figure 6**). The parasitic capacitance to ground has two major impacts. The capacitance absorbs energy, causing lost power. This power loss raises overall inverter input power because the inverter must supply both parasitic and intended load paths. Some techniques can minimize the effects of parasitic capacitance, but the compensation is never complete (**Reference 1**).

A second effect of parasitic capacitance, manifested in magnetically based inverters, is much subtler. A magnetically based inverter has a finite source impedance at frequency, which corrupts the produced sinusoid. The amount of parasitic capacitance influences the degree of corruption. Displays have varying amounts of parasitic capacitance, resulting in varying degrees of waveform dis-

tortion. The RC-averaging time-constant circuit of the magnetic and PZT-based inverters is not an rms-to-dc converter and produces different outputs as distortion content in its input waveform changes. The amplitude loop acts on the dc output of the RC-averaging circuit, and you generally assume that the input-waveform-distortion content is constant. In a well-designed magnetically based inverter, this fact is essentially true, even as operating conditions vary. The averaging circuit's output error is consistent, and you can "calibrate away" the error using scale-factor adjustments. However, changing the display type subjects the averaging circuit to a differently distorted waveform, and new scale-factor adjustments are necessary. Thus, some calibration-constant adjustment is necessary for each display type, complicating production and inventory requirements.

**Figure 7**




**When a PZT inverter drives a low-parasitic-capacitance display, the resulting waveforms are nearly ideal sinusoids (a). A display with higher capacitive loss causes minor distortion, but the lamp's rms current changes by only 0.5% (b).**

PZT-based inverters are largely immune to this problem because of their extraordinarily high Q factor, which is typically greater than 1000. The PZT transformer forces the output waveform to have a consistent amount of distortion, nominally zero. The PZT transformer's resonant mechanical filtering produces an almost-pure sinusoidal output, even with widely varying parasitic and intended loads. **Figure 7a** shows PZT output voltage (Trace A) and current (Trace B) with a low-parasitic-loss display. The waveshapes are essentially ideal sinusoids. **Figure 7b** shows the same waveforms with a much higher parasitic-loss display. Minor waveform distortion, particularly in the current trace, is evident, although minimal. The RC-averaging circuit produces little error compared with that in **Figure 7a**, and less than 0.5% lamp-current difference exists between the two cases. In contrast, a magnetically based inverter can easily suffer 10 to 15% lamp-current differences, which impact display luminosity and lamp lifetime.□

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